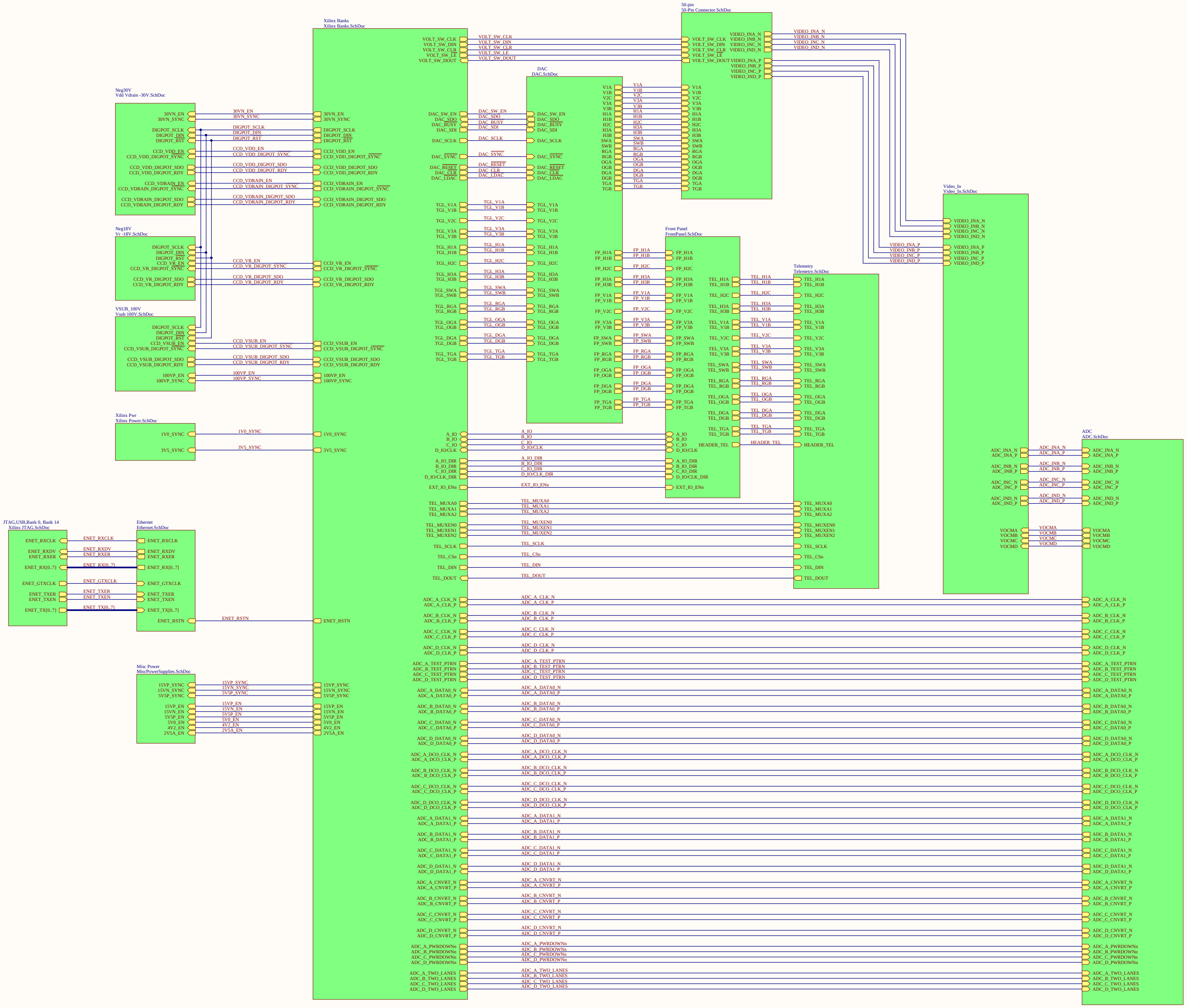
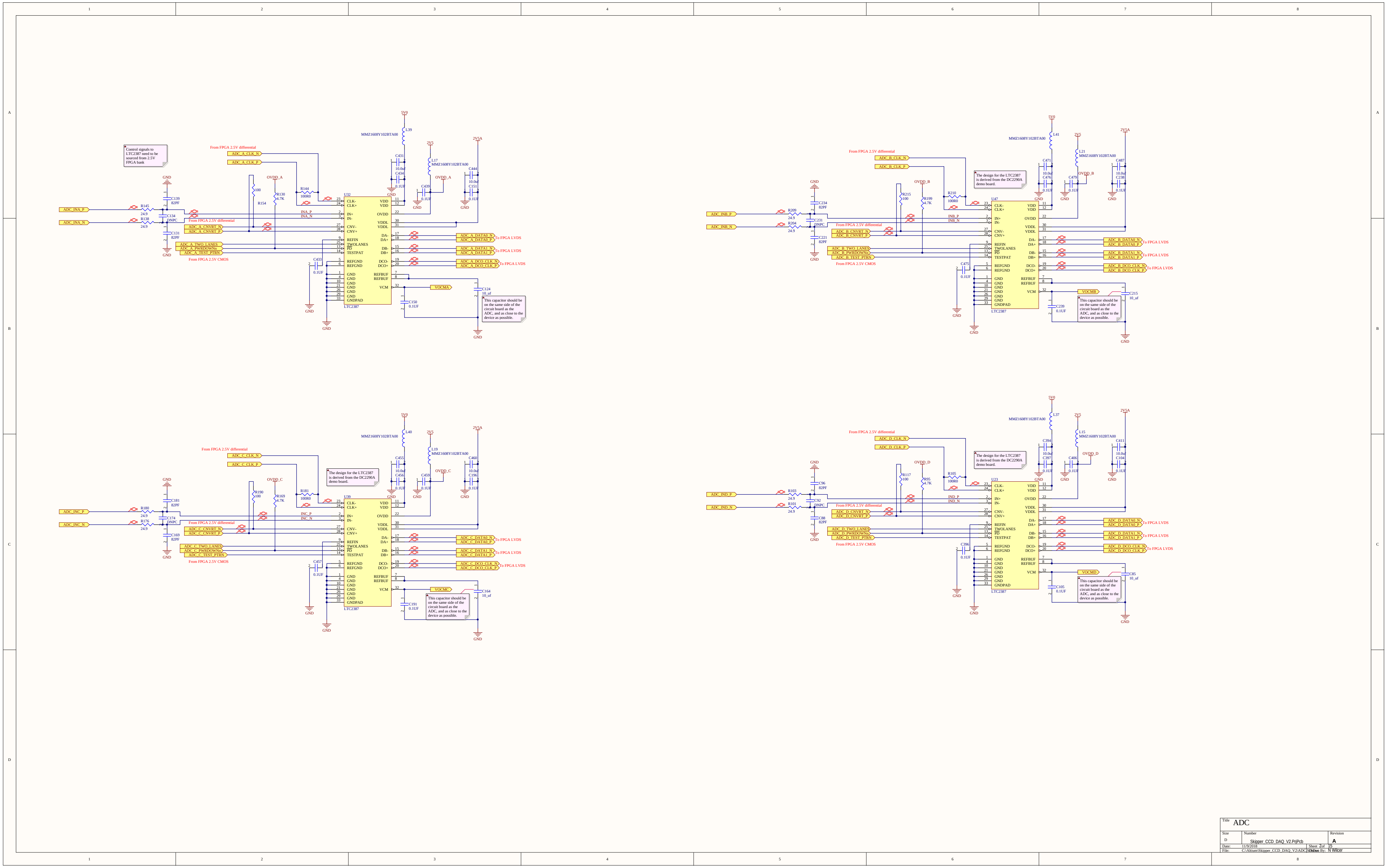
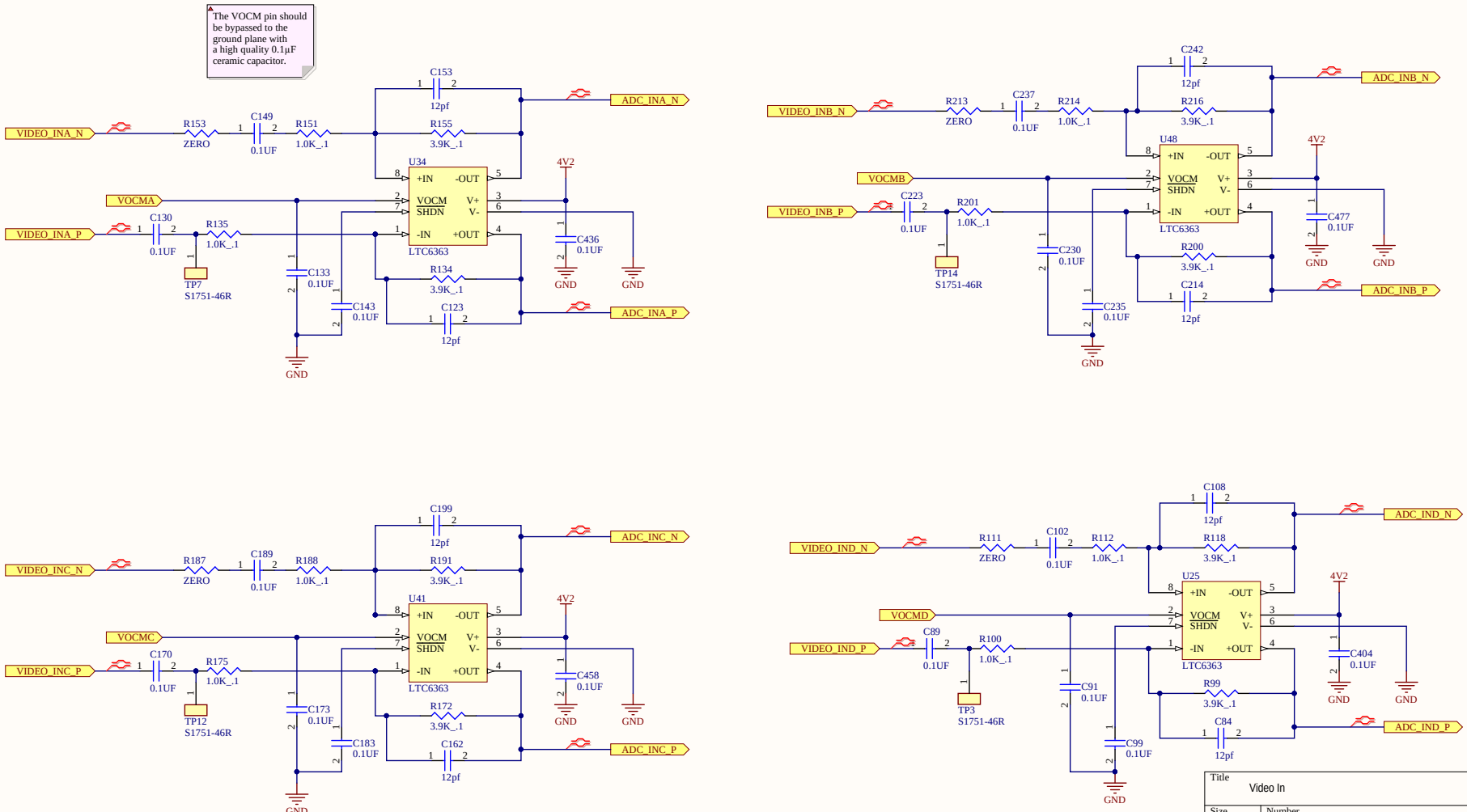
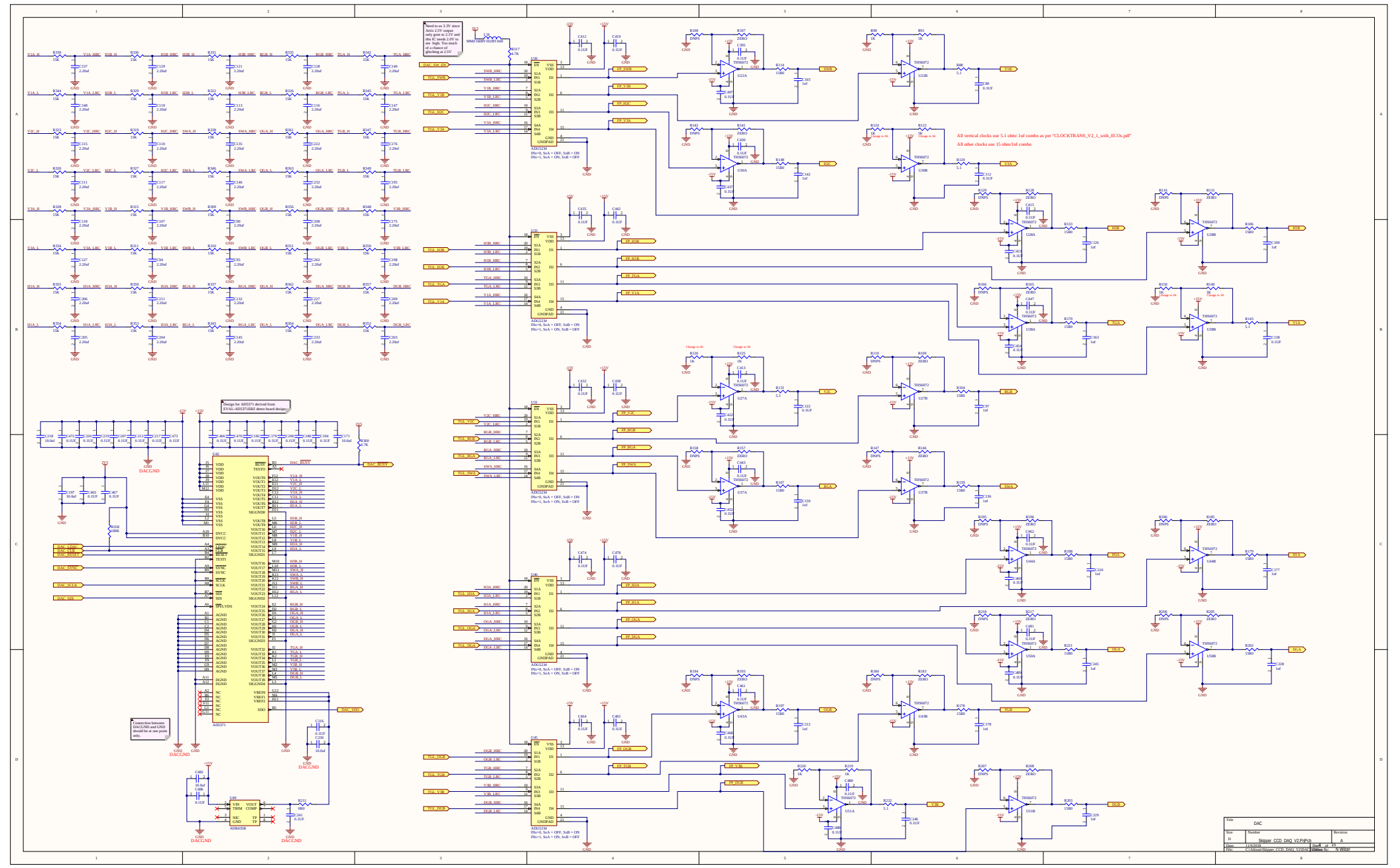
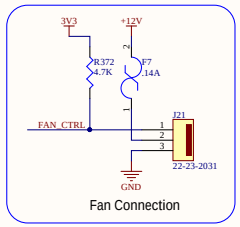

Xilinx Banks
Xilinx Banks.SchDoc
50-pin
50-Pin Connector.SchDoc
DAC
DAC.SchDoc
Neg30V
Vdd Vdrain -30V.SchDoc
Neg18V
Vr -18V.SchDoc
VSUB_100V
Vsub 100V.SchDoc
Xilinx Pwr
Xilinx Power.SchDoc
Front Panel
FrontPanel.SchDoc
Telemetry
Telemetry.SchDoc
Video_In
Video_In.SchDoc
ADC
ADC.SchDoc
JTAG,USB,Bank 0, Bank 14
Xilinx JTAG.SchDoc
Ethernet
Ethernet.SchDoc
Misc Power
MiscPowerSupplies.SchDoc

Title	Top	
Size: D	Number: Skipper_CCD_DAQ_V2.PrjPcb	Revision: A
Date: 11/9/2018		Sheet 1 of 15
File: C:\Altium\..\Skipper_CCD_DAQ.SchDoc		Drawn By: N Wilcer

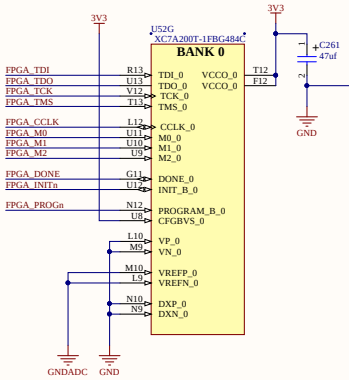

Control signals to LTC2387 need to be sourced from 2.5V FPGA bank
The design for the LTC2387 is derived from the DC2290A demo board.
This capacitor should be on the same side of the circuit board as the ADC, and as close to the device as possible.
From FPGA 2.5V differential
From FPGA 2.5V CMOS
To FPGA LVDS
LTC2387
MMZ1608Y102BTA00
ADC_INA_P
ADC_INA_N
ADC_INB_P
ADC_INB_N
ADC_INC_P
ADC_INC_N
ADC_IND_P
ADC_IND_N
5V0
2V5
2V5A
GND
Title ADC
Size D
Number Skipper_CCD_DAQ_V2.PrjPcb
Revision A
Date: 11/9/2018
Sheet 2 of 15
File: C:\Altium\Skipper_CCD_DAQ_V2\ADC.SchDoc
Drawn By: N Wilcer

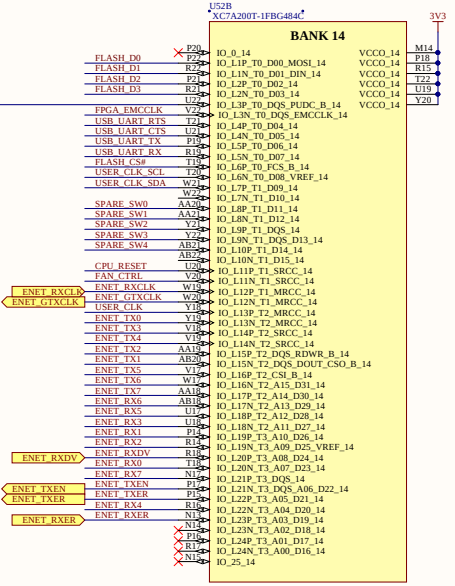

The VOCM pin should be bypassed to the ground plane with a high quality 0.1µF ceramic capacitor.
VIDEO_INA_N
R153
ZERO
C149
0.1UF
R151
1.0K_.1
C153
12pf
R155
3.9K_.1
ADC_INA_N
U34
+IN
-OUT
VOCM
V+
SHDN
V-
-IN
+OUT
LTC6363
4V2
VOCMA
VIDEO_INA_P
C130
0.1UF
R135
1.0K_.1
TP7
S1751-46R
C133
0.1UF
C143
0.1UF
R134
3.9K_.1
C123
12pf
C436
0.1UF
ADC_INA_P
GND
VIDEO_INB_N
R213
ZERO
C237
0.1UF
R214
1.0K_.1
C242
12pf
R216
3.9K_.1
ADC_INB_N
U48
VOCMB
VIDEO_INB_P
C223
0.1UF
R201
1.0K_.1
TP14
S1751-46R
C230
0.1UF
C235
0.1UF
R200
3.9K_.1
C214
12pf
C477
0.1UF
ADC_INB_P
VIDEO_INC_N
R187
ZERO
C189
0.1UF
R188
1.0K_.1
C199
12pf
R191
3.9K_.1
ADC_INC_N
U41
VOCMC
VIDEO_INC_P
C170
0.1UF
R175
1.0K_.1
TP12
S1751-46R
C173
0.1UF
C183
0.1UF
R172
3.9K_.1
C162
12pf
C458
0.1UF
ADC_INC_P
VIDEO_IND_N
R111
ZERO
C102
0.1UF
R112
1.0K_.1
C108
12pf
R118
3.9K_.1
ADC_IND_N
U25
VOCMD
VIDEO_IND_P
C89
0.1UF
R100
1.0K_.1
TP3
S1751-46R
C91
0.1UF
C99
0.1UF
R99
3.9K_.1
C84
12pf
C404
0.1UF
ADC_IND_P
Title
Video In
Size
B
Number
Skipper_CCD_DAQ_V2.PrjPcb
Revision
A
Date:
11/9/2018
Sheet 3of 15
File:
C:\Altium\..\Video_In.SchDoc
Drawn By:
N Wilcer

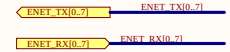

All vertical clocks use 5.1 ohm/.1uf combo as per "CLOCKTRANS_V2_1_with_ECOs.pdf"
All other clocks use 15 ohm/1nf combo
Design for AD5371 derived from EVAL-AD5371BZ demo board design.
Connection between DACGND and GND should be at one point only.
Need to on 3.3V since Actix 2.5V output only goes to 2.1V and this IC needs 2.0V to see 'high. Too much of a chance of glitching at 2.5V
Title: DAC
Size: D
Number: Skipper_CCD_DAQ_V2.PrjPcb
Revision: A
Date: 11/5/2010
Sheet 1 of 15
File: C:\Altium\Skipper CCD_DAQ_V2\DAC.SchDoc
Drawn By: B. Wicker

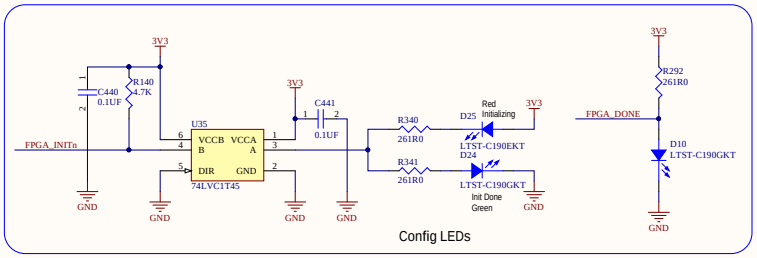


Fan Connection

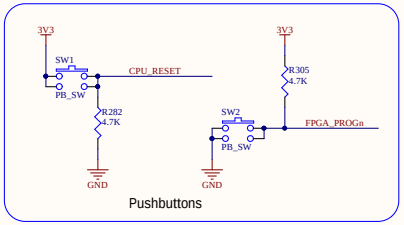




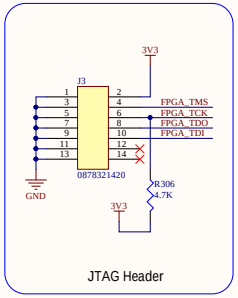




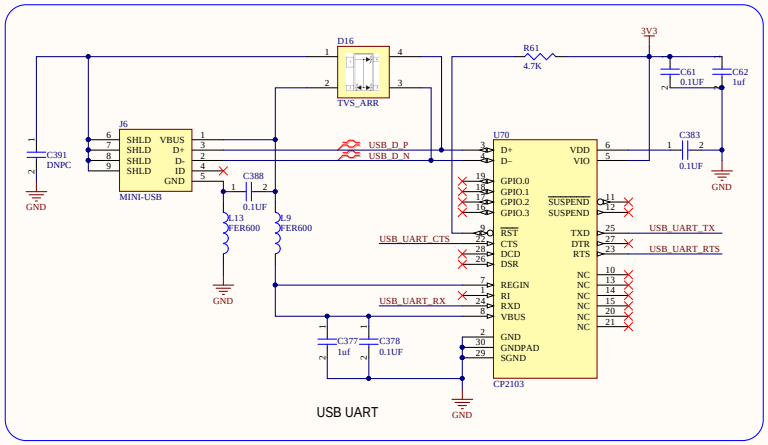
Config LEDs



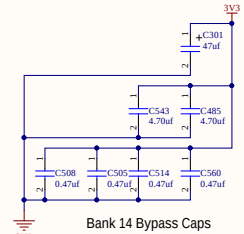
Pushbuttons



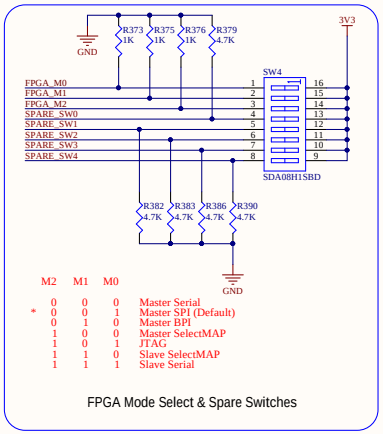
JTAG Header



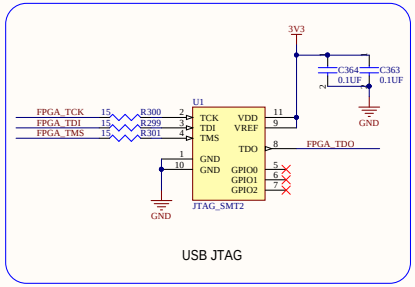
USB UART



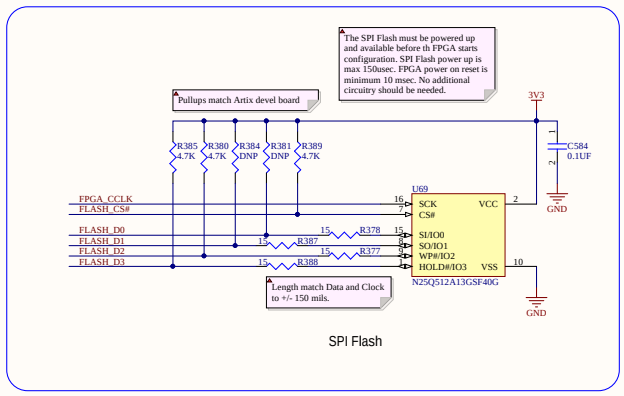
Bank 14 Bypass Caps



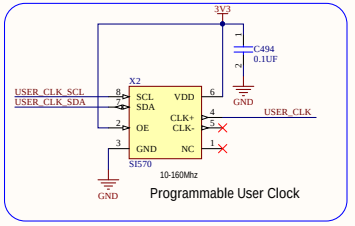
FPGA Mode Select & Spare Switches



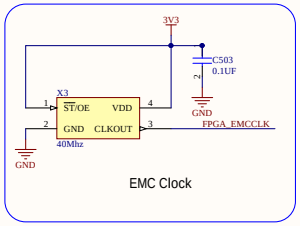
USB JTAG



SPI Flash

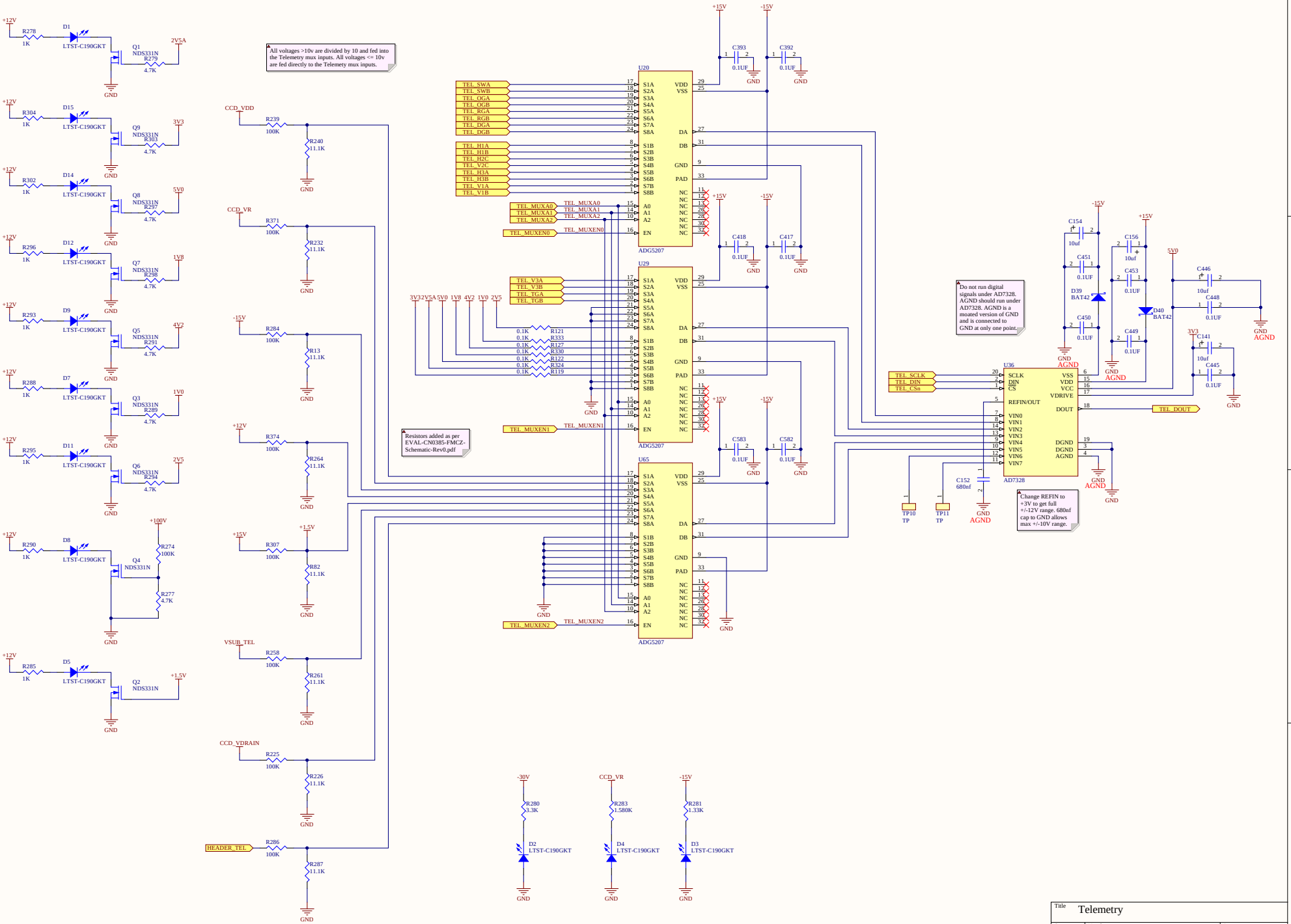


Programmable User Clock



EMC Clock

Title	JTAG, USB , Flash, Bank 0, Ethernet, Bank 14
Size	C
Number	Skipper_CCD_DAQ_V2.PrjPcb
Revision	
Date:	11/9/2018
Sheet	of
File:	C:\Altium\..\Xilinx JTAG.SchDoc
Drawn By:	


All voltages >10v are divided by 10 and fed into the Telemetry mux inputs. All voltages <= 10v are fed directly to the Telemetry mux inputs.
Resistors added as per EVAL-CN0385-FMCZ-Schematic-Rev0.pdf
Do not run digital signals under AD7328. AGND should run under AD7328. AGND is a moated version of GND and is connected to GND at only one point.
Change REFIN to +3V to get full +/-12V range. 680nf cap to GND allows max +/-10V range.
U20
U29
U65
ADG5207
U36
AD7328
TEL_SWA
TEL_SWB
TEL_OGA
TEL_OGB
TEL_RGA
TEL_RGB
TEL_DGA
TEL_DGB
TEL_H1A
TEL_H1B
TEL_H2C
TEL_V2C
TEL_H3A
TEL_H3B
TEL_V1A
TEL_V1B
TEL_V3A
TEL_V3B
TEL_TGA
TEL_TGB
TEL_MUXA0
TEL_MUXA1
TEL_MUXA2
TEL_MUXEN0
TEL_MUXEN1
TEL_MUXEN2
TEL_SCLK
TEL_DIN
TEL_CSn
TEL_DOUT
CCD_VDD
CCD_VR
CCD_VDRAIN
VSUB_TEL
HEADER_TEL
+12V
-15V
+15V
-30V
+100V
+1.5V
2V5A
3V3
5V0
1V8
4V2
2V5
1V0
1V2
GND
AGND
Title
Telemetry
Size
C
Number
Skipper_CCD_DAQ_V2.PrjPcb
Revision
Date:
11/9/2018
Sheet of
File:
C:\Altium\..\Telemetry.SchDoc
Drawn By:

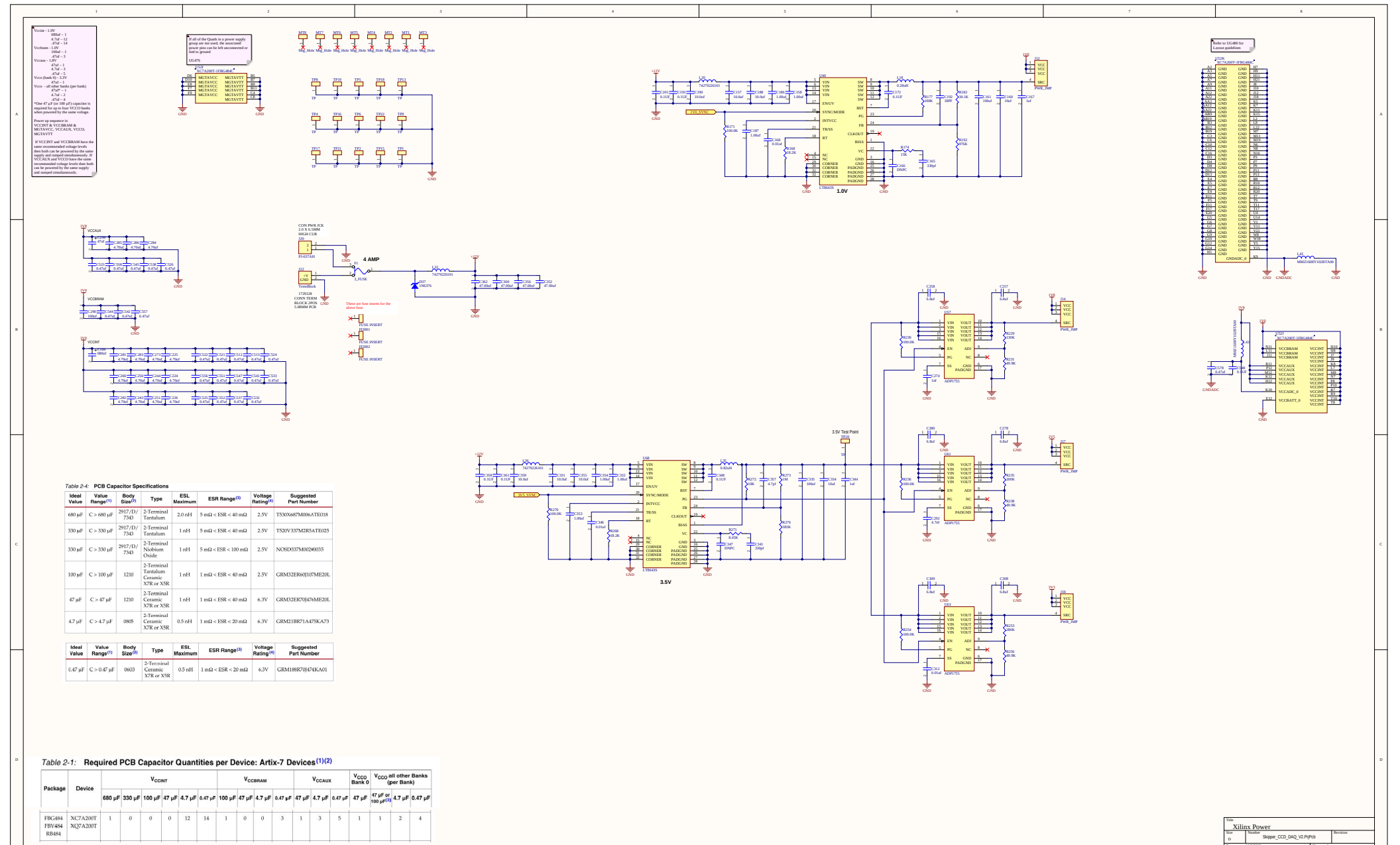


Table 2-4: **PCB Capacitor Specifications**

Ideal Value	Value Range[1]	Body Size[5]	Type	ESL Maximum	ESR Range[3]	Voltage Rating[4]	Suggested Part Number
680 µF	C > 680 µF	2917/D/7343	2-Terminal Tantalum	2.0 nH	5 mΩ < ESR < 40 mΩ	2.5V	T530X687M006ATE018
330 µF	C > 330 µF	2917/D/7343	2-Terminal Tantalum	1 nH	5 mΩ < ESR < 40 mΩ	2.5V	T520V337M2R5ATE025
330 µF	C > 330 µF	2917/D/7343	2-Terminal Niobium Oxide	1 nH	5 mΩ < ESR < 100 mΩ	2.5V	NOSD337M002#0035
100 µF	C > 100 µF	1210	2-Terminal Tantalum Ceramic X7R or X5R	1 nH	1 mΩ < ESR < 40 mΩ	2.5V	GRM32ER60J107ME20L
47 µF	C > 47 µF	1210	2-Terminal Ceramic X7R or X5R	1 nH	1 mΩ < ESR < 40 mΩ	6.3V	GRM32ER70J476ME20L
4.7 µF	C > 4.7 µF	0805	2-Terminal Ceramic X7R or X5R	0.5 nH	1 mΩ < ESR < 20 mΩ	6.3V	GRM21BR71A475KA73

Ideal Value	Value Range[1]	Body Size[5]	Type	ESL Maximum	ESR Range[3]	Voltage Rating[4]	Suggested Part Number
0.47 µF	C > 0.47 µF	0603	2-Terminal Ceramic X7R or X5R	0.5 nH	1 mΩ < ESR < 20 mΩ	6.3V	GRM188R70J474KA01

Table 2-1: **Required PCB Capacitor Quantities per Device: Artix-7 Devices[1][2]**

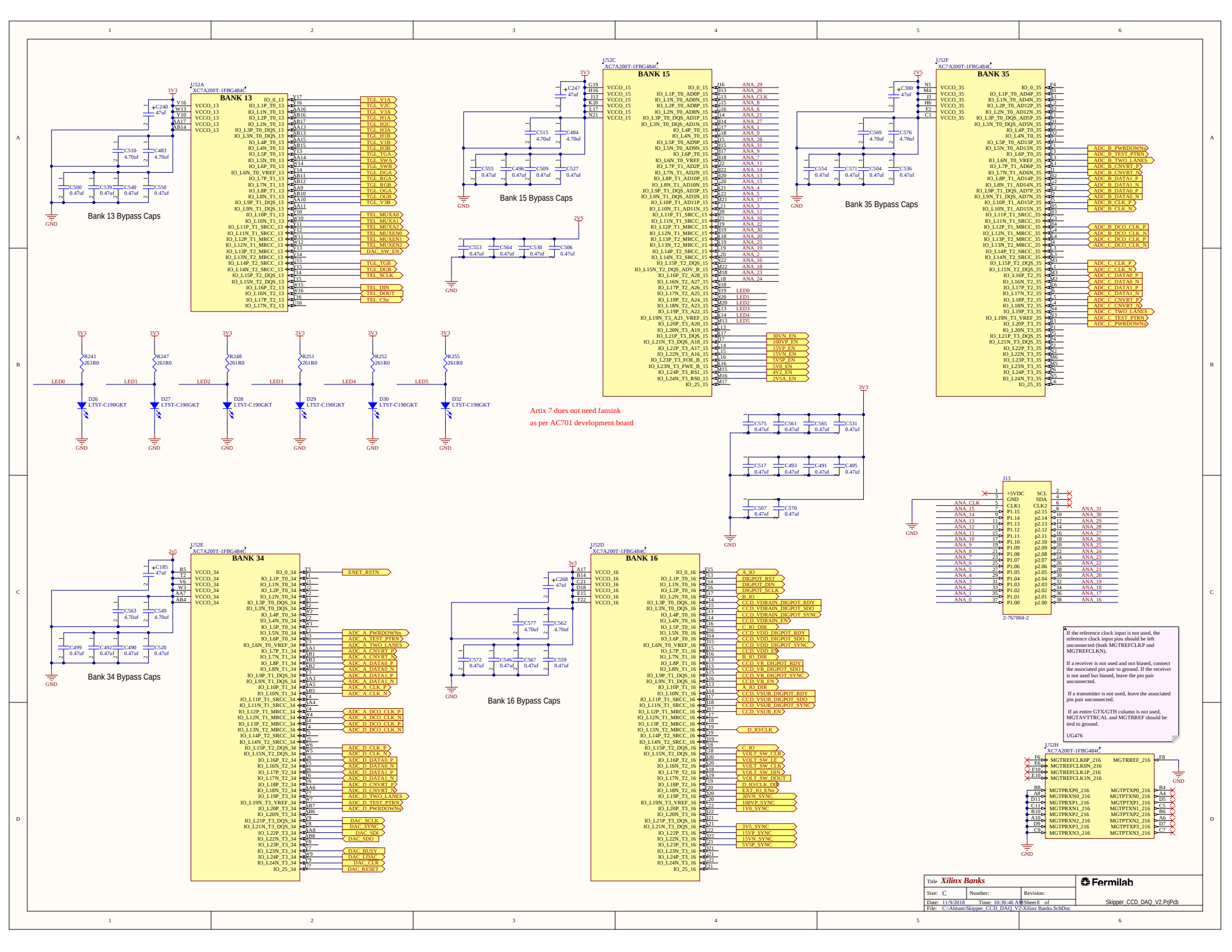
Package	Device	V_{CCINT}						V_{CCBRAM}				V_{CCAUX}			V_{CCO} Bank 0	V_{CCO} all other Banks (per Bank)		
		680 µF	330 µF	100 µF	47 µF	4.7 µF	0.47 µF	100 µF	47 µF	4.7 µF	0.47 µF	47 µF	4.7 µF	0.47 µF	47 µF	47 µF or 100 µF[3][4]	4.7 µF	0.47 µF
FBG484 FBV484 RB484	XC7A200T XQ7A200T	1	0	0	0	12	14	1	0	0	3	1	3	5	1	1	2	4

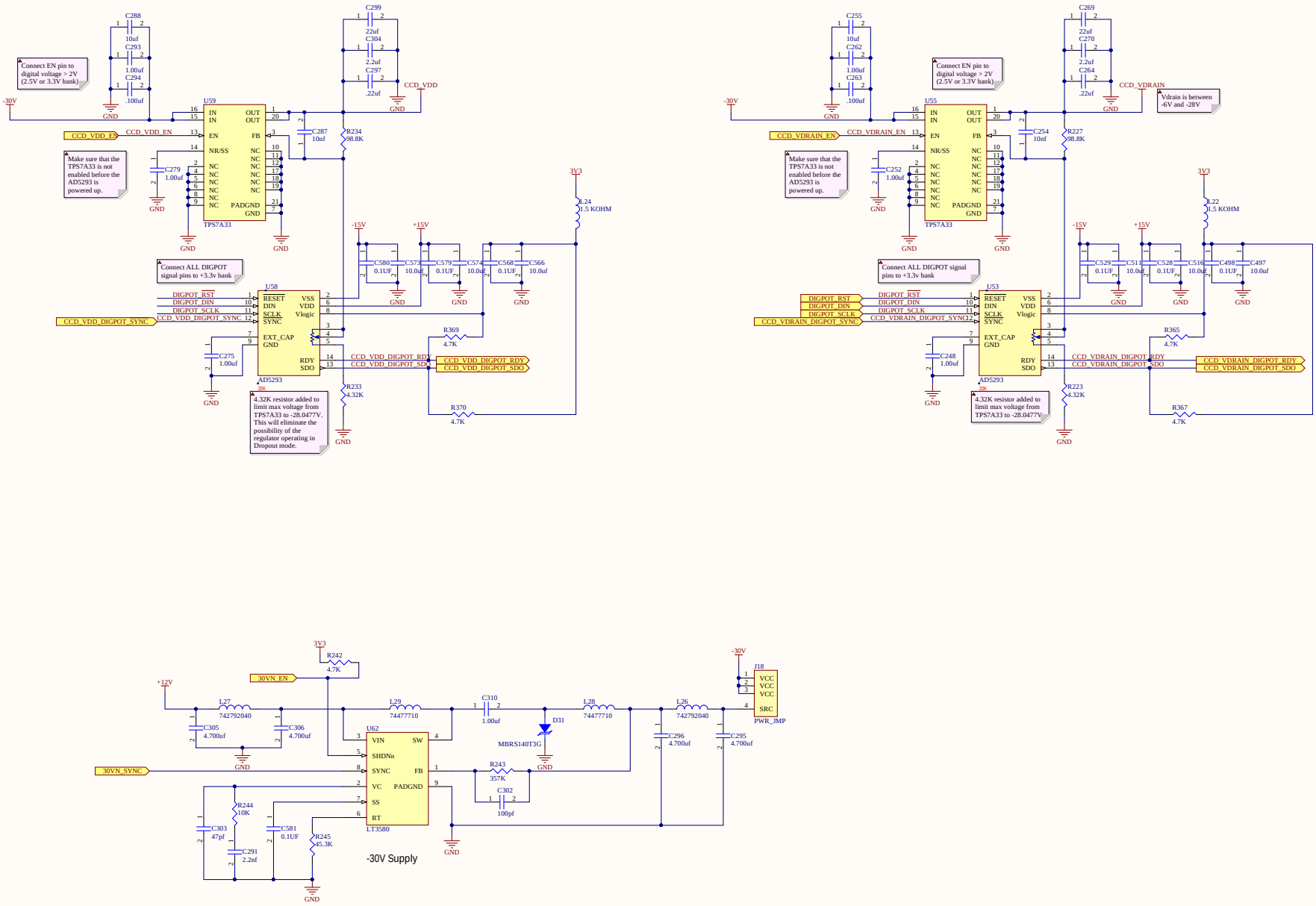
Xilinx Power

Skipper_CCD_DAQ_V2.PrjPcb

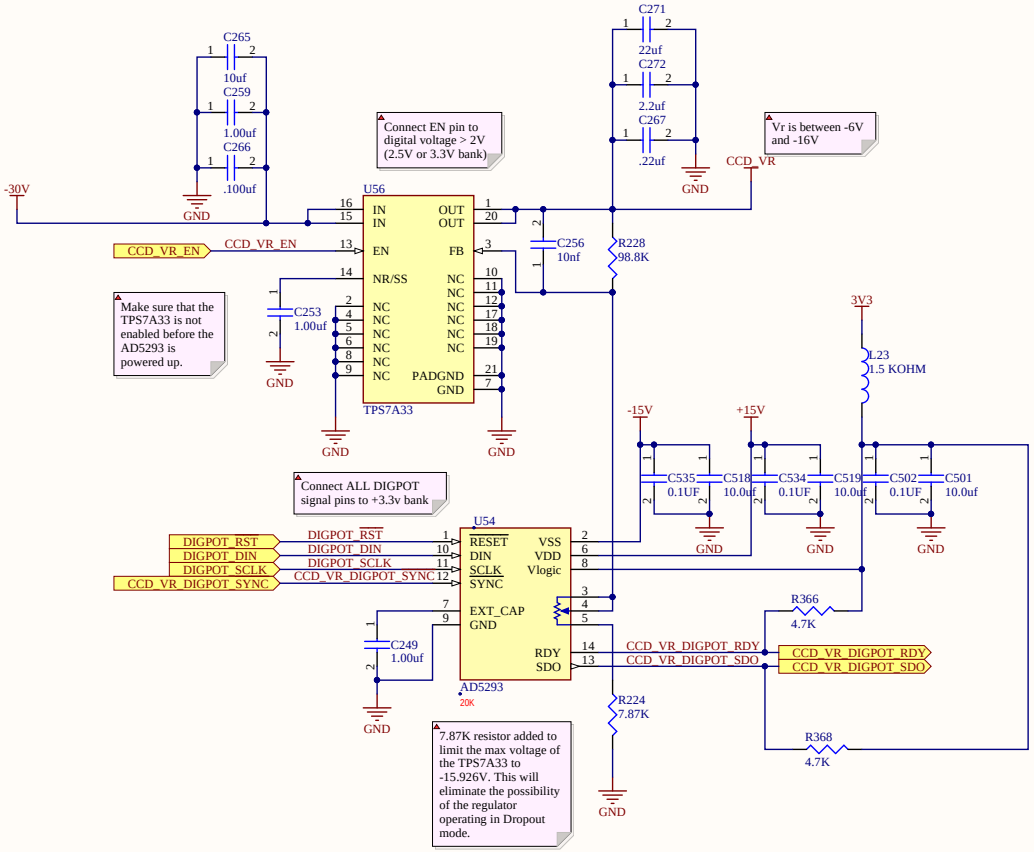
11/5/2018

C:\Xilinx\...\Xilinx Power.SchDoc

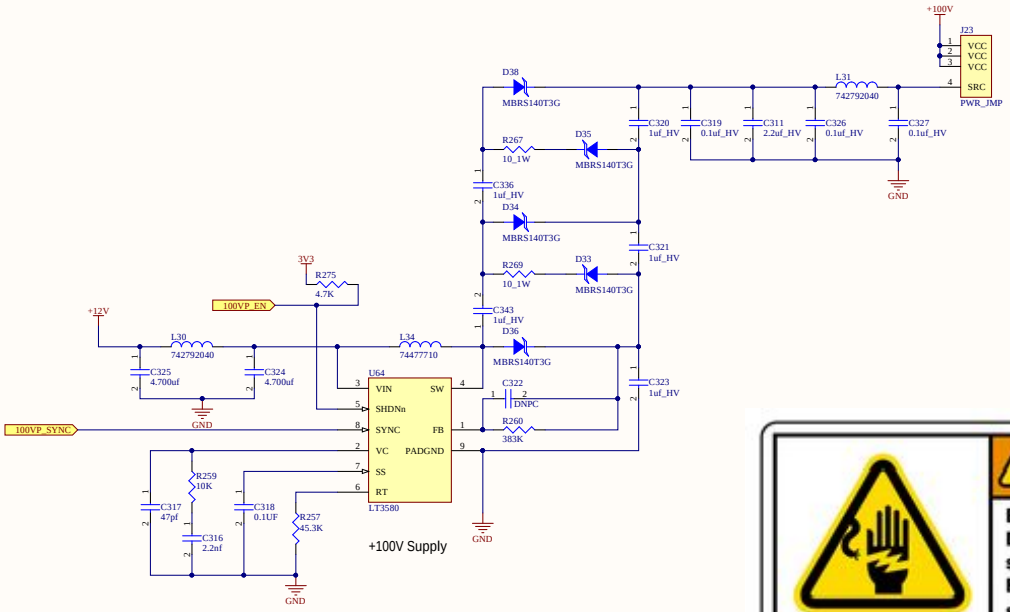

U52A
XC7A200T-1FBG484C
BANK 13
Bank 13 Bypass Caps
U52C
BANK 15
Bank 15 Bypass Caps
U52F
BANK 35
Bank 35 Bypass Caps
LED0
LED1
LED2
LED3
LED4
LED5
D26 LTST-C190GKT
D27 LTST-C190GKT
D28 LTST-C190GKT
D29 LTST-C190GKT
D30 LTST-C190GKT
D32 LTST-C190GKT
Artix 7 does not need fansink
as per AC701 development board
U52E
BANK 34
Bank 34 Bypass Caps
U52D
BANK 16
Bank 16 Bypass Caps
J13
2-767004-2
U52H
If the reference clock input is not used, the reference clock input pins should be left unconnected (both MGTREFCLKP and MGTREFCLKN).
If a receiver is not used and not biased, connect the associated pin pair to ground. If the receiver is not used but biased, leave the pin pair unconnected.
If a transmitter is not used, leave the associated pin pair unconnected.
If an entire GTX/GTH column is not used, MGTAVTTRCAL and MGTRREF should be tied to ground.
UG476
Title Xilinx Banks
Size: C
Number:
Revision:
Date: 11/9/2018
Time: 10:36:46 AM
Sheet 8 of
File: C:\Altium\Skipper_CCD_DAQ_V2\Xilinx Banks.SchDoc
Fermilab
Skipper_CCD_DAQ_V2.PrjPcb

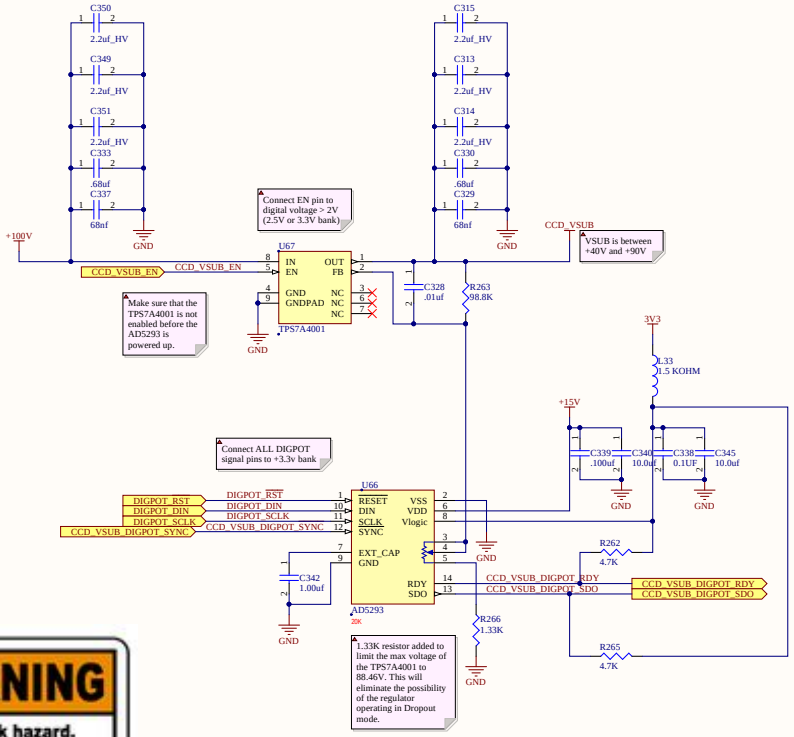


Title	Vdd Vdrain -30V	
Size: C	Number: Skipper_CCD_DAQ_V2.PrjPcb	Revision: A
Date: 11/9/2018	Sheet 9of 15	
File: C:\Altium\..\Vdd Vdrain -30V.SchDoc	Drawn By:	



Title	Vr -18V	
Size: B	Number: Skipper_CCD_DAQ_V2.PrjPcb	Revision: A
Date: 11/9/2018	Sheet 10 of 15	
File: C:\Altium\..\Vr -18V.SchDoc	Drawn By: Neal Wilcer	





Title	VSUB 100v	
Size: C	Number: Skipper_CCD_DAQ_V2.PrjPcb	Revision: A
Date: 11/9/2018	Sheet 11 of 15	
File: C:\Altium\..\Vsub 100V.SchDoc	Drawn By: Neal Wilcer	

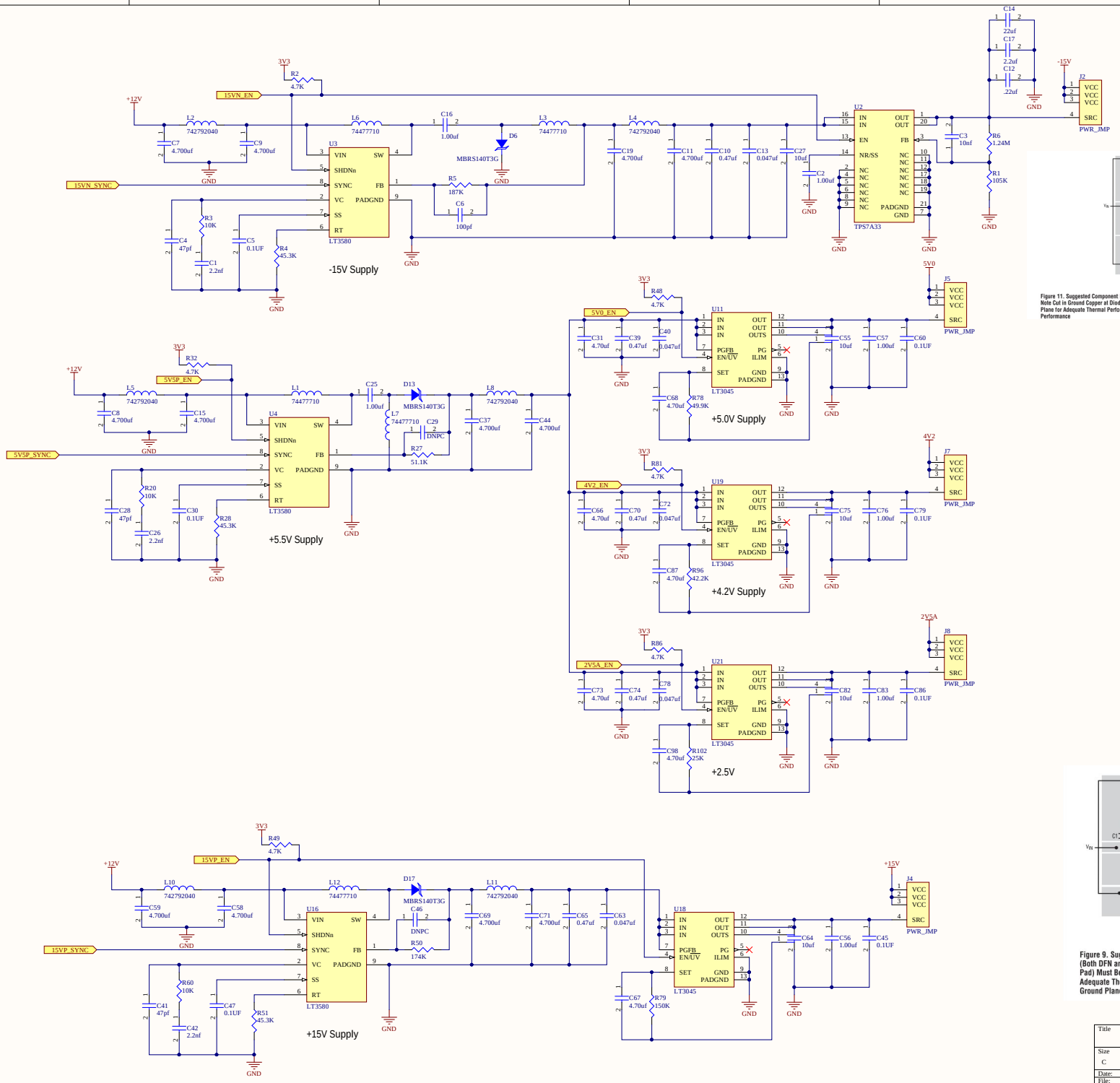


Figure 11. Suggested Component Placement for Inverting Topology (Both DFN and MSOP Packages. Not to Scale). Note Cut in Ground Copper at Diode's Cathode. Pin 9 (Exposed Pad) Must be Soldered Directly to Local Ground Plane for Adequate Thermal Performance. Multiple Vias to Additional Ground Planes Will Improve Thermal Performance

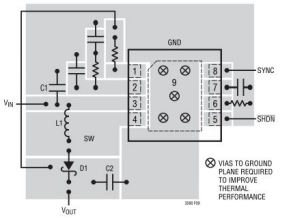
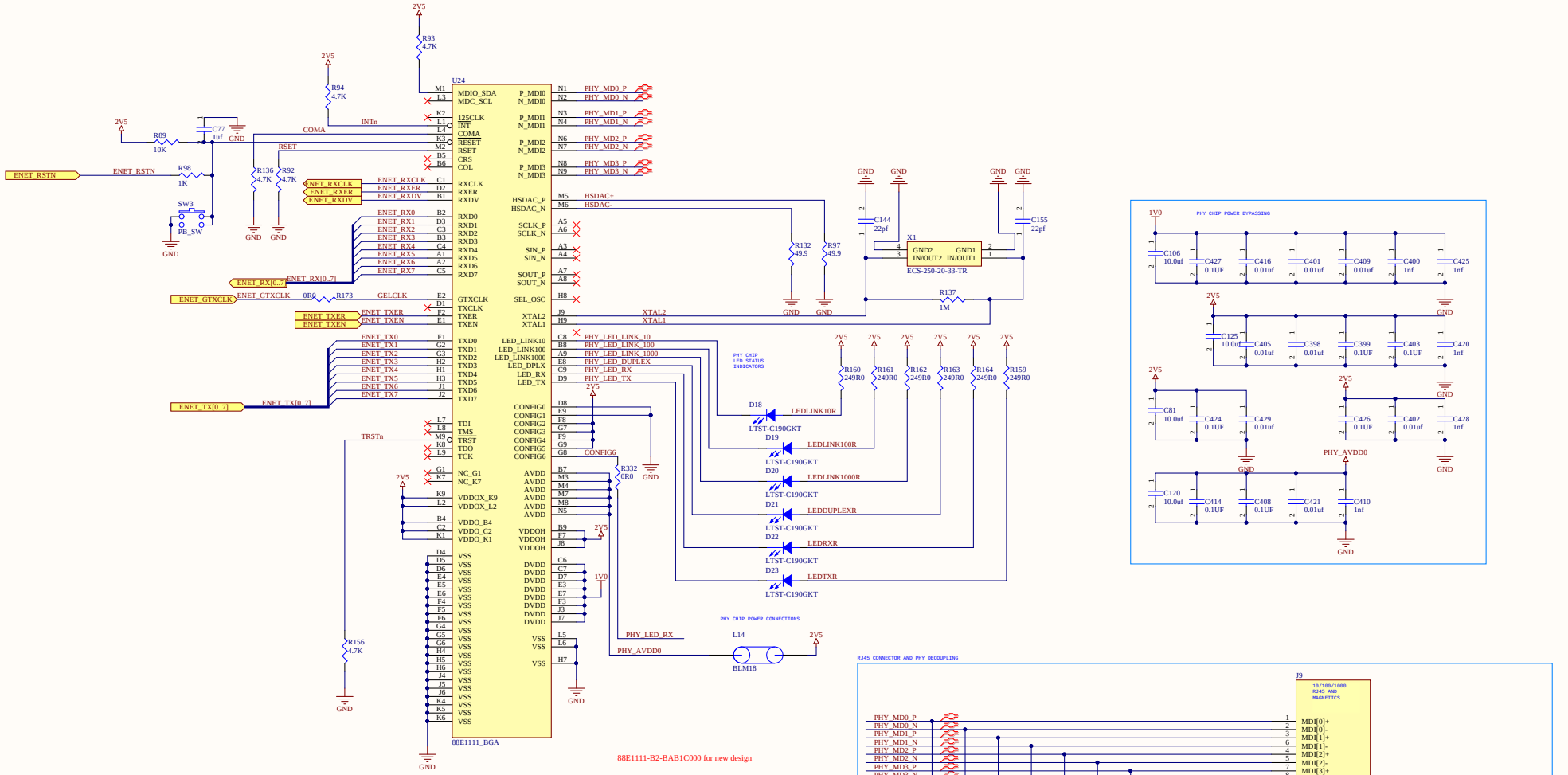
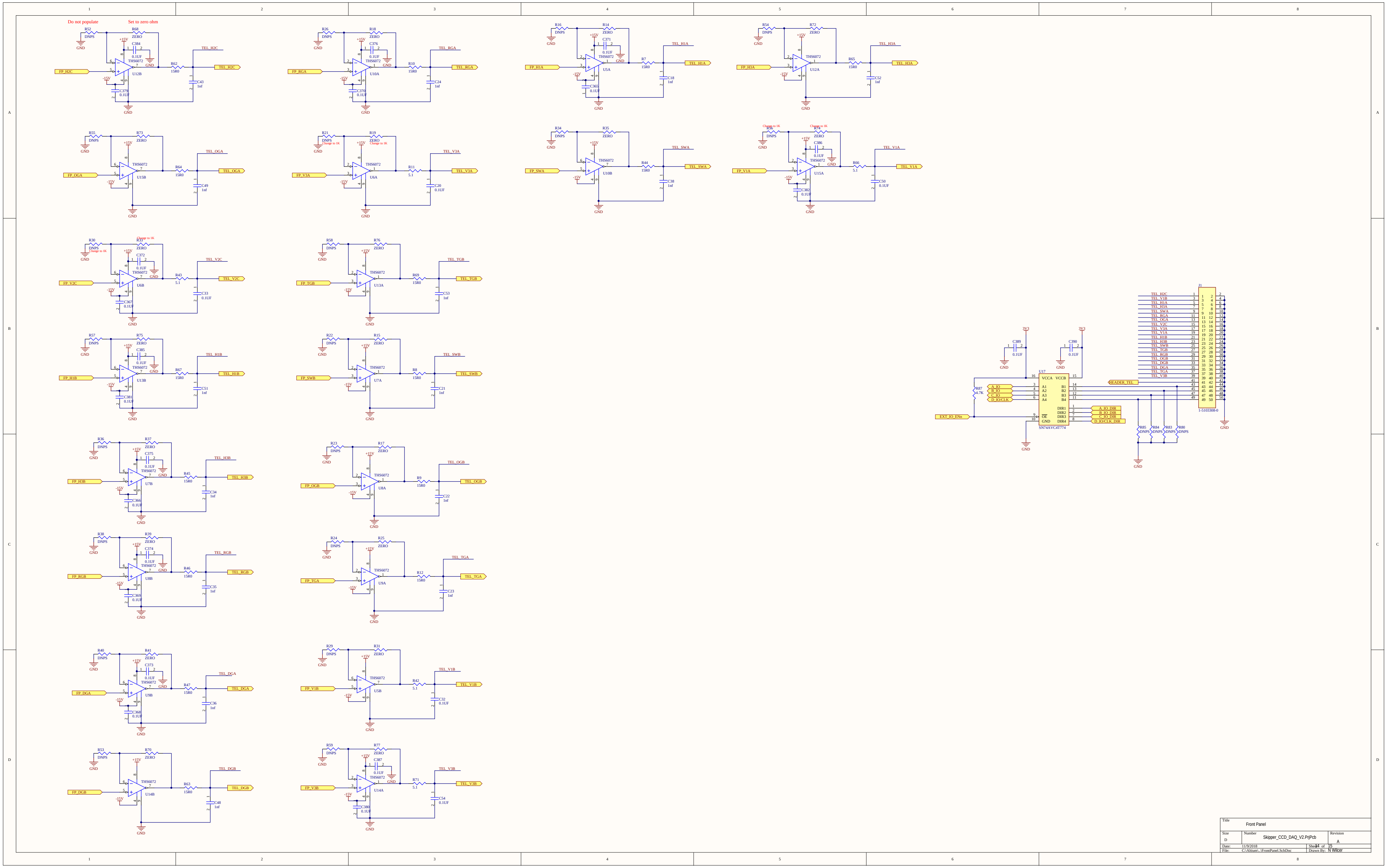


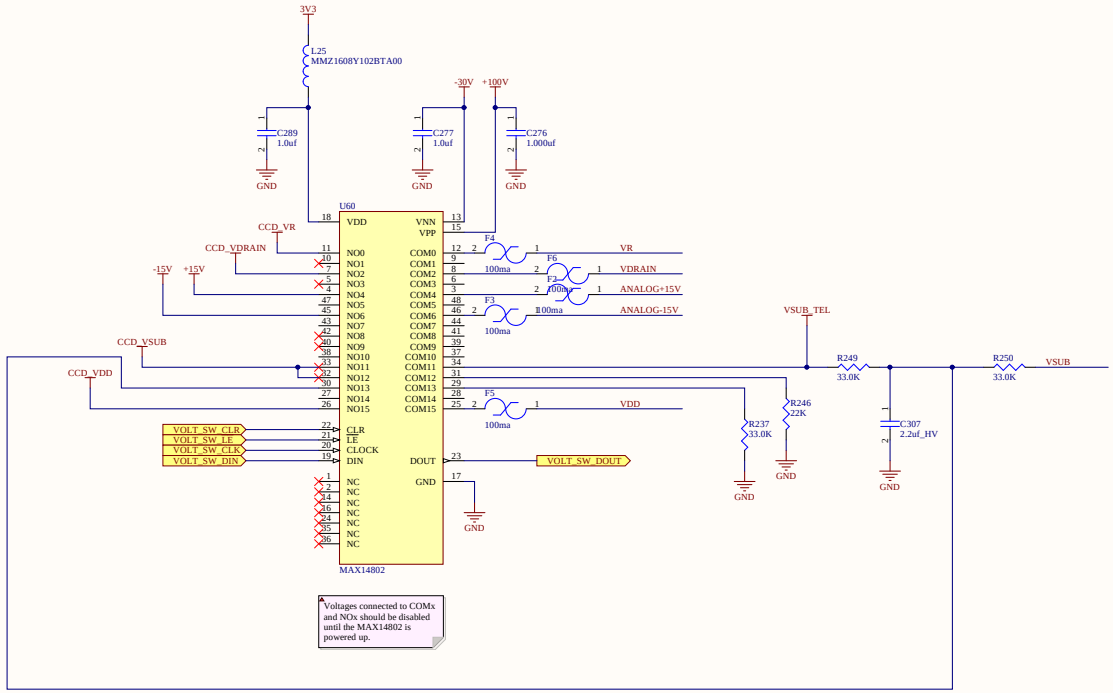
Figure 9. Suggested Component Placement for Boost Topology (Both DFN and MSOP Packages. Not to Scale). Pin 9 (Exposed Pad) Must Be Soldered Directly to the Local Ground Plane for Adequate Thermal Performance. Multiple Vias to Additional Ground Planes Will Improve Thermal Performance

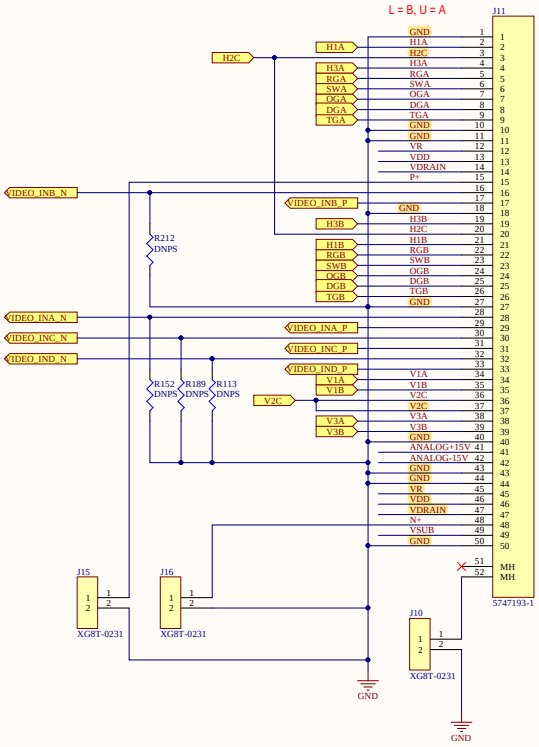
Title	Misc Power Supplies	
Size: C	Number: Skipper_CCD_DAQ_V2.PrjPcb	Revision: A
Date: 11/9/2018	Sheet 12 of 15	
File: C:\Altium\..\MiscPowerSupplies.SchDoc	Drawn By: Neal Wilcer	



Title	Ethernet
Size	C
Number	Skipper_CCD_DAQ_V2.PrjPcb
Revision	A
Date:	11/9/2018
Sheet	13 of 15
File:	C:\Altium\..\Ethernet.SchDoc
Drawn By:	Neal Wilcer


Do not populate
Set to zero ohm
Title
Front Panel
Size
D
Number
Skipper_CCD_DAQ_V2.PrjPcb
Revision
A
Date: 11/9/2018
Sheet 14 of 15
File: C:\Altium\..\FrontPanel.SchDoc
Drawn By: N Wilcer





Title	50-Pin Connector	
Size: C	Number: Skipper_CCD_DAQ_V2.PrjPcb	Revision: A
Date: 11/9/2018	Sheet 15 of 15	
File: C:\Altium\..\50-Pin Connector.SchDoc	Drawn By: N Wilcer	