Readout of the MAPS vertex detector at sPHENIX

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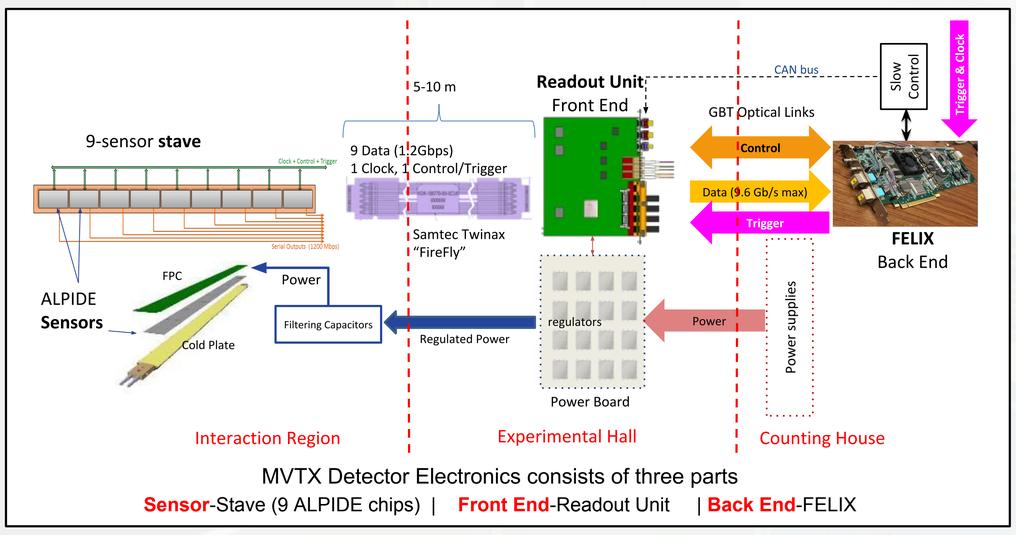
Abstract

The MVTX detector will serve as the micro-vertex tracking detector of the sPHENIX experiment at RHIC. It is an extremely precise silicon pixel vertex detector, with excellent displaced secondary vertex detecting capabilities. The MVTX will enable key measurements of heavy-flavor-tagged jets and B-mesons in heavy ion collisions. The detector is based on the latest generation of Monolithic Active Pixel Sensors (MAPS) technology, developed for the ALICE collaboration at CERN.
The readout chain is comprised of three parts: a sensor stave assembly, a RU (Readout Unit) board, and a FELIX (Front End LInk eXchange) board. The stave assembly consists of 9 ALPIDE (ALice PIxel DEtector) sensor chips, which will send its data on 9 gigabit links over a FireFly cable to an RU board. The RU board consists of two FPGA's, one for reading the stave data and sending data using CERN's rad-hard GBT links over fiber to the FELIX board and a second FPGA which is used for scrubbing (SEU detection). The FELIX board consists of an FPGA that reads out the the data over the fiber link and sends its data to a 16 lane PCIe interface, placing the data to disk.
We will present the R&D efforts and performance achievements for the three parts of the Readout system mentioned above.

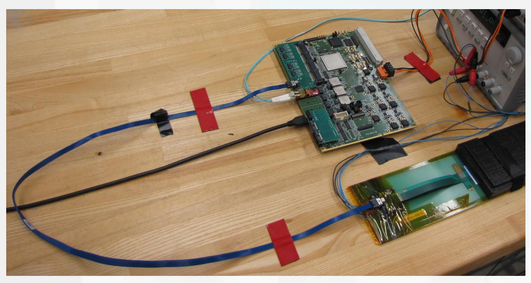
MVTX Readout System

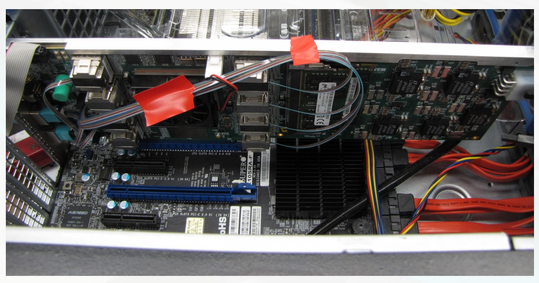


- FELIX and Readout Unit are integrated: FELIX sends triggers and aggregates RU data
- MVTX is integrated into the sPHENIX DAQ: working rcdaq plugin for FELIX and online data decoding/monitoring of ALPIDE data

Lab R&D

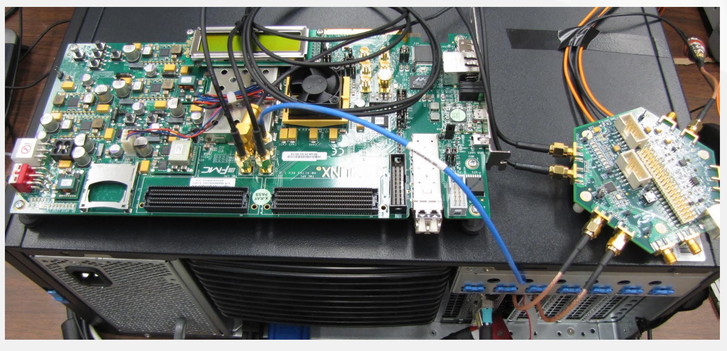
- Successful readout of single ALPIDE in internal pulsing mode, with full 15 kHz sPHENIX trigger rate and occupancy
- Successful readout of multiple ALPIDEs on a stave
- FELIX data rate test: 8-channel loopback of emulated RU data at 15 kHz trigger rate demonstrates full MVTX data rate

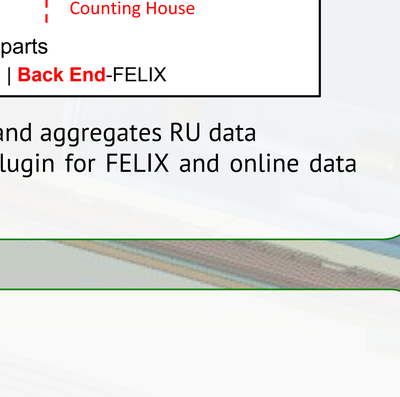




Test Beam

- Successful readout of four-ALPIDE telescope using external trigger (up to 7 kHz), external clock, and a range of threshold, shaping, and trigger latency parameters
  - Hit efficiency >99.5%, further analysis in progress

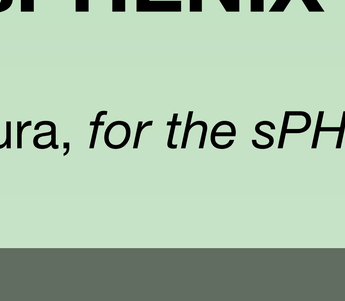


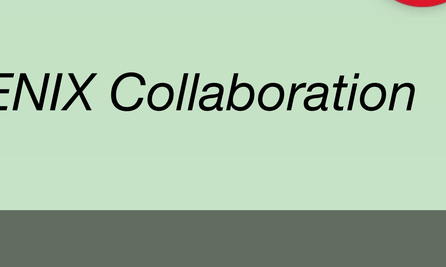


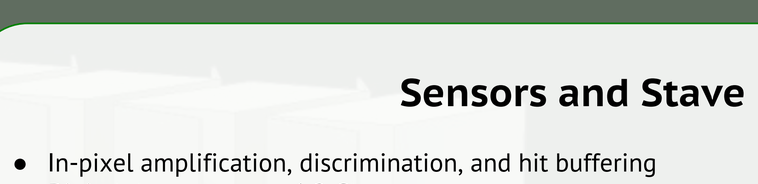
Sensors and Stave

- In-pixel amplification, discrimination, and hit buffering
- Digital data output at 1.2 Gbps
- Integrated test and masking

In pixel:
Amplification
Discrimination
3 hit storage registers







Stave– 9 chips, common clock and control, independent data lines

To Readout Unit: Samtec FireFly twinax cable
- 9 independent 1.2 Gbps data streams
- Common 40 MHz clock
- Common control line

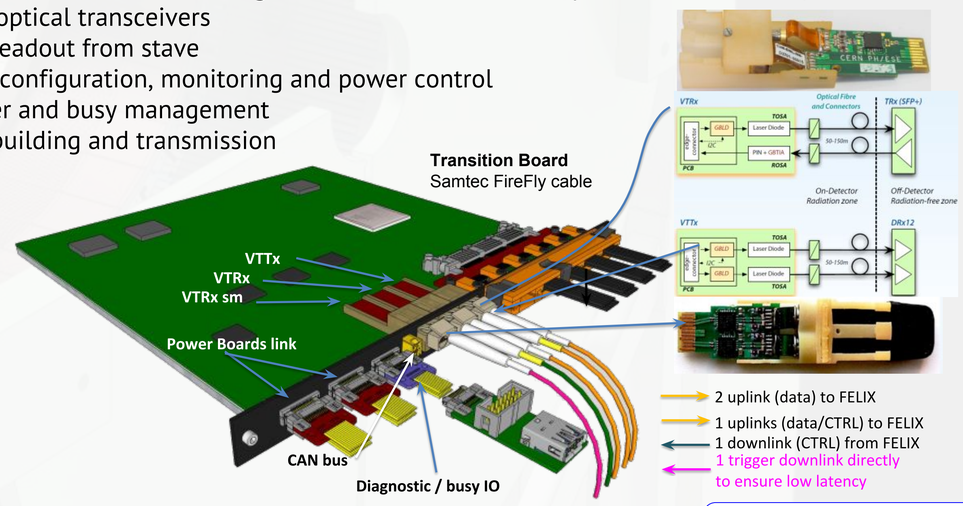
1 stave per Readout Unit

To stave: transition board
- control and clock outputs
- up to 27 inputs for 1.2 Gbps data streams from ALPIDEs

Readout Unit

The Readout Units will be located inside the experimental hall and just outside the magnet, approximately 5 meters from the staves.

- Radiation tolerant: logic is triplicated in Kintex Ultrascale main FPGA, rad-hard ProAsic3 FPGA scrubs the main FPGA
- Optical communication using radiation-hard CERN components: GBTx ASIC, VTRx and VTTx optical transceivers
- Data readout from stave
- Stave configuration, monitoring and power control
- Trigger and busy management
- Data building and transmission



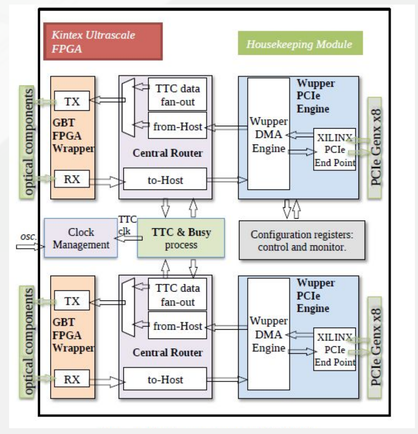
To FELIX: rad-hard 4.8 Gbps GBT optical links

8 Readout Units per FELIX

To Readout Units: 48 bidirectional GBT links

FELIX

- Data readout from 8 Readout Units
- Slow control and monitoring to/from sensors
- Trigger and timing interface
- Data aggregation and subevent packaging
- Data transmission through PCIe to server CPU



To DAQ: 16 lane Gen3 PCIe (>100 Gbps)

6 FELIX boards for full MVTX detector

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