MVTX progress report

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Interface to sPHENIX

- Goal: understand sPHENIX infrastructures, and build our software and firmware to work with sPHENIX
  - We are bridging two systems that have been defined for us: ALICE ITS and sPHENIX. This subtask deals with the sPHENIX side and the "glue," other subtasks deal with work to be done on the ITS/MVTX side (including FELIX).
  - BNL has promised significant help related to integrating FELIX with sPHENIX (sPHENIX TPC is also using FELIX)
- DAQ: Need to get data from FELIX card to sPHENIX DAQ
  - Plan: Develop an rcdaq plugin for MVTX (rcdaq is a lightweight DAQ system meant to be compatible with the PHENIX/sPHENIX DAQ), develop file format and analysis/monitoring software
    - ★ This will be our test beam DAQ
    - ★ It is promised that if we have MVTX working with rcdaq, integration work with the "real" sPHENIX DAQ will be minimal
    - ★ BNL has promised to write a basic rcdaq plugin for FELIX
- Timing, trigger, control (TTC): FELIX must use the sPHENIX system instead of the ATLAS system
  - FELIX v2.0 will have a "timing mezzanine" card, with ATLAS and sPHENIX options: BNL will take care of this
  - FELIX can lock its clocks to either the 40 MHz LHC clock or the 10 MHz RHIC clock, so RU and ALPIDE don't see any difference
- Detector control system (DCS): need to insert detector status data in DAQ

Readout firmware

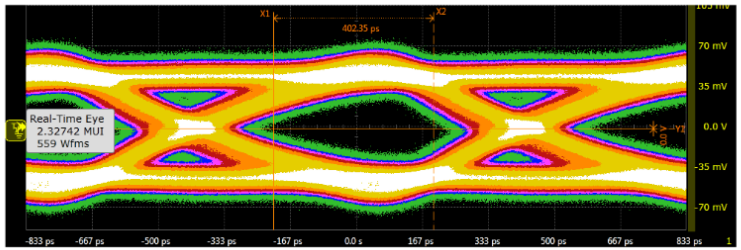
- Goal: develop firmware for RU and FELIX with all necessary functions (DAQ, TTC, DCS)
  - Ideally we will not need to make any changes to the RU firmware: the only change to the RU interfaces is that the ALICE CRU and LTU are both replaced by the FELIX
- We can compile the provided FELIX firmware
  - Given to us: GBT links to communicate with RU, DMA engine to push data out through PCIe
  - What we need to do: recognize, package, and compress data coming from the RU, configure, control, and trigger the RU
  - So far we can put fake data on a GBT output, loop it back on a fiber to a GBT input, push it to PCIe and write it to disk using FELIX software
  - Next step: take all the GBT inputs, mux+pack data so we can read out all links over PCIe
- Asked ALICE firmware group for firmware source access so we can start to understand the RU and CRU functions

Detector control system (DCS)

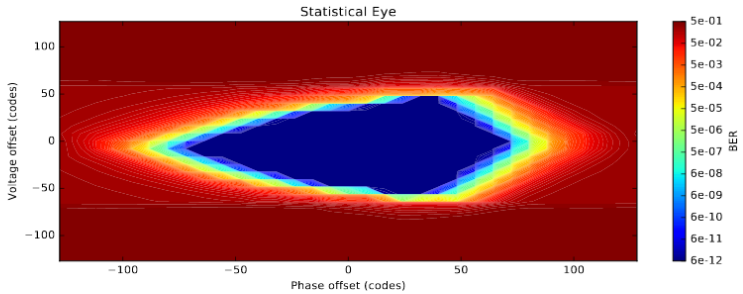
- FELIX should:
  - Monitor and configure the ALPIDE chips (through the RU)
  - Monitor and control the RU, and remotely program the RU firmware
  - Monitor and control the power boards (through the RU)
- Also: CAEN bulk power supplies, cooling system
- RU uses GBT-SCA chip for monitoring, control, and remote programming; FELIX has built-in support for communicating to GBT-SCA, we need to add specific RU support (some combination of firmware and software)
- CAEN power supplies are here

FireFly cable test w/ MOSAIC

- We need to know whether the readout will still work with possible changes to the stave readout (longer twinax cables, extension to the flex circuit)
- Key measure of performance is the “eye diagram” (see below, from CERN tests of IB HIC)
- MOSAIC developers at INFN gave us example code for running eye scans using the MOSAIC test system: this should work for us with minor changes
- We can also use an oscilloscope with high-speed differential probe: expected in the next week or two



(a) Scope measurement



(b) Statistical eye recorded with FPGA