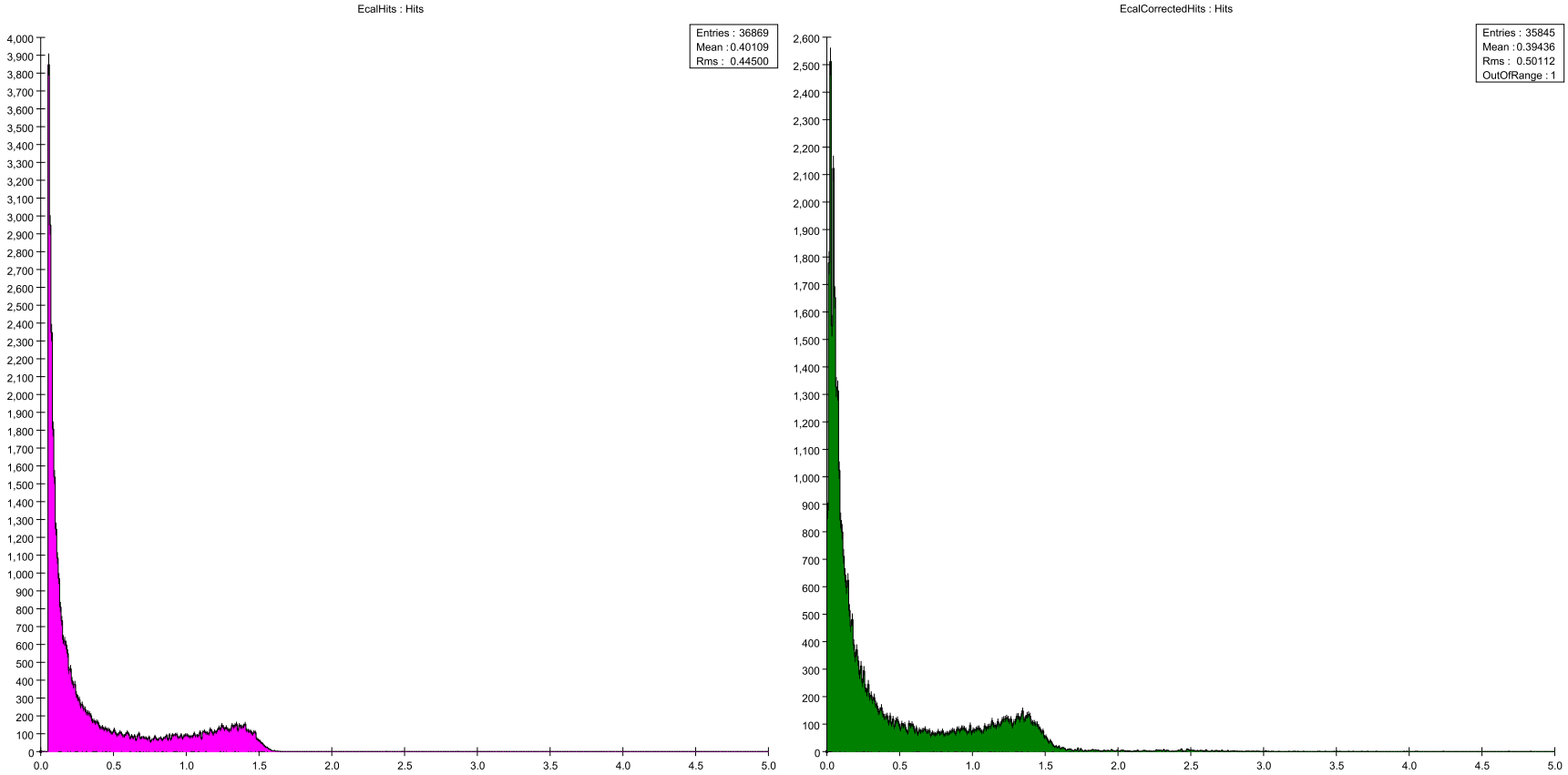
FADC operation

- Analog signal is sampled every 4 ns
- FADC starts a sum window when analog signal exceeds a set threshold, and stops summing when signal drops below threshold
- On 16-ns cycle, send sum (6 bits) and timestamp (2 bits indicating which 4-ns sample in the cycle started the sum window)
- Latest from JLab: there is some question about what the best values are for the cycle length and the number of bits for sum and timestamp; limiting factor is data rate (4 GBit/s or 8 GBit/s)

Implementation

- Ignore subtleties of cycle and timestamp — just read out on a 4-ns cycle for trigger studies
- Store calibration (pedestal and scale) in HPSEcalConverter; converts from RawCalorimeterHit to CalorimeterHit and vice versa
- Normalize the FADC energy sums so the integral over the pulse equals the hit energy

Test



- Beam background events: hit energy deposition on left, FADC energy sums on right
- Good correspondence at high E; effects at low E are dependent on FADC threshold (50 MeV for this test)

Next steps

- Clusterer accepts hits with adjacent hit times (i.e. within 8 ns of each other) — implement this in clusterer
- Finish up with the rest of the clusterer/trigger chain
- Use FADC crate sums for 1-bit trigger (latest 1-bit trigger rates on right — no upper discriminator, hot crystals removed, 5 ns trigger logic and 10 ns discriminator pulse width)