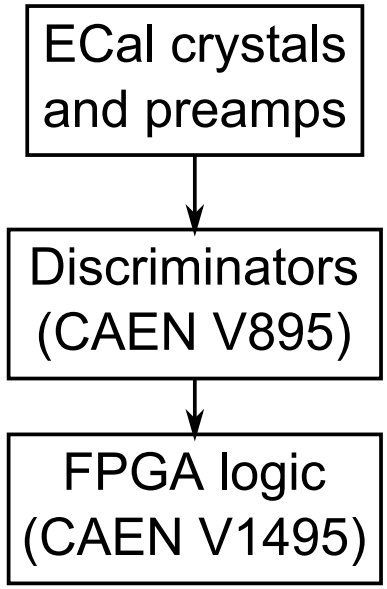
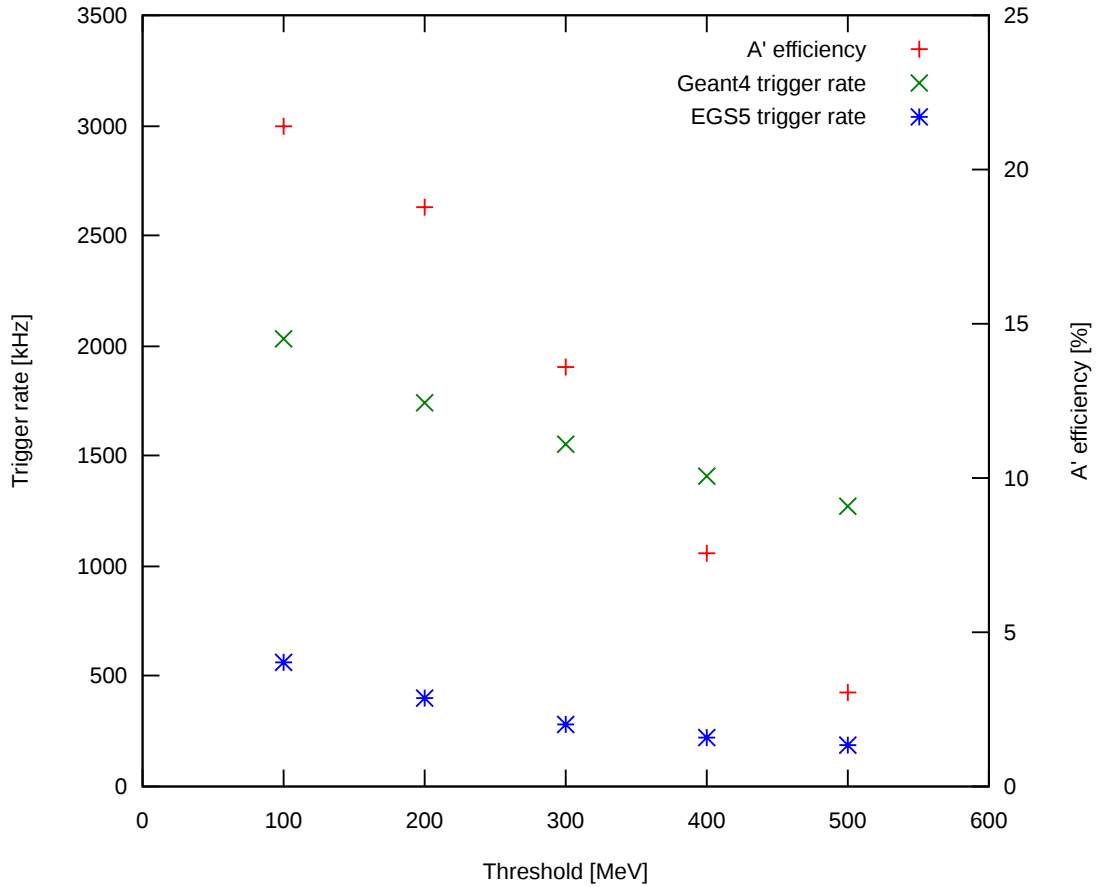
1-bit trigger simulation

- Simulation of 1-bit trigger rate on background is complete
  - Beam background only; trident background needs to be overlaid
  - A' efficiency neglects discriminator jitter
- Simulation parameters:
  - CR-RC shaper with $t_s = 18$ ns (update with better model once JLab has numerical data)
  - Retriggerable leading-edge discriminators, 32 ns output pulse width (actual value is 35)
  - Clusterer/trigger logic runs on 15 ns period
  - Require one hit-above-threshold to define a cluster
  - Require two clusters in opposite quadrants



1-bit trigger rates

- Target thickness $0.125\% X_0$
- A' mass 75 MeV

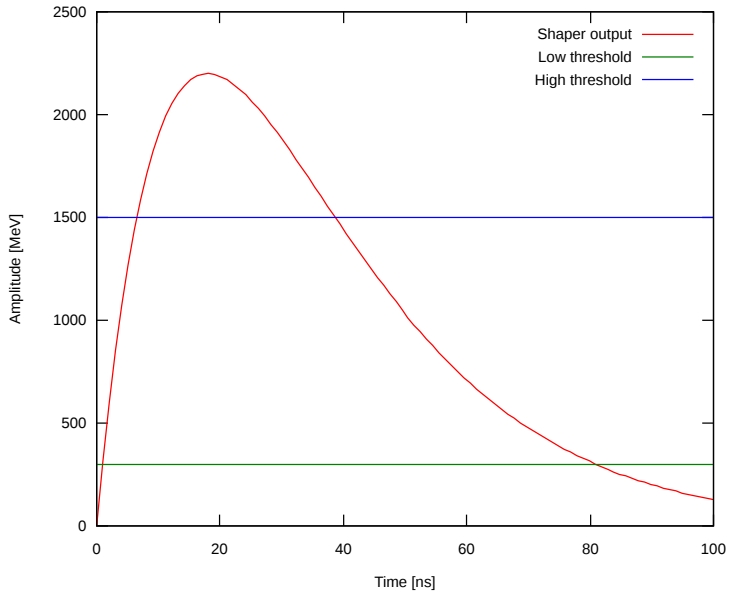


Approaches to reducing trigger rate

- Add upper discriminator
  - Is this practical?
- Adjust discriminator output pulse width (configurable 4-40 ns, currently 35 ns)
- Drop hot crystals from trigger logic
- Can we use energy in trigger decision? (does FPGA have analog inputs?)
  - Note: we already assume we can implement an opposite-quadrants requirement, presumably in MTrigger

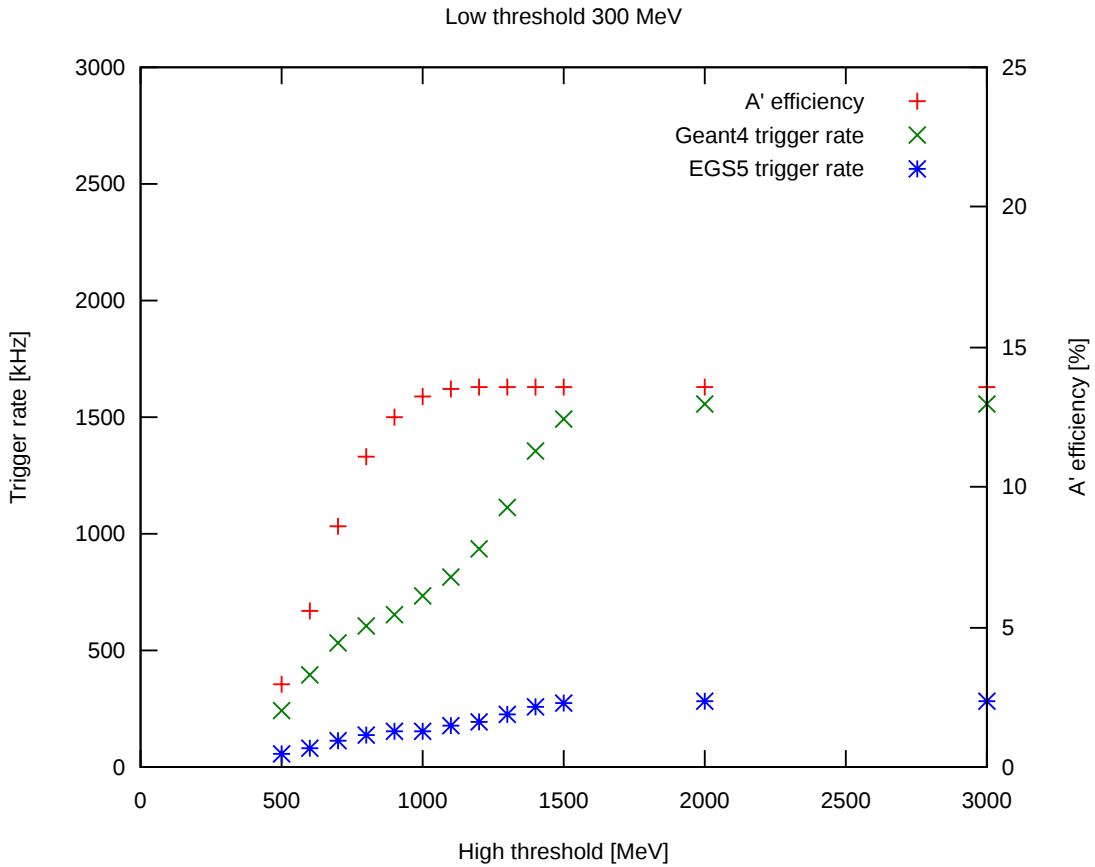
2-bit trigger

- Each crystal is read by two discriminators
- Upper discriminator is a veto
- Example: 2.2 GeV hit; thresholds at 300 MeV and 1500 MeV
  - Lower discriminator fires at $t_0 + 0.95$ ns
  - Upper discriminator fires at $t_0 + 6.46$ ns
  - Result: output to trigger logic is 6.5 ns wide instead of 35 ns



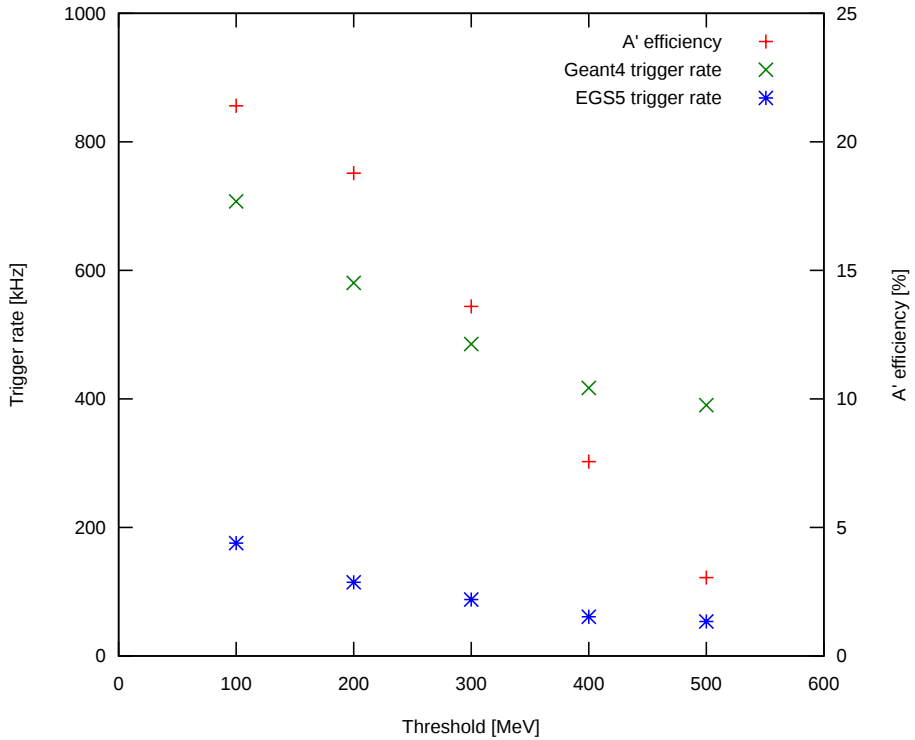
2-bit trigger rates

- A' efficiency is unaffected by upper threshold $>$ 1.1 GeV (the maximum energy for the e^+e^-)
- Background trigger rates start to drop around 1.5 GeV — not sure why
- ”Sweet spot” seems to be 1 GeV (this is true regardless of lower threshold value)
- Background trigger rate reduction: factor of 2-3



Discriminator output width

- Shortening discriminator output pulse reduces trigger rate
- Trigger is a two-hit coincidence, so trigger rate grows faster than linearly as a function of pulse width
- Halving pulse width reduces background triggers by a factor of 3
- A' efficiency will be hurt by pulse width less than 15 ns (more, allowing for jitter) — this is not yet in simulation



Results

- With both of these changes (lower threshold 300 MeV, higher threshold 1000 MeV, pulse width 15 ns):
  - A' efficiency 13.3%
  - Background rate (assuming Geant4) 268 kHz
  - Background rate (assuming EGS5) 50 kHz
- Removing hot crystals from trigger logic should get these rates down to usable levels