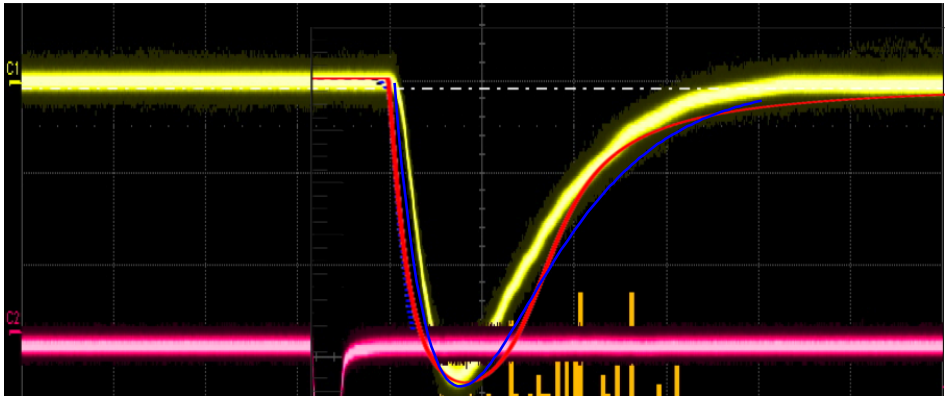
ECal readout/reconstruction

- SLIC simulates showers and energy deposition
- For trigger studies, need to simulate readout and trigger in LCSim
- Readout:
  - Effect of ECal preamp pulse shaping is significant
- Trigger:
  - FADC-based trigger
  - 1-bit trigger

Pulse shape



- For now, fitting with $(t/T_0)e^{1-t/T_0}$, with $T_0 = 18$ ns (blue curve)
  - Red curve is $\tan^{-1}$-based fit developed at JLab
  - A better fit than either of these might be a CR-RC shaper with different time constants for the integrator and differentiator
- Pulses from beam background hits stay above A' thresholds for a long time
  - 1-bit trigger is unaffected because it uses leading edge discriminators (fixed output pulse width)
  - May affect FADC trigger

1-bit trigger

- Trigger design document is on Confluence page for this meeting
- Trigger parameters:
  - Crystal preamp signals go to leading edge discriminators
  - Require 1 (or more) hit in a 3x3 block for a cluster
  - Trigger on clusters in opposite quadrants
  - Trigger runs every 15 ns (simulation currently uses 16 ns)

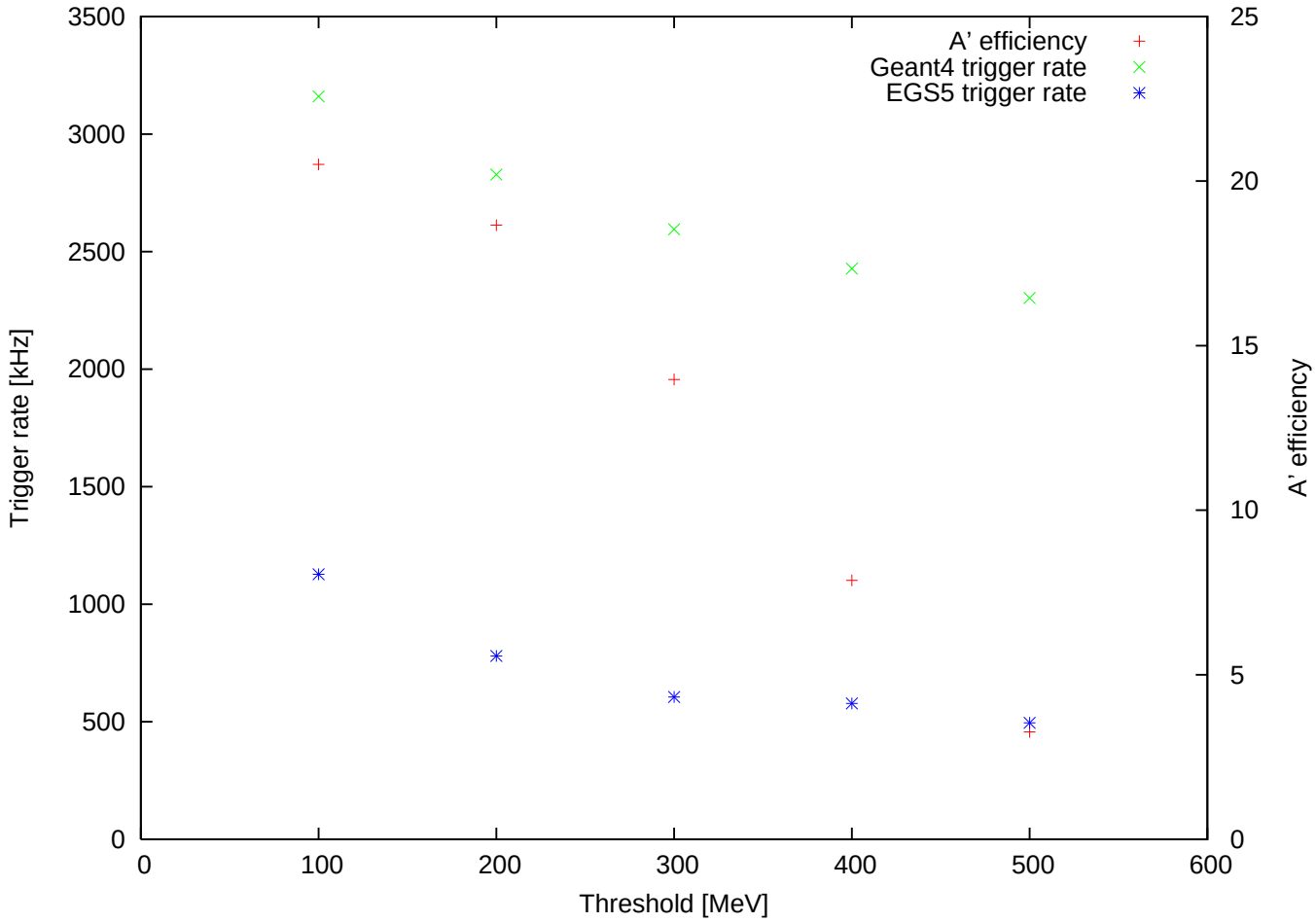
LCSim structure

- Readout driver: reads energy deposition (from SLIC), makes hits (for clusterer)
  - HPSEcalSimpleReadoutDriver: sums energy depositions in readout window
    - ★ Equivalent to previous trigger studies
  - HPSEcalTimeEvolutionReadoutDriver: simulates pulse shape and samples it at the readout period
    - ★ For FADC readout and trigger
  - HPSEcalDiscriminatorReadoutDriver: simulates pulse shape and leading edge discriminator at the beam period; samples discriminator output at the readout period
    - ★ For 1-bit trigger
- Clusterer driver: reads hits (from readout driver), makes clusters
  - HPSEcalClusterer: FADC clusterer
  - HPSEcal1BitClusterer: 1-bit clusterer

Other software

- HPSClockDriver maintains a clock based on the beam period; can be accessed by other drivers
- For now, trigger is part of HPSPlotsDriver, which plots hit and cluster statistics

1-bit trigger rates



Explaining these results

- Background trigger rates are about 10 times higher than those presented by Takashi on 8/23
  - 16 ns window vs. 8 ns window: factor of 2
  - Discriminator output pulse (32 ns) is double the window: factor of 3
    - ★ Discriminator output is “ON” for two consecutive trigger cycles, so the two opposite-quadrant hits needed for a trigger can be offset by one trigger period in either direction
  - Pulse pileup: 50% increase (depending on threshold)

Next steps

- Ways to improve 1-bit trigger:
  - Change thresholds/turn off hot crystals
  - Add upper discriminator (window)
  - Shorten discriminator output pulse
- Other to do:
  - Investigate effect of pileup on A' acceptance
  - Change 1-bit trigger period to 15 ns from 16 ns
  - Implement and test FADC trigger