PACIFICr5 - 64 channels SiPM readout ASIC for the SciFi Tracker detector

Data Sheet PACIFICr5

FEATURES

64 channels.
Current mode input.
Low input impedance (≈50Ω).
Zero components interface between sensor and device.
High Bandwidth preamplifier (≈250MHz).
Relative linearity error ±5%.
Adjustable input node DC voltage.
Low Power consumption (<12mW/channel).
Channel-to-channel Offset correction control.

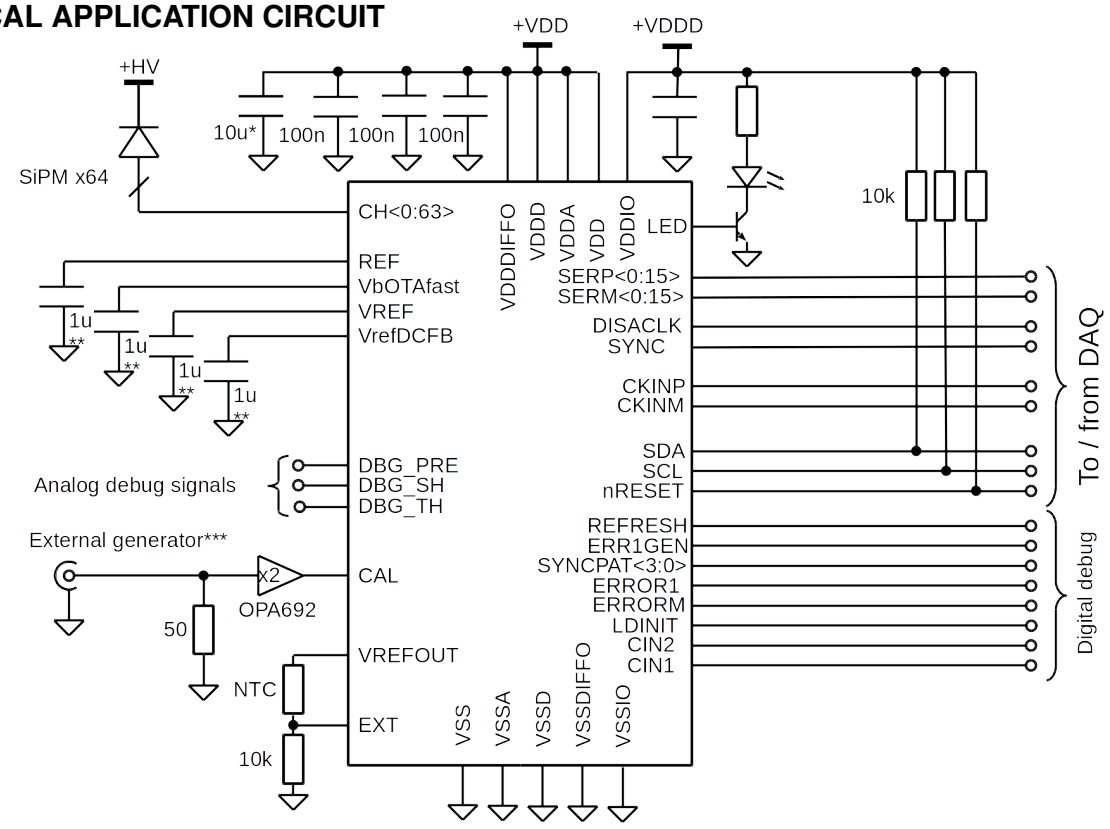
APPLICATION

Readout of Silicon Photo Multipliers arrays.

DESCRIPTION

PACIFICr5 is an 64 channel Silicon Photo Multiplier readout circuit with current mode input and digital output developed using TSMC 0.13μm process.
PACIFICr5 is available without package and will need of wire bonding. A BGA packaged version will be available for easily testing and handling of the devices.

TYPICAL APPLICATION CIRCUIT



*Due to high current transients for input signals in the range of mA, a 10uF capacitor should be placed close to every power pin.
**Filtering for internal reference voltages, needed only to improve noise.
***Circuitry needed for external signal injection to the channels, only needed for debug.

Figure 1: Typical application schematic

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REVISION HISTORY

03/17 - *Albert Comerma* - First version
05/17 - *Jose Mazorra* - Updated registers and descritpiton

FUNCTIONAL BLOCK DIAGRAM

The analog processing chain used for the Scintillating Fibre Tracker detector at LHCb has been split in different blocks to fit the requirements. The channel block diagram depicted in figure 2 includes:

- **Pre-amplifier:** it includes the current mode input stage already tested in the previous versions of the ASIC. It has a double feedback loop that sets the desired DC voltage at the input node and keeps at the same time a low input impedance over a broad bandwidth. The output structure has been modified to allow the selection over four different output gains. The current signal is then converted to voltage by means of a transimpedance amplifier (TIA). With respect to previous version, a filter has been added to avoid reaching the maximum slew rate of the TIA.
- **Shaper:** it has the function to reduce the peak duration of the signal to integrate as much signal as possible in the minimum time. For that purpose, it reduces the tail produced by the sensor. It must be configurable to cope with the large difference in signal shape from the different manufacturer devices. From the previous version, the shaping time has been changed to fit last SiPM version.
- **Integrator:** it is formed by two interleaved gated integrators switching at half the system clock frequency (20MHz). This structure allows to reduce the dead time almost to zero.
- **Offset trim:** a configurable block with trimming DACs allows to individually fine tune the DC voltage of each integrator (2 per channel). It is based on a current DAC with some mirrors and pass gates to change in both directions (up and down from usual value).
- **Track and Hold:** two single ended track and hold circuits based on gated capacitors are used to mix the two signals and keep the output stable between clock edges.
- **Digitization:** the conversion from analog to digital is based on three comparators with configurable thresholds. This scheme allows a non linear conversion adjusted to the desired operating conditions and range.

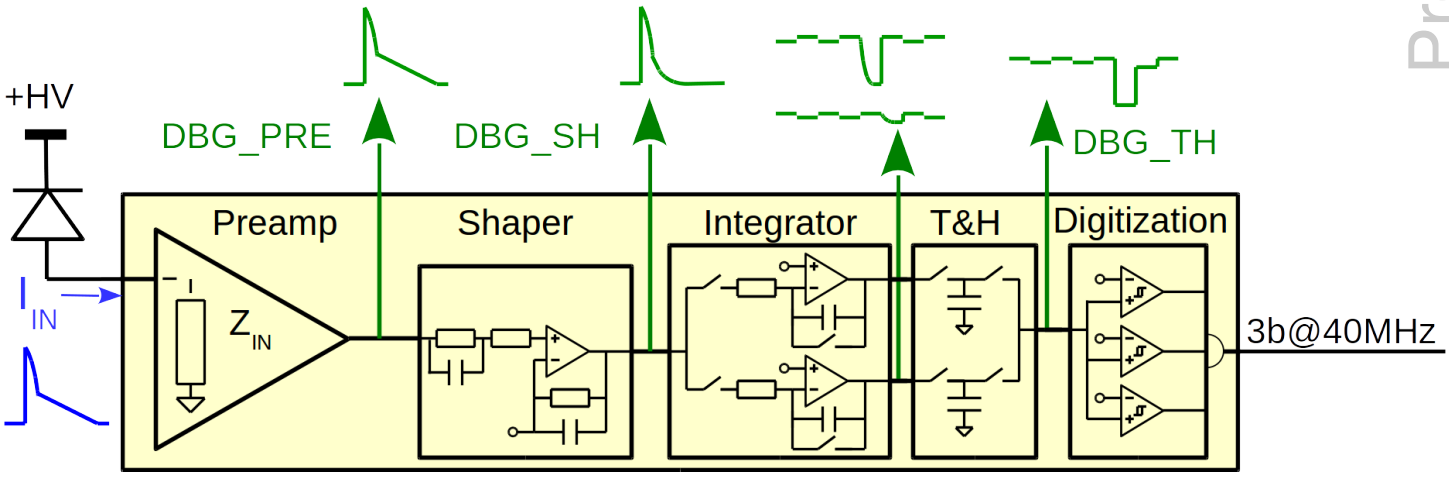

Figure 2: PACIFICr5 Channel block diagram

Some other blocks are also included to set the correct operation points of the circuit and configure tunable parameters. This blocks are a common biasing block controlled by a digital slow control block. This slow control is based on I^2C standard. At the output of every four channels, an encoder and serialization block is also included. It generates a bit stream at 320MHz, encoding the three outputs of each channel comparators in two bits and concatenating the encoded output of the four channels.

SPECIFICATIONS

T_A=25°C, VDDA = VDD = VDDD = VDDDIFFO = 1.2V , VDDIO = 1.5V

Parameter	Conditions	Min	Typ	Max	Unit
INPUT					
Z_{in}	Default input stage polarization currents	-	44	-	Ω
Bandwidth	15pF input capacitance (min) and 5pF (max)	340	-	540	MHz
DC adjustable at input		0.2	-	0.75	V
POWER CONSUMPTION					
I_{VDD}	1.2V	-	190	-	mA
I_{VDDA}	1.2V	-	200	-	mA
I_{VDDD}	1.2V	-	100	-	mA
$I_{VDDDIFFIO}$	1.2V	-	60	-	mA
I_{VDDIO}	1.5V	-	1	-	mA
DYNAMIC RANGE					
Input range	Gain = 0		-		pC
Input range	Gain = 1		-		pC
Input range	Gain = 2		-		pC
Input range	Gain = 3		-		pC
REFERENCE VOLTAGE					
VREF	Default values	-	500	-	mV
NOISE	Integrated rms noise from 10Hz to 300MHz	-		-	μA
DIGITAL SIGNALS					
Clock frequency		-	320	-	MHz
I^2C Clock frequency(internal)		-	40	-	MHz

Table 1: Specifications summary

PINS CONFIGURATION AND DESCRIPTION

PACIFICr5 is provided in two different formats: on die without packaging and packaged in a BGA format (12x12mm, 196 pins, 0.8mm pitch). In figures 3 and 4 both formats can be seen with the corresponding pin numbers. Numbering is from left to right and from top to bottom, looking die or package from top.

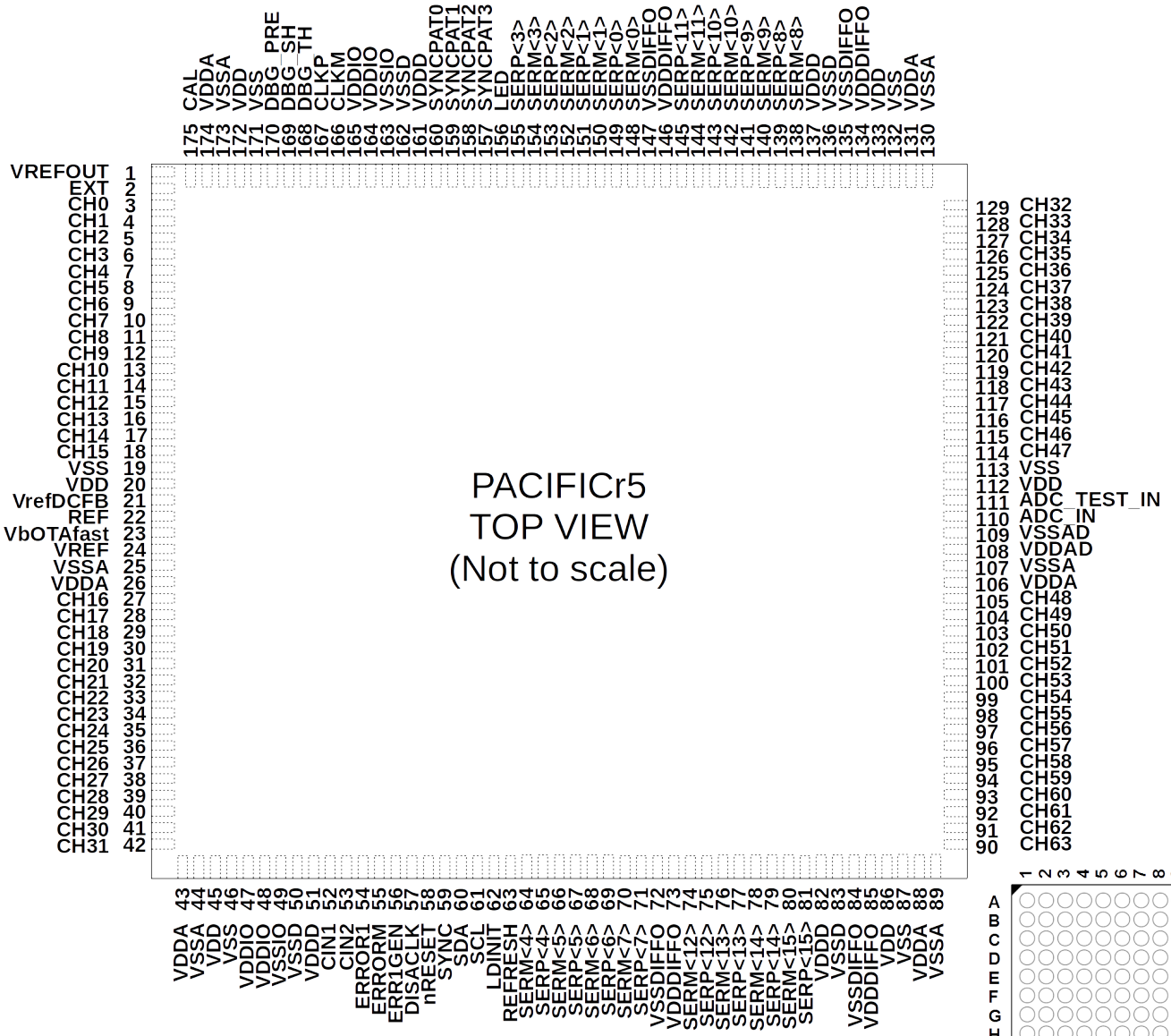

Figure 3: Die pin configuration (Top view)

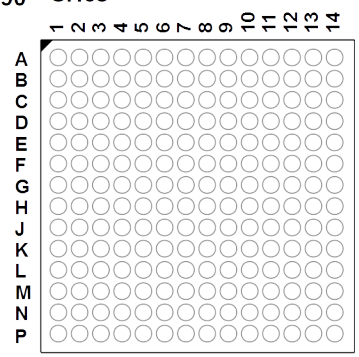

Figure 4: BGA package (Top view)

Several types of pins result from the pad ring. Most of them are analog input and digital output pairs. Additionally, some digital inputs and outputs are used for controlling the slow control interface and debug functions. Finally, several power pads are also needed due to the different power domains and voltages (core and pad digital buffers).

In tables 2, 3 and 4 a summary of the pinout is presented with its functionality. The correspondence between packaged (BGA) and die version is also included.

Table 2: Signals pinout

Die Pin	BGA	Pin Name	Die Pin	BGA	Pin Name	Die Pin	BGA	Pin Name
1	C3	VREFOUT	2	D3	EXT	3	A1	CH0
4	A2	CH1	5	B1	CH2	6	B2	CH3
7	C1	CH4	8	C2	CH5	9	D1	CH6
10		CH7	11	E2	CH8	12	E3	CH9
13		CH10	14	F2	CH11	15	G1	CH12
16		CH13	17	H1	CH14	18	H2	CH15
27		CH16	28	J2	CH17	29	K1	CH18
30		CH19	31	K3	CH20	32	L1	CH21
33		CH22	34	L3	CH23	35	M1	CH24
36		CH25	37	N1	CH26	38	N2	CH27
39		CH28	40	P2	CH29	41	A14	CH30
42		CH31	129	B14	CH32	128	B13	CH33
127		CH34	126	C13	CH35	125	D14	CH36
124		CH37	123	D12	CH38	122	E14	CH39
121		CH40	120	E12	CH41	119	F14	CH42
118		CH43	117	G14	CH44	116	G13	CH45
115		CH46	114	H13	CH47	105	J14	CH48
104		CH49	103		CH50	102		CH51
101	K14	CH52	100	K13	CH53	99		CH54
98		CH55	97	L14	CH56	96	L13	CH57
95		CH58	94	M14	CH59	93	M13	CH60
92		CH61	91	N13	CH62	90	P14	CH63
148		SERM0	149	B11	SERP0	150	A11	SERM1
151		SERP1	152	A12	SERM2	153	B9	SERP2
154		SERM3	155	B10	SERP3	64	A10	SERM4
65	B7	SERP4	66	A7	SERM5	67	B8	SERP5
68	A8	SERM6	69	B5	SERP6	70	A5	SERM7
71	B6	SERP7	138	A6	SERM8	139	P9	SERP8
140	P10	SERM9	141	P11	SERP9	142	P12	SERM10
143	P7	SERP10	144	N7	SERM11	145	P8	SERP11
74	N8	SERM12	75	P5	SERP12	76	N5	SERM13
77	P6	SERP13	78	N6	SERM14	79	P3	SERP14
80	N3	SERM15	81	P4	SERP15	21	J3	VrefDCFB
22	F3	REF	23	G3	VbOTAfast	24	H3	VREF
52	M3	CIN1	53	M4	CIN2	54	M4	ERROR1
55	M5	ERRORM	56	M6	ERR1GEN	57	M7	DISACLK
58	L7	nRESET	59	M8	SYNC	60	M9	SDA
61	N9	SCL	62	M10	LDINIT	63	N10	REFRESH
110	M11	ADC_IN	111	N11	ADC_TEST_IN	156	M12	LED
157	C11	SYNCPAT3	158	C10	SYNCPAT2	159	C9	SYNCPAT1
160	C8	SYNCPAT0	166	A4	CLKM	167	A3	CLKP
168	C5	DBG_TH	169	C4	DBG_SH	170	B4	DBG_PRE
175	B3	CAL						

Die Pins	BGA Pins	Power supply name
26, 43, 88, 106, 131, 174	E4, F4, G4, H4, J4, K4, D11, E11, F11, G11, H11, J11, K11, L11	VDDA
25, 44, 89, 107, 130, 173	E6, F6, G6, H6, J6, K6[1]	VSSA
20, 45, 86, 112, 133, 172	E5, F5, G5, H5, J5, K5, E10, F10, G10, H10, J10, K10	VDD
19, 46, 87, 113, 132, 171	E7, F7, G7, H7, J7, K7[1]	VSS
51, 82, 137, 161	D6, D8, D9, D10, L6, L8, L9, L10	VDDD
50, 83, 136, 162	E8, F8, G8, H8, J8, K8[1]	VSSD
47, 48, 164, 165,	D4, D5, L4, L5	VDDIO
49, 163	E9, F9, G9, H9, J9, K9[1]	VSSIO
73, 85, 134, 146		VDDDIFFO
72, 84, 135, 147[1]		VSSDDIFFO
108		VDDAD
109[1]		VSSAD

[1] All VSSA, VSS, VSSD, VSSAD, VSSIO and VSSDDIFFO are connected to a common VSS plane on BGA adapter.

Table 3: Power supply pins

Table 4: Pins function description

Pin name	Bus length	Type	Description
CH[0:64]	64	Analog in	SiPM anode connection for input signal. Directly to channel input, no components are needed for connection.
SERP[0:15], SERM[0:15]	32	SLVS out	Digital output serialized at 320MHz using custom driver. It includes 2 bits from four consecutive channels (in total 8 bits encoding the output of the 3 discriminators per channel).
VrefDCFB	-	Analog out	Reference voltage for slow feedback loop amplifier, to be decoupled with external capacitor.
VREFOUT	-	Analog out	Voltge reference, after DAC and derived from Bandgap Reference. It should be 2*VREF.
VREF	-	Analog out	Voltge reference used for common bias, after DAC and derived from Bandgap Reference. It should be set around 0.5V.
VbOTAfast	-	Analog out	Bias reference used for internal amplifiers, to be decoupled with external capacitor.
REF	-	Analog out	Voltage reference derived from voltage divider used in anode voltage control, to be decoupled with external capacitor.
DBG_PRE	-	Analog out	Pre-amplifier analog debug signal (internally multiplexed).
DBG_SH	-	Analog out	Shaper analog debug signal (internally multiplexed).

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Table 4 – continued from previous page

Pin name	Bus length	Type	Description
DBG_TH	-	Analog out	Integrator (after T&H) analog debug signal (internally multiplexed).
CAL	-	Analog in	Signal to inject an external current/waveform to any channel (internally multiplexed).
CIN1, CIN2	-	Digital in	Trigger for internal charge injection start.
ADC_IN	-	Analog out	Input signal comming into the ADC.
ADC_TEST_IN	-	Analog in	External input to the ADC.
EXT	-	Analog in	External input to the ADC.
nRESET	-	Digital in	General digital reset.
DISACLK	-	Digital in	Disable of I^2C clock (to avoid noise on analog).
SYNC	-	Digital in	Reset for clock divider to generate integration clock (20MHz) from main system clock (320MHz).
SDA	-	Digital in/out	Slow control Data line.
SCL	-	Digital in	Slow control Clock line.
LDINIT	-	Digital in	Forces configuration registers to load the initial values hardcoded in the slow control logic.
REFRESH	-	Digital in	Refresh from error flags.
ERR1GEN	-	Digital in	Pin to force error on digital memory (for debugging purposes).
SYNPAT[3:0]	2	Digital in	External injection of data to the serial links. The data is directly feed to the serializer when internal synMode signal is enabled.
ERROR1	-	Digital out	Indicator for single bit fips detected by the Hamming code in the configuration registers.
ERRORM	-	Digital out	Indicator for multiple bit fips detected by the Hamming code in the configuration registers.
LED	-	Digital out	Bit controlled by internal register.
CLKM, CLKP	-	SLVS in	Differential input of main clock (320MHz).
VDDA, VSSA	-	Power	Pre-amplifier, shaper and common bias power supply. 1.2V.
VDD, VSS	-	Power	Integrator, Trimming, Track and Hold and analog buffers power supply. 1.2V.
VDDD, VSSD	-	Power	Standard cells digital power supply. 1.2V.
VDDDIFFO, VSSDIFFO	-	Power	SLVS output buffers power supply. 1.2V.
VDDIO, VSSIO	-	Power	Digital PAD ring IO voltage. 1.5V.
VDDAD, VSSAD	-	Power	Integrated ADC power supply. 1.2V.

Table 4: Pins function description

FEATURES

Several features and blocks have been added to the design in order to cope with the different input signals and to allow an easier testing and debugging of the different features.

In order to debug the different analog blocks of the processing chain, several features and extra pins have been added. On the digital side, also a few operation modes and extra pins have been added to perform different checks.

DC INPUT VOLTAGE SELECTION

Even if high overvoltage operated SiPM array does not show an important dispersion of gain from channel to channel, the anode voltage can be fine tuned using the configuration registers of PACIFIC. To avoid voltage dispersion between channels and to reduce lines and power consumption, a single common reference (with 16 values) is shared for all channels. The voltage is derived from the Bandgap reference voltage (multiplied a factor 2) and then divided by equal resistors (see figure 5), giving around 50mV steps.

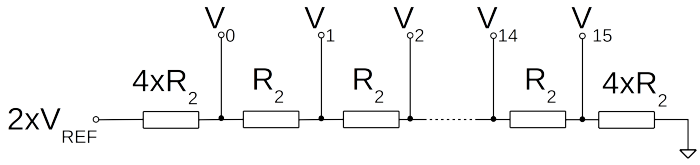

Figure 5: Anode voltage generation

Each channel can be independently connected to any of these references using the variable D_OFF_MUX_* (4 bits) from the channel configuration registers. The four digital signals are delivered to the channel, where a decoder generates the corresponding enable signal to the 16 pass gates that implement the connection.

THRESHOLDS AND VrefDCFB

VrefDCFB is a voltage reference used in all the analog processing chain to keep a constant DC value at the output of the different blocks. For this reason the resulting thresholds must be evaluated with respect to this voltage. Since the gated integrator uses an inverting structure the output signal should be smaller than this voltage.

The threshold generation has been completely modified from the previous version. The thresholds are generated independently of VrefDCFB by injecting the output of the current DACs into a $\approx$50k Ω resistor. The granularity of the current DACs has been increased to 8 bits, providing a voltage range between ground and 760mV. As a consequence, VrefDCFB cannot be set to values above 700mV without affecting the operation of the circuit.

In this version, the threshold generation structure has been instantiated only once in the common biasing block, instead of three. Additionally, a copy of this structure has been placed in every channel, allowing to define specific thresholds for each channel. The flag D_SELVTH_* from the channel configuration register controls the selection between the common and local thresholds at a channel level.

ANALOG DEBUG

The analog signal from the critical points of the processing chain are available through the DBG_PRE, DBG_SH and DBG_TH pins (as seen in figure 2). The flag DBG_EN_OUT from the debug configuration registers must be set to enable this analog readout. Alternatively, when the flag DBG_EN_OUT is not set these output give access to the channel local thresholds.

In order to avoid using a large amount of pads, this outputs are multiplexed in a single output for the whole 64 channels. The channel connected to this debug output is controlled by the variable DBG_MUX (5 bits) from the debug configuration registers, accessible through the slow control interface. The debug features require an additional decoder, included in the slow interface logic.

The output can be connected directly to a high input impedance test probe (1MΩ). The output buffers do not feature enough slew rate to drive directly low impedance (50Ω). If needed, external amplifier can be used for this purpose (OPA692 is recommended).

CALIBRATION ADC

In order to simplify the characterization of the different DACs in the ASIC, a 10 bit ADC has been integrated in the chip. It operates with a 6.67MHz clock generated by the slow control logic. It also uses an specific 1.2V power supply, independent from the power supplies of the rest of the chip.

The input to the ADC is multiplexed, selecting the desired signal by setting the corresponding value in the variable DBG_ADC_ADDR (4 bits) of the debug configuration registers:

- (0:2): Common threshold voltages.
- (3:5): Local channel threshold voltages, where the channel is selected with the the variable DBG_MUX (5 bits) from the debug configuration registers.
- (6): Common bias voltage reference VREF.
- (7): Bandgap voltage.
- (8): Temperature sensor output voltage.
- (9): Channel voltage reference VrefDCFB.
- (10:13): Several steps of the input voltage selection circuit REF[15,12,9,6].
- (14): External input EXT.

- (15): External input ADC_TEST_IN.

The selected input signal of the ADC can be readout through the dedicated pin ADC_IN after being buffered.

An extra 1V reference output derived from VREF can be used for powering external circuits and is available at VREFOUT pin.

The conversion process is triggered by setting the flag DBG_ADC_START from the debug configuration registers. When the conversion is completed, the slow control logic stores the result in the lower bits of the variable DBG_ADC_Out (16 bit). The rest of the bits are fixed at '0' except the MSB, which is used to indicate the completion of the conversion (EOC).

CALIBRATION INPUT

A single calibration input allows to inject electrical signal to the desired channel for characterization. This calibration input (see figure 6) consists on a pass gate followed by a ≈100 Ω resistor (to convert external voltage signal to current) in series to the input. The connection is in parallel to the sensor input to avoid affecting this signal. This feature can be enabled by setting the flag DBG_EN_IN from the debug configurations registers. Additionally, the flag DBG_Cin must be not set to select this charge injection option instead of the internal injection system presented in the next section. The pass gate of each channel can be independently selected by using the variable DBG_CH from the debug configuration registers. Based on these three configuration variables, a decoder placed in the slow control logic generates the signal CAL_{CH} that appears in figure 7.

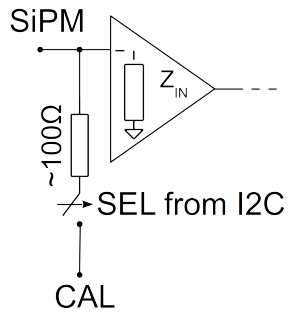

Figure 6: Calibration input

CHARGE INJECTION

Similar to the calibration input, a charge injection structure has been inserted in the channel for characterization.

This structure charges two small on channel capacitors, while CIN1 and CIN2 are in the '0' state, and discharges them to the input stage when a rising edge arrives. To fully discharge the signal they must be kept during at least 4*RC time. Depending on CIN1 and CIN2 control, three different values of charge can be injected.

To avoid interfering with the normal input signal, this feature can be enabled by setting the flag DBG_EN_IN from the debug configurations registers. Additionally, the flag DBG_Cin must be set to select this charge injection option instead of the external calibration input presented in the previous section. The pass gate of each channel can be independently selected by using the variable DBG_CH from the debug configuration registers. Based on these three configuration variables, a decoder placed in the slow control logic generates the signal CIN_{CH} that appears in figure 7. The slow control logic ensures that CIN_{CH} and CAL_{CH} never collide.

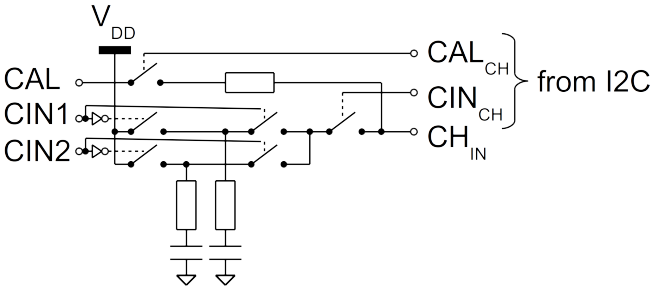

Figure 7: Charge injection and calibration schematics

Simulation with relatively small capacitors (630fF and 1pF) and relatively large resistor in series (12 kΩ and 9 kΩ respectively) to mimic SiPM tail shows a reasonable output.

Using the slow control, any combination of channels can be selected to use this charge injection, what should allow a much faster but less fine characterization of the whole prototype, compared to the calibration input.

OFFSET COMPENSATION

MonteCarlo simulations with the full channel presents a problem in the offset level at the output of the integrators. First problem is the channel to channel variation and a second one is the intra-channel (integrator to integrator) variation. According to simulations, few of the channels are expected to have a variation higher than 1/4phe leading to problematic setting of the thresholds for measurements.

The closed loop DC correction mechanism, which automatically corrected the channel to channel variations, has been deprecated. On the other hand, the sub-channel offset trimming has been moved to the positive input of the integrator, where VrefDCFB was previously set. The trimming is based on a current output DAC and some mirrors that can feed current in both direction, leading to positive or negative movement of the reference voltage of the integrator. In figure 8 the schematic of

the block can be observed. The control lines are reduced to 4 bits for the current setting and 1 bit of sign.

With this configuration, the channel to channel dispersion of the offset level can be corrected using the offset trimming, by shifting the baseline of both integrators in parallel, or by adjusting the channel specific threshold to compensate this spread. The intra-channel variation can still be corrected with the offset trimming as in previous versions.

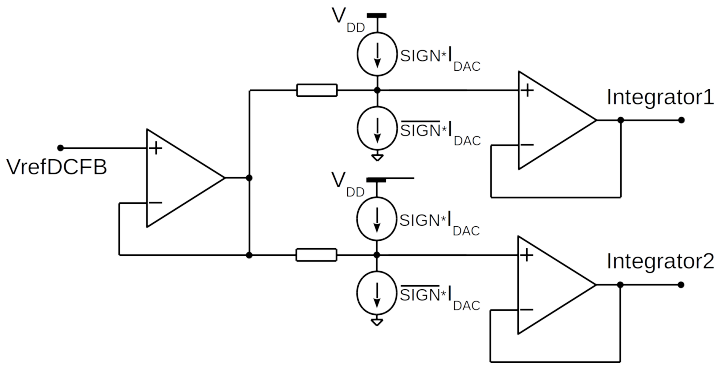

Figure 8: Sub-channel DC level trimming

POWER ON RESET

Previous prototype revealed a random startup of registers value after power is applied, leading to some high current consumption during the time between powering and generating correct initialization sequence via control signals. To avoid this condition a Power On Reset (POR) circuit has been added. The function of this circuit is to generate a clean startup pulse to set all registers to the default value.

This block has been connected to the digital power supply (V_{DDD}) since it will interact with the slow control registres. A schematic of the POR circuit can be seen in figure 9.

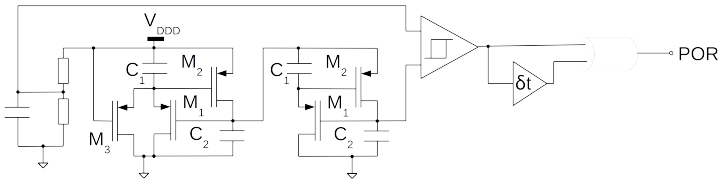

Figure 9: Power on Reset circuit

Since rising time of power supply is not predictable and should take some μs, an initial block generates a controlled slope of the power supply. This signal is introduced to an inverter and then delayed using several inverters. The output of the first inverter is fed into an XOR together with the delayed output, generating a short digital pulse.

DIGITAL FEATURES & DEBUG

On the digital side, three different check structures have been added;

- **Hamming encoding**: All the registered memory bits that hold the configuration are checked by a Hamming encoding algorithm. The registers have a length of 8 bits and are composed of two equal blocks. Each block implements a Hamming(7,4) code with an additionally parity bit, requiring 4 parity bits to protect 4 data bits. In this way, if an error occurs (due to Single Event Upset) it can be detected, discriminating whether a single bit or several bits flipped, and corrected on the fly in the case of a single bit flip.

  To signal the errors two signals are generated;

  – ERROR1: Indicates a single error in the register.

  – ERRORM: Indicates multiple errors.

  Once a single error is detected, a high level in the REFRESH signal is needed to clear the error signal. Internally, the signal is corrected by the logic inside the register blocks. In case of multiple errors, the configuration registers must be rewritten to correct the error and clear the error signal. Internally, ERROR counters are present to count the number of errors, one 8 bits counter for single errors (one bit) and a second 8 bits counter for the multiple errors. The counter is driven by the state of the error signals of all the registers, being automatically written when any of these signals changes its state. Consequently, the single error counter is cleared by the REFRESH signal and the multiple error counter is cleared when the registers are rewritten.
  ERROR1GEN signal is designed to test the functionality of the Hamming encoding error detection and correction, by setting the LSB of all register blocks and forcing single errors in the memory.

- **SYNPAT**: an external digital pattern can be introduced in the serializer block to test the serialization and digital link. This pattern can be generated externally at 40MHz and used in all the channels. This test mode and the corresponding inputs are selected with the flag synMode in the debug configuration registers.

- **LED**: there is a flag in the debug configuration register reserved to control a digital output that should be connected to a LED on the PCB to allow the verification of the slow control.

SLOW CONTROL INTERFACE

Slow control is based on standard 10bit addressing I^{2}C. The basic write transmission frame can be observed in figure 10. Auto-increment of address is performed internally to allow more than one consecutive register read or write without repeating the preamble (first 2 bytes).

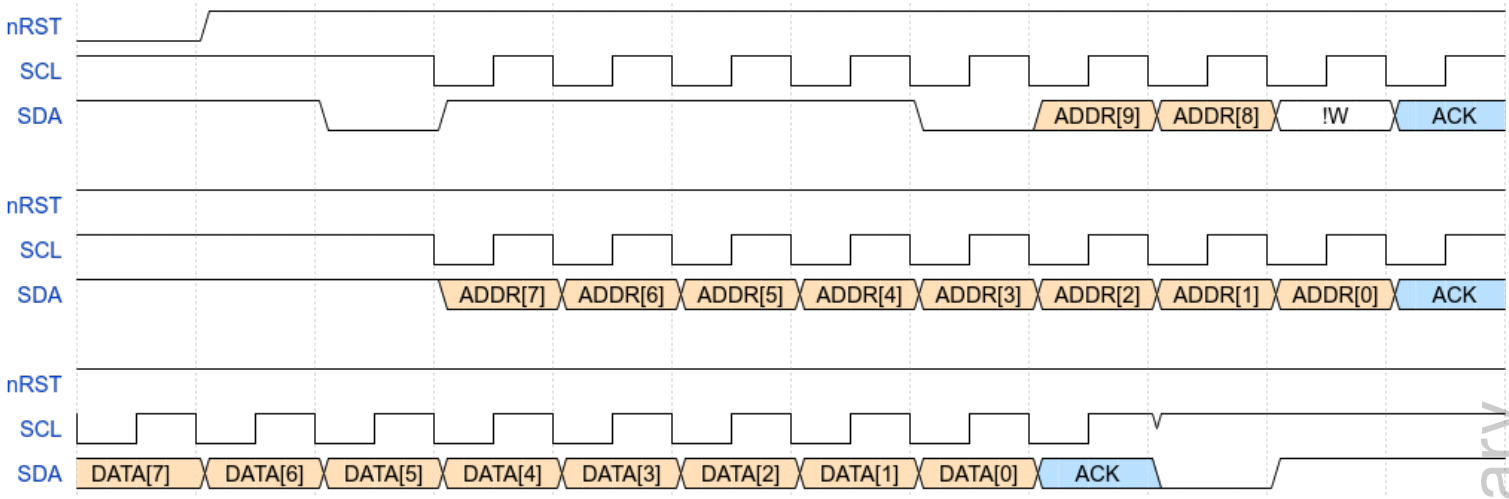

Figure 10: PACIFICr3 Write example sequence

In the case of a read operation a repeated start must be provided after first byte transmission to start the read process, as seen in figure 11. It introduces the need of an extra byte in the preamble. During read data the nACK must be provided by master.

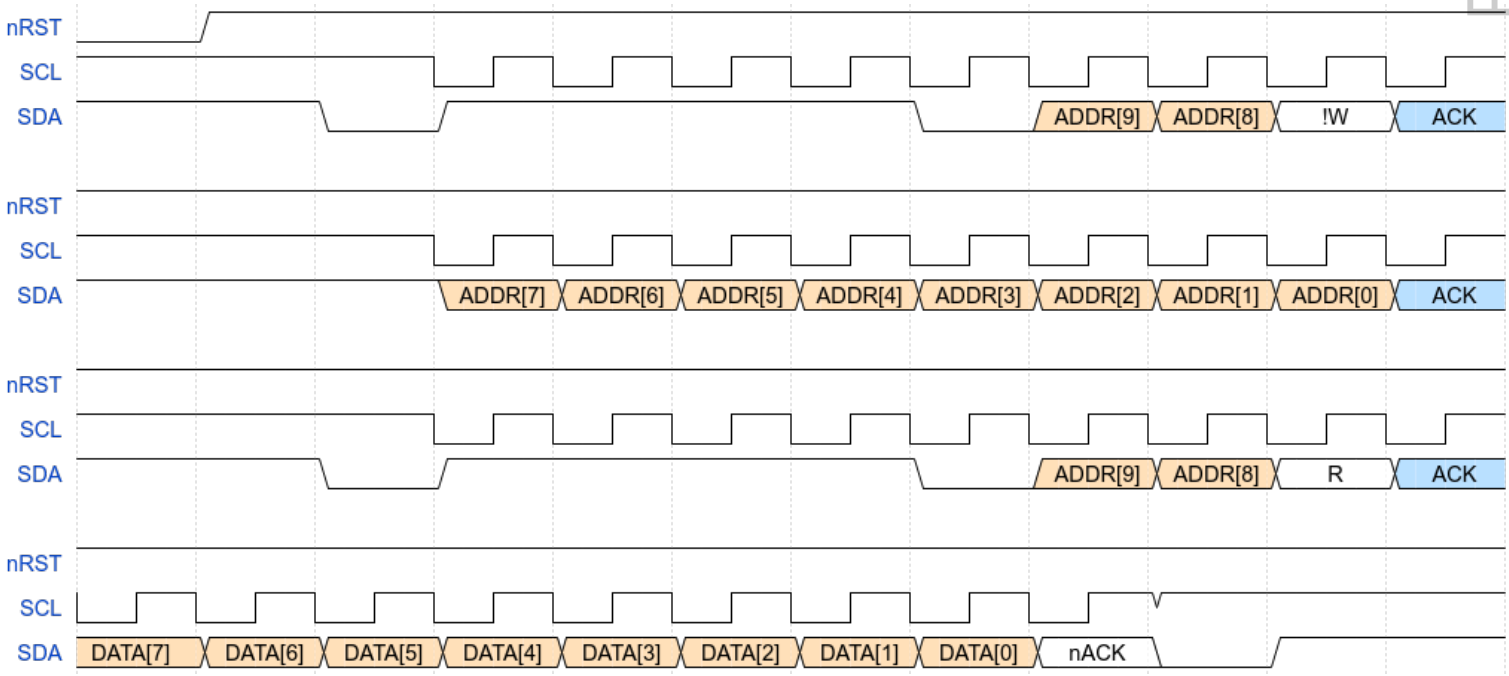

Figure 11: Read example sequence

CONFIGURATION REGISTERS

Several configuration registers are available for settling different parameters. Configuration words are divided in common parameters (see table 5), channel parameters (see table 7) and debug parameters (see table 6). Common parameters and debug parameters are shared among all the 64 channels while channel parameters are different for every channel. A total of **2700 control bits** are needed, with 339 logical registers. The registers are logically organized in groups of 8 bits.

Signal Name	bits	Function	Length	Default*	Hex	Dec	Value	Unit
Vth1	7:0	First comparator lower threshold	8	00101101	2D	45	0.66	V
Vth2	7:0	Second comparator lower threshold	8	00111010	3A	58	0.62	V
Vth3	7:0	Third comparator lower threshold	8	01010100	54	84	0.543	V
VrefDCFB	5:0	Shaper DC feedback voltage control	6	000111	07	7	0.72	V
BLHen	6	Baseline restorarion enable signal	1	1	1	1	ON	
THOFFen	7	ThDAC adjustment enable signal	1	1	1	1	OFF	
THOFF	7:0	ThDAC offset and slope adjustment	8	11111111	FF	255	?	μA
IDCFB	5:0	Shaper DC feedback current control	6	110101	35	53	?	μA
I_{SHGRAL}	7:0	Shaper reference current	8	11001000	C8	200	55	μA
Ibias	5:0	Input stage bias current	6	011101	1D	29	51	μA
Gain	7:6	Input stage gain control	2	10	2	2	1.5	-
Ifbk	5:0	Input stage feedback bias current	6	011101	1D	29	46	μA
Vref	5:0	Bandgap fine tunning voltage	6	011111	1F	31	0.5	V
IrefTRIM	5:0	Integrator trimming DAC ref. current	6	100011	23	35	50	μA
IrefOTALP	3:0	Correction OTA bias current	4	1010	A	10	50	μA
Itxslvs	4	Differential output extra current	1	0	0	0	OFF	
PZConf:		Pole zero timing configuration						
LowAtLad_PZ1	5	Pole zero 1 low attenuation	1	1	1	1	ON	
IbofHam	6	Offset current added	1	0	0	0	OFF	
				00101010	3A	42		
Rlad_PZ1	2:0	Pole zero 1 Resistor	3	001	1	1	9.2	kΩ
Cap_PZ1	6:3	Pole zero 1 Capacitance Coarse	4	0111	7	7	790	fF
CapF_PZ1	7	Pole zero 1 Capacitance Fine	1	0	0	0	OFF	1.8pF
				00111001	39	57		
Rlad_PZ2	2:0	Pole zero 2 Resistor	3	110	6	6	1.9	kΩ
Cap_PZ2	6:3	Pole zero 2 Capacitance	4	0101	5	5	560	fF
CapF_PZ2	7	Pole zero 2 Capacitance Extra	1	0	0	0	OFF	1.8pF
				00101110	2E	46		

*Bits order is MSB to LSB

Table 5: Common control register summary

Signal Name	bits	Function	Length	Default(MSB to LSB)	Value
DBG_CH	63:0	Debug input channel selector	64	0x0000000000000000	OFF
DBG_MUX	5:0	Debug analog output channel selector	6	000000	OFF
DBG_EN_OUT	6	Debug output signal selector	1	0	VTH
synMode	7	Enable serializer external input	1	0	OFF
DBG_EN_IN	0	Debug input enable signal	1	0	OFF
DBG_Cin	1	Charge injection system selector	1	0	CAL
DBG_ADC_ADDR	5:2	ADC input signal selector	4	0000	VTH0
DBG_ADC_START	6	ADC conversion trigger	1	0	OFF
aLED	7	Debug LED	1	0	OFF

Table 6: Debug control register summary

Table 7: Eight channel block control registers summary

Signal Name	bits	Function	Length	Default*	Hex	Dec	Value	Unit
D_OFF_MUX_0	3:0	CH0 input offset voltage	4	1000	8	8	0.6	V
D_OFF_MUX_1	7:4	CH1 input offset voltage	4	1000	8	8	0.6	V
D_OFF_MUX_2	3:0	CH2 input offset voltage	4	1000	8	8	0.6	V
D_OFF_MUX_3	7:4	CH3 input offset voltage	4	1000	8	8	0.6	V
D_OFF_MUX_4	3:0	CH4 input offset voltage	4	1000	8	8	0.6	V
D_OFF_MUX_5	7:4	CH5 input offset voltage	4	1000	8	8	0.6	V
D_OFF_MUX_6	3:0	CH6 input offset voltage	4	1000	8	8	0.6	V
D_OFF_MUX_7	7:4	CH7 input offset voltage	4	1000	8	8	0.6	V
D_TRIM_TDAC_0	3:0	CH0 Top Offset trimming	4	1111	F	15	0	μA
D_TRIM_BDAC_0	7:4	CH0 Bottom Offset trimming	4	1111	F	15	0	μA
D_TRIM_TDAC_1	3:0	CH1 Top Offset trimming	4	1111	F	15	0	μA
D_TRIM_BDAC_1	7:4	CH1 Bottom Offset trimming	4	1111	F	15	0	μA
D_TRIM_TDAC_2	3:0	CH2 Top Offset trimming	4	1111	F	15	0	μA
D_TRIM_BDAC_2	7:4	CH2 Bottom Offset trimming	4	1111	F	15	0	μA
D_TRIM_TDAC_3	3:0	CH3 Top Offset trimming	4	1111	F	15	0	μA
D_TRIM_BDAC_3	7:4	CH3 Bottom Offset trimming	4	1111	F	15	0	μA
D_TRIM_TSIGN_0	0	CH0 Top trimming sign	1	1	1	1	DOWN	
D_TRIM_BSIGN_0	1	CH0 Bottom trimming sign	1	1	1	1	DOWN	
D_TRIM_TSIGN_1	2	CH1 Top trimming sign	1	1	1	1	DOWN	
D_TRIM_BSIGN_1	3	CH1 Bottom trimming sign	1	1	1	1	DOWN	
D_TRIM_TSIGN_2	4	CH2 Top trimming sign	1	1	1	1	DOWN	
D_TRIM_BSIGN_2	5	CH2 Bottom trimming sign	1	1	1	1	DOWN	
D_TRIM_TSIGN_3	6	CH3 Top trimming sign	1	1	1	1	DOWN	
D_TRIM_BSIGN_3	7	CH3 Bottom trimming sign	1	1	1	1	DOWN	
D_TRIM_TDAC_4	3:0	CH4 Top Offset trimming	4	1111	F	15	0	μA
D_TRIM_BDAC_4	7:4	CH4 Bottom Offset trimming	4	1111	F	15	0	μA
D_TRIM_TDAC_5	3:0	CH5 Top Offset trimming	4	1111	F	15	0	μA
D_TRIM_BDAC_5	7:4	CH5 Bottom Offset trimming	4	1111	F	15	0	μA
D_TRIM_TDAC_6	3:0	CH6 Top Offset trimming	4	1111	F	15	0	μA
D_TRIM_BDAC_6	7:4	CH6 Bottom Offset trimming	4	1111	F	15	0	μA
D_TRIM_TDAC_7	3:0	CH7 Top Offset trimming	4	1111	F	15	0	μA
D_TRIM_BDAC_7	7:4	CH7 Bottom Offset trimming	4	1111	F	15	0	μA
D_TRIM_TSIGN_4	0	CH4 Top trimming sign	1	1	1	1	DOWN	
D_TRIM_BSIGN_4	1	CH4 Bottom trimming sign	1	1	1	1	DOWN	
D_TRIM_TSIGN_5	2	CH5 Top trimming sign	1	1	1	1	DOWN	
D_TRIM_BSIGN_5	3	CH5 Bottom trimming sign	1	1	1	1	DOWN	
D_TRIM_TSIGN_6	4	CH6 Top trimming sign	1	1	1	1	DOWN	
D_TRIM_BSIGN_6	5	CH6 Bottom trimming sign	1	1	1	1	DOWN	
D_TRIM_TSIGN_7	6	CH7 Top trimming sign	1	1	1	1	DOWN	
D_TRIM_BSIGN_7	7	CH7 Bottom trimming sign	1	1	1	1	DOWN	
D_Vth1_0	7:0	CH0 lower threshold local value	8	11111111	FF	255	0	V
D_Vth2_0	7:0	CH0 middle threshold local value	8	11111111	FF	255	0	V
D_Vth3_0	7:0	CH0 higher threshold local value	8	11111111	FF	255	0	V
D_Vth1_1	7:0	CH1 lower threshold local value	8	11111111	FF	255	0	V
D_Vth2_1	7:0	CH1 middle threshold local value	8	11111111	FF	255	0	V
D_Vth3_1	7:0	CH1 higher threshold local value	8	11111111	FF	255	0	V
D_Vth1_2	7:0	CH2 lower threshold local value	8	11111111	FF	255	0	V
D_Vth2_2	7:0	CH2 middle threshold local value	8	11111111	FF	255	0	V

*Bits order is MSB to LSB

– continued on next page

Table 7 – continued from previous page

Signal Name	bits	Function	Length	Default*	Hex	Dec	Value	Unit
D_Vth3_2	7:0	CH2 higher threshold local value	8	11111111	FF	255	0	V
D_Vth1_3	7:0	CH3 lower threshold local value	8	11111111	FF	255	0	V
D_Vth2_3	7:0	CH3 middle threshold local value	8	11111111	FF	255	0	V
D_Vth3_3	7:0	CH3 higher threshold local value	8	11111111	FF	255	0	V
D_Vth1_4	7:0	CH4 lower threshold local value	8	11111111	FF	255	0	V
D_Vth2_4	7:0	CH4 middle threshold local value	8	11111111	FF	255	0	V
D_Vth3_4	7:0	CH4 higher threshold local value	8	11111111	FF	255	0	V
D_Vth1_5	7:0	CH5 lower threshold local value	8	11111111	FF	255	0	V
D_Vth2_5	7:0	CH5 middle threshold local value	8	11111111	FF	255	0	V
D_Vth3_5	7:0	CH5 higher threshold local value	8	11111111	FF	255	0	V
D_Vth1_6	7:0	CH6 lower threshold local value	8	11111111	FF	255	0	V
D_Vth2_6	7:0	CH6 middle threshold local value	8	11111111	FF	255	0	V
D_Vth3_6	7:0	CH6 higher threshold local value	8	11111111	FF	255	0	V
D_Vth1_7	7:0	CH7 lower threshold local value	8	11111111	FF	255	0	V
D_Vth2_7	7:0	CH7 middle threshold local value	8	11111111	FF	255	0	V
D_Vth3_7	7:0	CH7 higher threshold local value	8	11111111	FF	255	0	V
D_SELVTH_0	0	CH0 threshold selection	1	0	0	0	COM	
D_SELVTH_1	1	CH1 threshold selection	1	0	0	0	COM	
D_SELVTH_2	2	CH2 threshold selection	1	0	0	0	COM	
D_SELVTH_3	3	CH3 threshold selection	1	0	0	0	COM	
D_SELVTH_4	4	CH4 threshold selection	1	0	0	0	COM	
D_SELVTH_5	5	CH5 threshold selection	1	0	0	0	COM	
D_SELVTH_6	6	CH6 threshold selection	1	0	0	0	COM	
D_SELVTH_7	7	CH7 threshold selection	1	0	0	0	COM	

*Bits order is MSB to LSB

Table 7: Eight channel block control registers summary

Table 8 summarizes the address of the registers, with length and contents. Their contents map directly to control signals in tables 7, 6 and 5. LED output is directly driven by the corresponding bit in register.

Name	Function	Bits used (total)	Address Range
Common Register	Controls for common bias block	103 (112)	x001h-x00Eh
Channels 0-7 Register	Controls channel specific features	312 (312)	x00Fh-x035h
Channels 8-15 Register	Controls channel specific features	312 (312)	x036h-x05Ch
Channels 16-23 Register	Controls channel specific features	312 (312)	x05Dh-x083h
Channels 24-31 Register	Controls channel specific features	312 (312)	x084h-x0AAh
Channels 32-39 Register	Controls channel specific features	312 (312)	x0ABh-x0D1h
Channels 40-47 Register	Controls channel specific features	312 (312)	x0D2h-x0F8h
Channels 48-55 Register	Controls channel specific features	312 (312)	x0F9h-x11Fh
Channels 56-63 Register	Controls channel specific features	312 (312)	x120h-x146h
Debug Register	Controls for debug functions	80 (80)	x147h-x150h
ADC Register*	ADC output registers	16 (16)	x151h-x152h
Error Register*	Counters for Hamming detected errors	16 (16)	x153h-x154h

*Read only registers.

Table 8: Registers addresses summary

FLOORPLAN

A total size of 15.4mm^2 (4000μm x 3850μm) has been needed to include the described functionality. PACIFICr5 is divided into four identical 16 channel blocks, each one placed in one corner of the die. The common biasing generation structure was placed between the two left blocks and the ADC between the right ones. The slow control logic and configuration registers are located between the left and right blocks. Some of the signals are common to all the blocks (channels debugging control basically) while others are in separated registers (common analog references and voltages setup). In figure 12 the top layout can be observed with both sides highlighted.

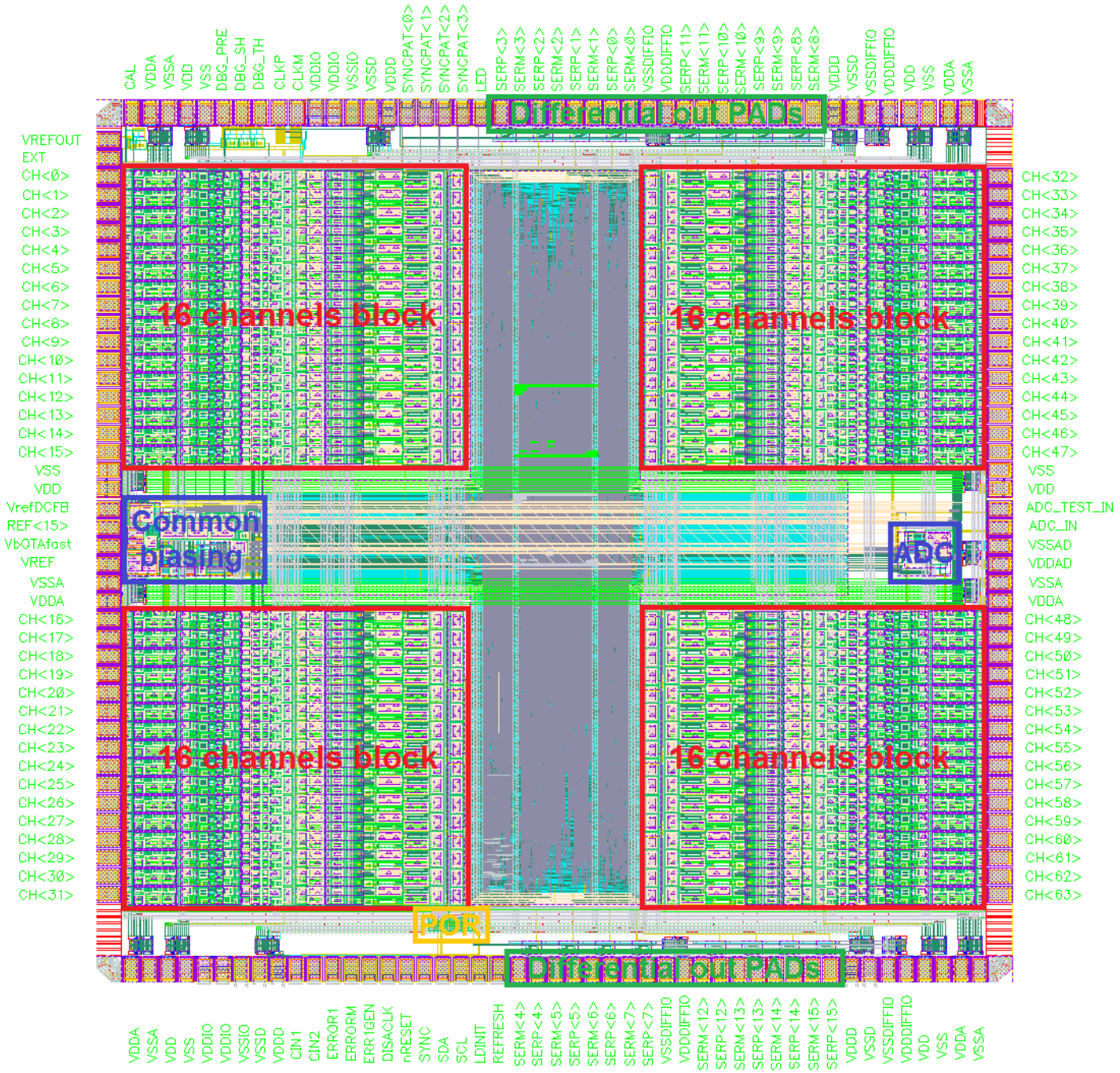

Figure 12: PACIFICr5 Die of 4000μm x 3850μm with blocks

POWER DISTRIBUTION

Different power domains are present in the design. The different VSS connections are separated logically during design but are all connected to the same substrate. On the power supply, different power rails are used until the PCB level (there could be joined to the same power supply). This allows for external filtering if needed, avoiding any noise transmission between power supplies. Several redundant power pad's (see figure 13) have been placed in the design to reduce the parasitic inductance and voltage drop.

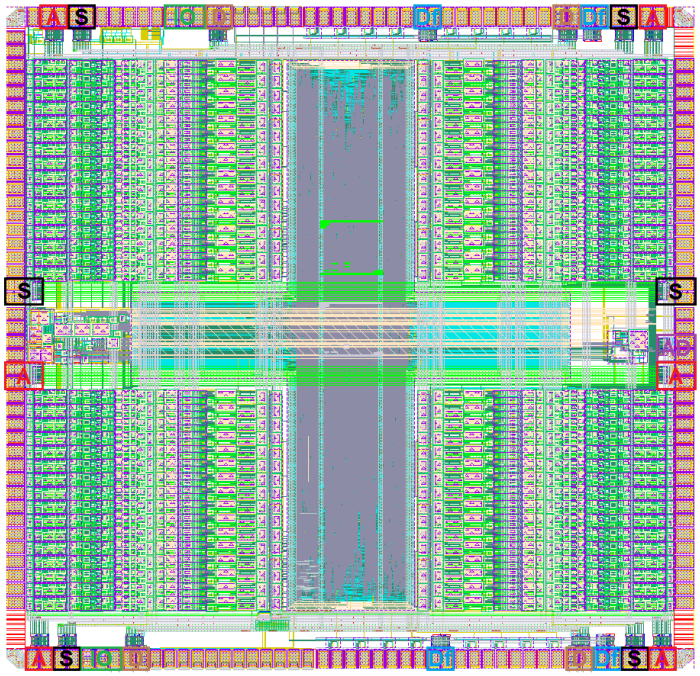

Figure 13: PACIFICr5 Power Pads placement

Different power pairs on figure 13 are from the different power domains present on PACIFICr5;

- **A** - VDDA/VSSA Analog power PAD pairs
- **S** - VDD/VSS Switched power PAD pairs
- **D** - VDDD/VSSD Digital power PAD pairs
- **IO** - VDDIO/VSSIO Digital in/out buffers power PAD pairs
- **Df** - VDDDIFFO/VSSDIFFO Digital differential out buffers power PAD pairs
- **AD** - VDDAD/VSSAD ADC power PAD pairs

ESD PROTECTION

TSMC recommendations lead to the inclusion of the PCLAMPA cells to avoid any damage on all the power supply connections from the device, except of the digital in/out buffers power PAD pairs VDDIO/VSSIO. In figure 14 the placement of the cells is depicted (highlighted in orange boxes).

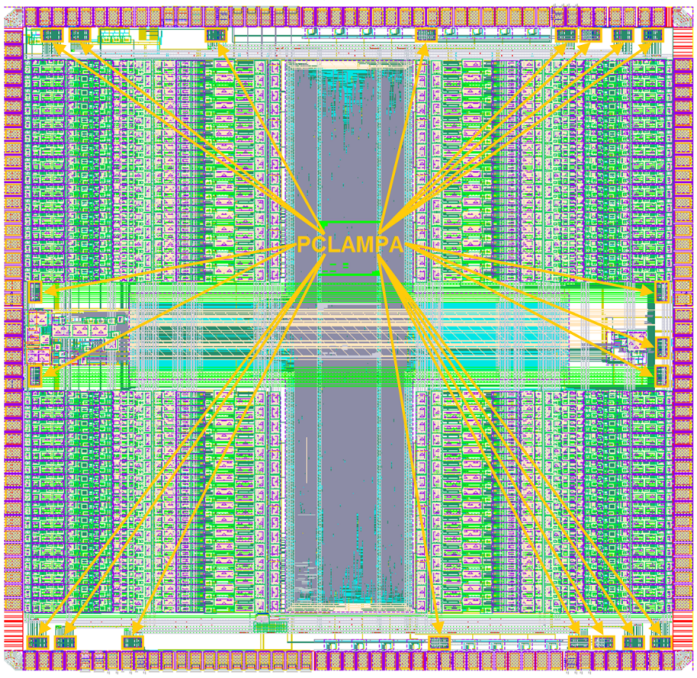

Figure 14: PACIFICr5 clamp cells

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

APPLICATION INFORMATION

In order to match the desired application implemented solution has different features to improve overall behaviour of the combined electronics and sensor system. To achieve this goal some boundary conditions must be defined.

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating
V_{DDA}	1.2 V
V_{DD}	1.2V
V_{DDD}	1.2 V
V_{DDADC}	1.2 V
V_{DDIO}	1.5 V
Temperature Range	
Operatingjunction	-40°C to 125°C
Storage	-65°C to 150°C
Soldering Conditions	To Be Determined

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTES

http://icc.ub.edu
http://www.physi.uni-heidelberg.de
http://clrwww.in2p3.fr
http://ific.uv.es