GLAST Large Area Telescope

LAT Flight Software
System Checkout TRR

Test Environment

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Test Environment

- Configuration Management
- Code Version Control
- Testbed
- Other EGSE
  - FES
  - LTX
  - VSC
  - ADCSIM
- Primary Test Configuration
- Special Test Configurations

Configuration Management

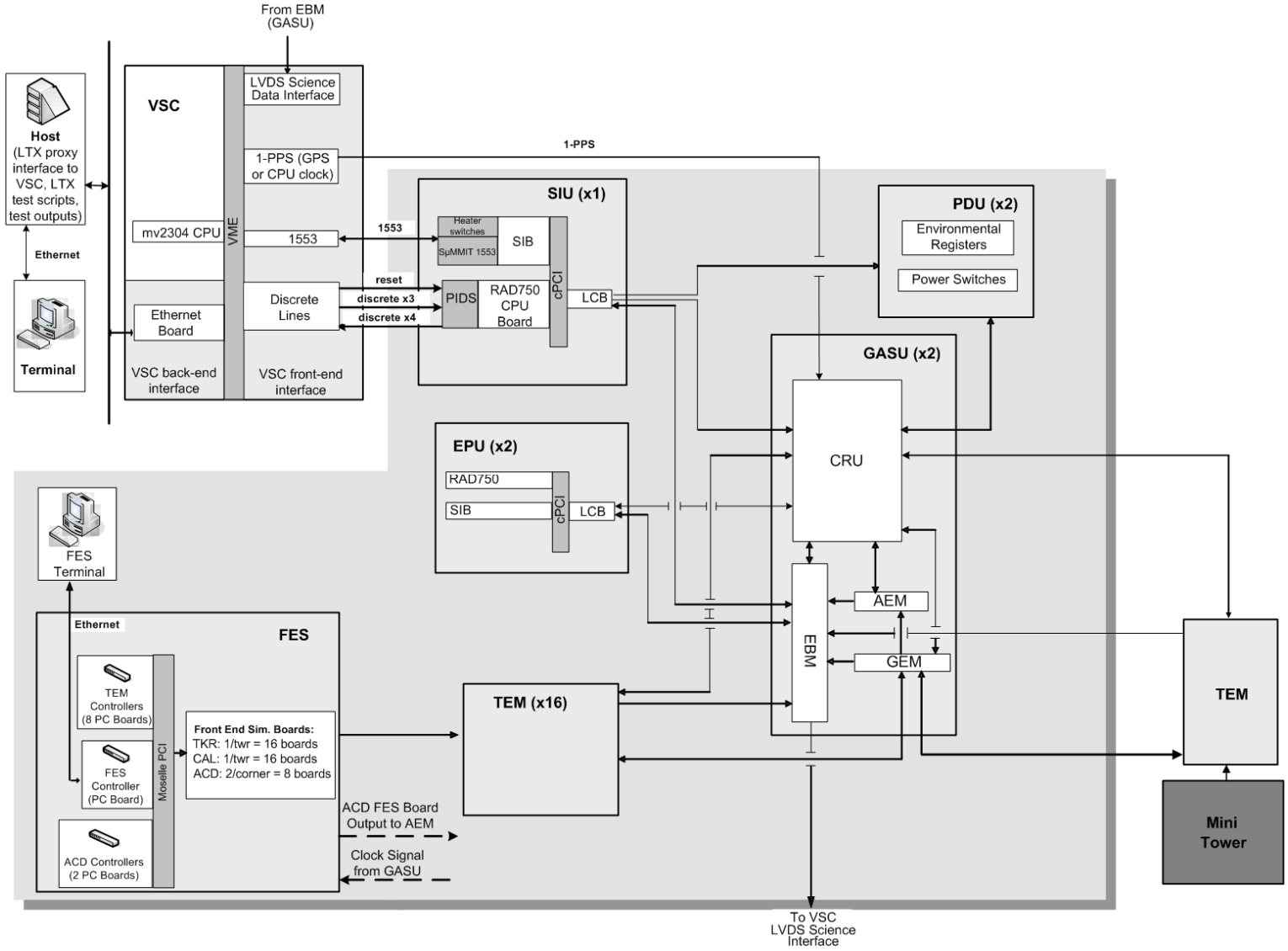
- Hardware
  - Hardware database used to keep track of units/versions
    - All hardware units are assigned a GLAT# (bar coded)
    - GLAT# recorded in LAT-DS-03541
  - Each FPGA also has unique VHDL# (stored electronically)
    - HW version info available in diagnostic telemetry packet
- FSW and Test scripts
  - CMX
- Documents
  - LATDocs

Code Version Control

- **CMX (Test Procedures and Test Scripts)**
  - **Command-line driven code management tool built on the CVS and CMT systems**
  - **Developed and maintained by the FSW Development Team**
  - **Tracks source files as they are checked in and out (with transaction logging)**
  - **Defines lists of files and file/versions within the library**
  - **Test Team engineers check out source files into private areas, modify them, test the changes then check them back in.**

- **FMX (FSW Builds)**
  - **Used by the Test Team to create "uploadable" builds, each defined by a specification file**
  - **FMX processes a list of FSW packages by version, then outputs encoded, compressed library and configuration files for upload**
    - **File numbers/IDs assigned automatically according to location in a random access database table**
  - **FMX also produces a startup and initialization file used by the secondary boot code to locate and load software modules during boot**

Testbed


From EBM
(GASU)
Host
(LTX proxy interface to VSC, LTX test scripts, test outputs)
Ethernet
Terminal
VSC
LVDS Science Data Interface
1-PPS (GPS or CPU clock)
mv2304 CPU
VME
1553
Ethernet Board
Discrete Lines
VSC back-end interface
VSC front-end interface
1-PPS
1553
reset
discrete x3
discrete x4
SIU (x1)
Heater switches
SμMMIT 1553
SIB
PIDS
RAD750 CPU Board
cPCI
LCB
PDU (x2)
Environmental Registers
Power Switches
GASU (x2)
CRU
EPU (x2)
RAD750
SIB
cPCI
LCB
FES Terminal
Ethernet
FES
TEM Controllers (8 PC Boards)
FES Controller (PC Board)
ACD Controllers (2 PC Boards)
Moselle PCI
Front End Sim. Boards:
TKR: 1/twr = 16 boards
CAL: 1/twr = 16 boards
ACD: 2/corner = 8 boards
ACD FES Board Output to AEM
Clock Signal from GASU
TEM (x16)
EBM
AEM
GEM
TEM
Mini Tower
To VSC LVDS Science Interface

Front End Simulator (FES)

- The Front End Simulator permits testing of static and dynamic properties of the LAT T&DF system.
- FES system components:
  - An assembly of Front End Simulator electronics boards controlled by PCs.
  - On the input side, the PCs define the signal patterns to be pulsed to the T&DF system
    - Both simple patterns and Monte Carlo-generated physics data patterns.
  - On the output side, the FES boards manage the time sequenced distribution of data and the data presentation to the T&DF subsystem trigger and data cables.
    - The boards use the data to simulate both the sensor side and cable side of the LAT front-end electronics.
- A User System Control provides a user interface to the entire system, allowing testers to simulate anywhere from one contributor up to a number of contributors representing the entire LAT.

LAT Test Executive (LTX)

- **LTX is a tool designed to create, edit, execute, and save qualification tests written by the LAT FSW Test Team.**
  - **Implemented entirely in Python and XML and utilizes some shell scripting**
  - **A MySQL database system is used to archive test results and products**
  - **The syntax of the commands and various other features are based on CMX**

- **PCs on which LTX can be run are networked (via unix hosts) with the Testbed CPUs.**

Virtual Spacecraft (VSC)

- **Spacecraft simulator EGSE:**
  - **Provides a complete implementation of the LAT to Spacecraft ICD with emulation of all hardware interfaces between the spacecraft at the LAT.**
    - **1553 and discrete line connections to the SIU**
    - **1-PPS time hack signal and 1 Hz time tone message**
    - **Support for data output from the LAT on the science data interface**
  - **Provides software to:**
    - **Drive the hardware**
    - **Expose a "front-end" interface to the LAT and a "back-end" and "proxy" interface to other EGSE and testing tools**
  - **The VSC provides full SC to LAT interface redundancy and cross-strapping support.**
- **Built at SLAC by the Trigger and Dataflow Electronics Engineering Team**

ADCSIM Software

- FSW is responsible for collecting and reporting environmental quantities stored in registers in the LAT's Power Distribution Units (PDUs).
  - PDU registers are read by the thermal control FSW
  - In addition, subsets of the data are assembled by the housekeeping FSW for transmission to the ground in narrowband telemetry
- A special-purpose software package, ADCSIM, allows test engineers to work with simulated raw ADC values and thus provide readouts for testing.
  - Simulates raw ADC values read from the TEM, PDU, and ACD hardware by intercepting LAT Communications Board (LCB) command lists and encoding the data in the corresponding result lists.
  - A single ADCSIM library is loaded to and executed on the SIU during qualification tests that require simulated readouts.
- Coding of the ADCSIM package is a responsibility of the FSW Development Team.

Primary Test Configuration

- All 46 qualification tests run on the Testbed
  - 1 test uses *additional* EGSE (Corelis)
  - 2 tests run special-purpose test software loaded to the Testbed SIU (ADCSIM)
- The following tests are run on the Testbed, without special hardware or software, using either the full Testbed configuration or a subset of the configuration:
  - MEMMGT_001, 002
  - CMDFNC_001, 002, 003
  - IPCFNC_001
  - SIUCFG_001, 002
  - TIMPRC_001
  - EVTPMO_001, 002, 003, 004
  - EVTFIL_001, 002, 003, 004
  - DCMODE_001, 002, 003
  - NBTLMV_001, 002
  - FSWINI (except 003)
  - FECALB_001, 002, 003, 004, 005
  - WBTLMV_001
  - FILMGT_001
  - OPMODE_001
  - VSGIFV_001

Special Test Configurations

- **Test FSWINI_003 makes use of Corelis hardware and utilities:**
  - **A Corelis crate and a PC running Corelis software applications and tools are located "off" the Testbed.**
  - **During the test, the SIU's RAD750 board is physically removed from the SIU crate and slotted into the Corelis crate**
  - **At the Corelis PC, JTAG utilities are used to load a corrupt primary boot code image to the RAD750 board**
  - **The RAD750 board is then returned to the SIU crate on the Testbed, and the test continues**

- **Tests NBTLMV_003 and THRMCS_001 use ADCSIM software:**
  - **In both tests, the libadcsim.o constituent is loaded to SIU RAM during the test sequence, and removed at the end of the test**
  - **NBTLMV_003 uses the library to simulate FREE board environmental registers and create an alert condition**
  - **THRMCS_001 uses the library to simulate the PDU environmental ADC values read as inputs to the thermal control algorithm**