

**Gamma-ray Large  
Area Space  
Telescope**



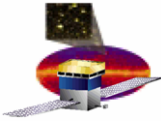
# **GLAST Large Area Telescope**

**Instrument Flight Software  
EM2 Review  
26 February 2004**

**Instrument Configuration**

**Curt Brune  
Stanford Linear Accelerator Center**

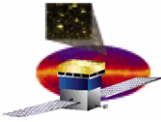
**[curt@slac.stanford.edu](mailto:curt@slac.stanford.edu)  
650-926-4028**



# Instrument Configuration: Requirements

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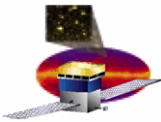
- **Flight Software General Requirements:**
  - **Req. [5.3.4.6.2](#): FSW shall read back and record the configuration of the CAL, TKR, ACD, T&DF and LAT power supply subsystems by reading back the T&DF provided configuration registers.**
  - **Req. [5.3.4.6.1](#): FSW shall configure the CAL, TKR, ACD, T&DF, and LAT power-supply subsystems by writing to the T&DF-provided configuration registers.**



# Instrument Configuration: Functional Components

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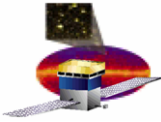
- **Functional Inputs**
  - **FSW receives different inputs for its write and read operations:**
    - **Write:**
      - Addressing data that identifies registers of LAT subsystems (TKR, CAL, ACD, TEM, CRU, EBM, GEM, and PDU)
      - Data to write to the register
    - **Read:**
      - Addressing data
- **Functional Processing**
  - **FSW produces bit streams that are sent to the registers of subsystems on the LAT**
  - **FSW decodes responses received from registers of subsystems on the LAT**
  - **FSW validates responses by checking parity**
- **Functional Outputs**
  - **FSW outputs values read from registers on the LAT (TKR, CAL, ACD, TEM, AEM, CRU, EBM, GEM, and PDU)**
  - **FSW outputs I/O completion status and time stamps**



# Instrument Configuration: Overview

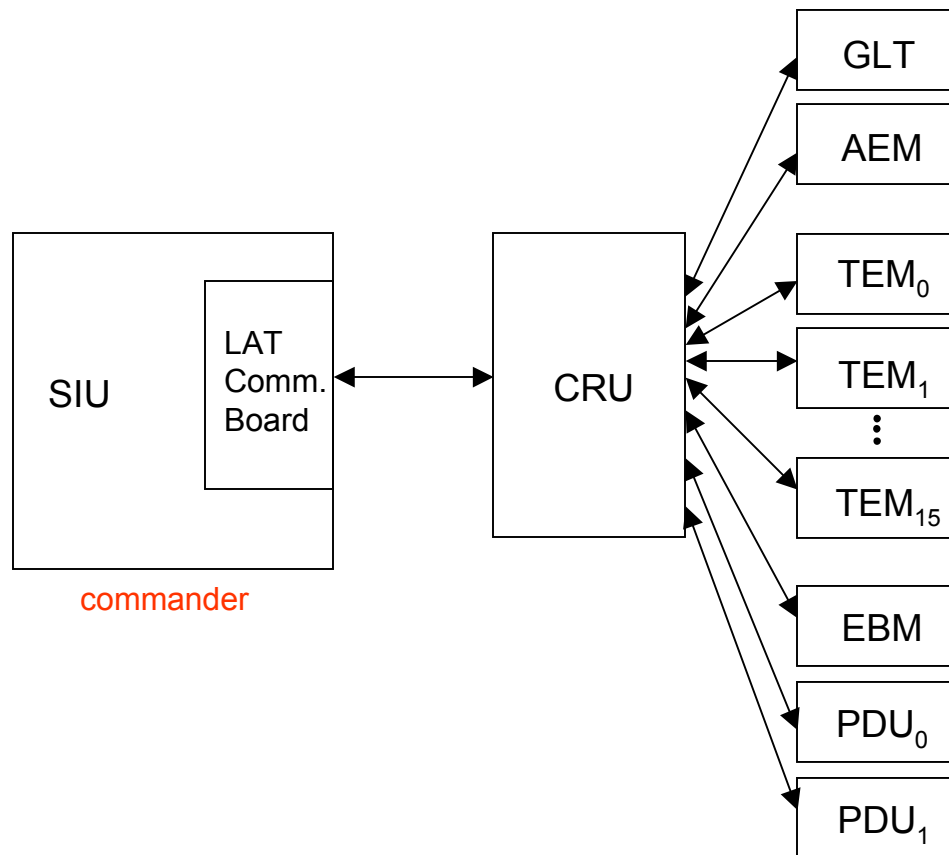
- **Purpose**
  - To place and maintain the instrument in a known configuration
  - To report the configuration
    - Knowledge of instrument configuration is *essential* to a successful physics analysis
- The instrument appears to flight software as a collection of registers
  - *A large collection*

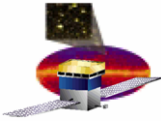
Subsystem / Block	Chip / Sub-block	Number in Instrument	Register Count	Register documentation
TKR	GTFE	13824	69120	<a href="#">LAT-SS-00169</a>
	GTRC	1152	2304	<a href="#">LAT-SS-00170</a>
CAL	GCFE	3072	21504	<a href="#">LAT-TD-00424</a>
	GCRC	256	2048	<a href="#">LAT-SS-00208</a>
ACD	GAFE	216	2376	<a href="#">LAT-SS-00363</a>
	GARC	12	528	
TEM	GTCC	128	768	<a href="#">LAT-TD-00605</a>
	GCCC	64	448	
	GTIC	16	272	
	Common	16	112	
GASU	AEM	1 (primary and redundant)	6	<a href="#">LAT-TD-00639</a>
	CRU	1 (primary and redundant)	4	<a href="#">LAT-TD-01547</a>
	EBM	1 (primary and redundant)	31	<a href="#">LAT-TD-01546</a>
	GEM	1 (primary and redundant)	59	<a href="#">LAT-SS-01596</a>
PDU			7	<a href="#">LAT-SS-01543</a>
			99587	



# Instrument Configuration: Communications Architecture

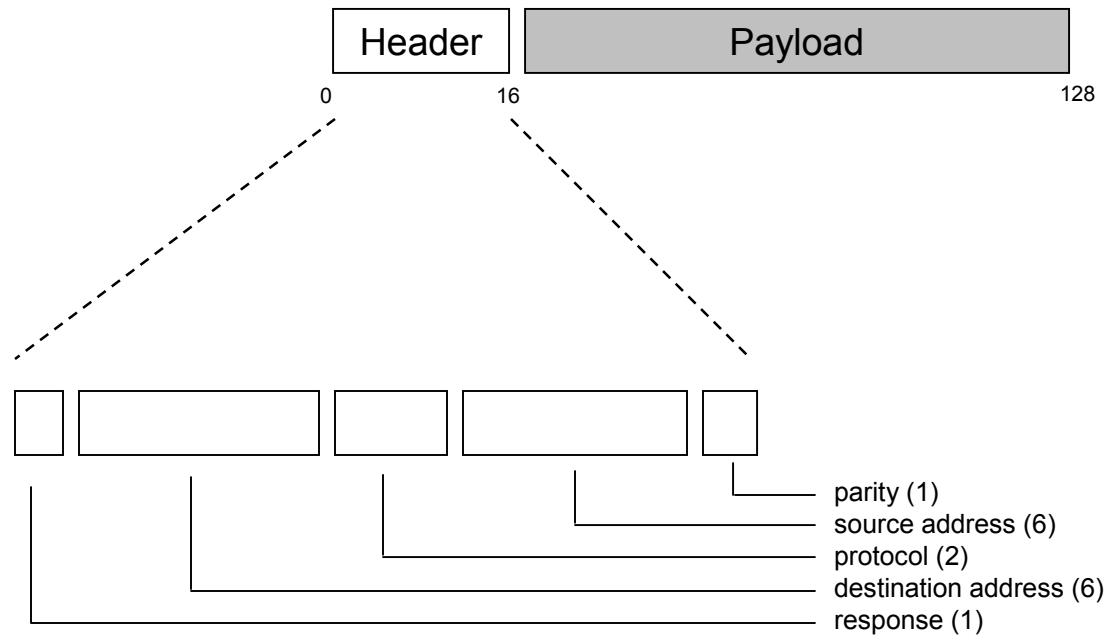
- Communications with registers on the CAL, TKR, ACD, T&DF and LAT power supply subsystems occur over a network fabric using the LATp communications protocol:
  - Certain nodes (SIUs) are *commanders*. Other nodes (EPUs, Tower Electronics Modules, ACD Electronics Modules, Global Triggers) are *responders*.

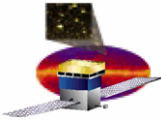




# Instrument Configuration: Communications Architecture (cont'd)

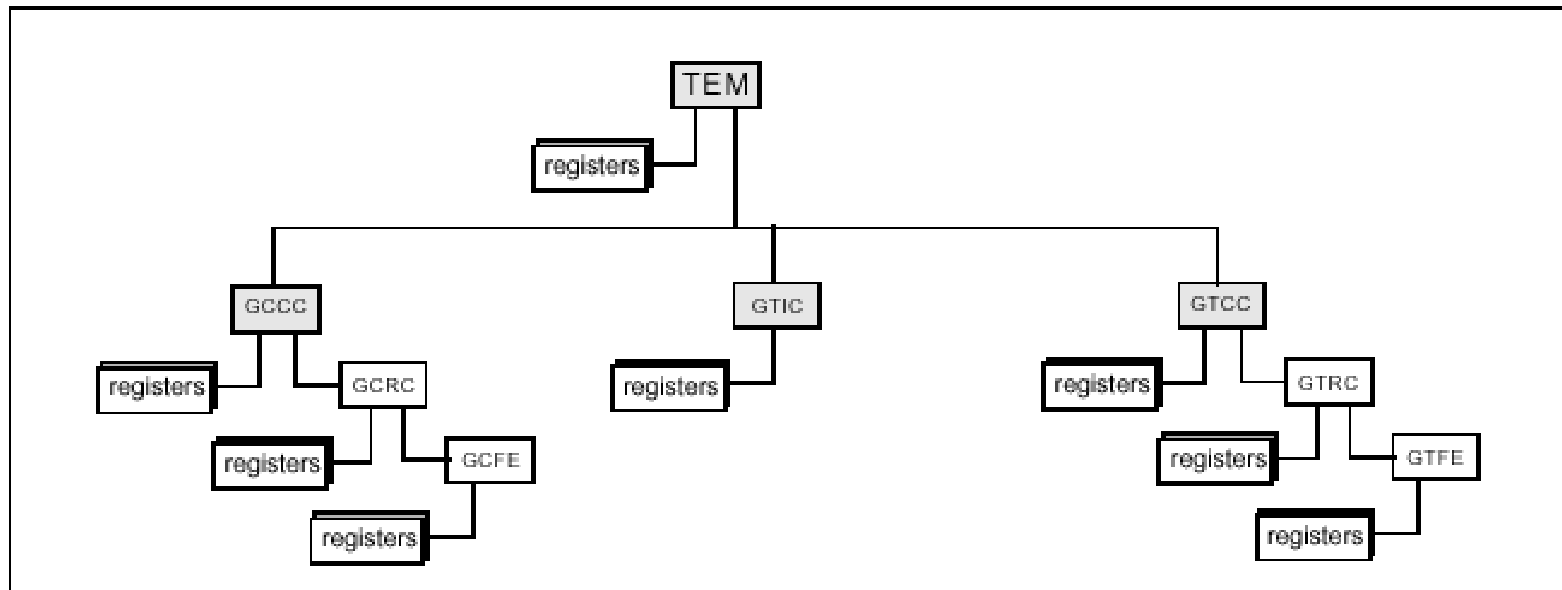
- The LATp protocol provides a type of communication packet called a *command packet*. Command packets are used to send read and write commands to registers on the LAT.
- LATp command packets are 128 bits long. They are broken down into a header of 16 bits, followed by 112 node-specific bits.

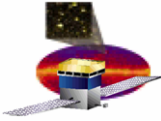




# Instrument Configuration: Reaching the Registers

- The registers in a LATp node (e.g., a TEM) are arranged in a hierarchy of function blocks (e.g., a TEM CAL cable controller), each block containing registers and possibly more function blocks.
- To access the registers of a function block, one specifies the hierarchical path to the register.

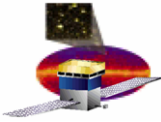




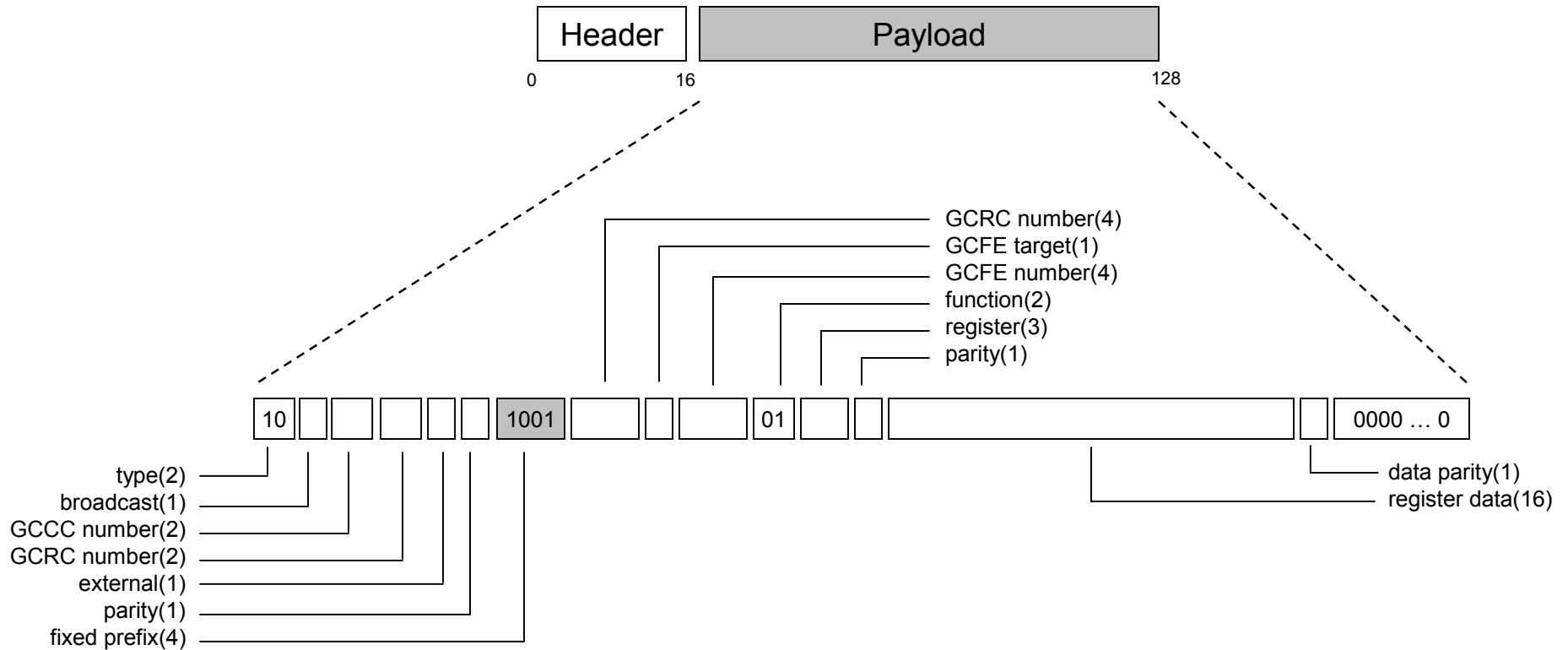
## Instrument Configuration: Reaching the Registers (cont'd)

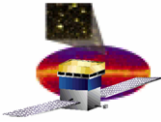
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- For instance, to write a register in the CAL front-end ASIC, one specifies the path through the hierarchy, indicating:
  - Which of the 16 TEMs (LATp nodes) to address
  - Which of the 4 GCCCs (TEM board ASICs) to address
  - Which of the 4 GCRCs (off-board CAL layer readout controller ASICs) to address
  - Which of the 12 GCFEs (off-board CAL front-end ASICs) to address
  - Which of the 7 registers on that GCFE to write to
- The next slide illustrates the packet structure used to write to a register on the CAL front-end ASIC.



# Instrument Configuration: Reaching the Registers (cont'd)

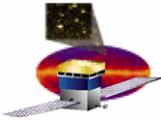




# Instrument Configuration: Reaching the Registers (cont'd)

- The same messaging and addressing system is used to write and read registers on all subsystems.

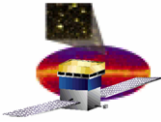
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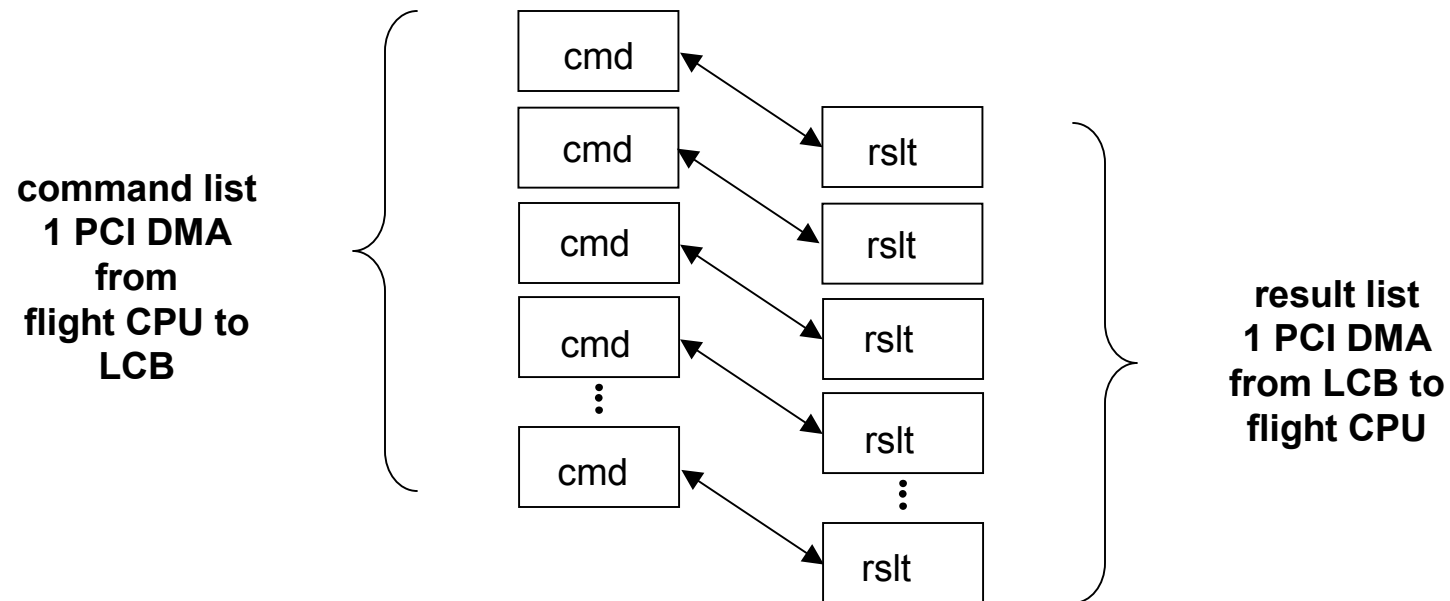
## Instrument Configuration: Sending Multiple Commands

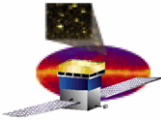
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- To speed up configuration, multiple commands and responses can be bundled into DMA transfer operations between a flight CPU (e.g., an SIU) and the LAT Communications Board (LCB):
  - Multiple command items in a “command list” are DMA’d to the LCB.
    - There the command items are sent one by one to LAT subsystems.
    - The command list can be up to 4 KB long, enough space to hold 150 register write commands.
  - Multiple responses are assembled into a “results list.”
    - All results have a timestamp and a status word.
    - For command items that expect a response, the result item also contains the data read back from the instrument subsystem.
    - The results list can also be up to 4 KB long.
  - A one-to-one relationship between items on the command and results lists is maintained.
  - The results list is DMA’d back to the flight CPU, and LCB raises an interrupt to signal the transfer is complete.



# Instrument Configuration: Sending Multiple Commands (cont'd)

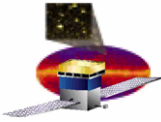




# Instrument Configuration: Software Implementation

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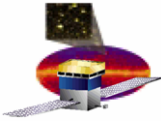
- **Communications via LATp and transmission of bit strings carrying register settings are handled by three completed FSW packages:**
  - **The LCB package controls the LAT Communications Board (PCI register access) and handles LATp communications**
  - **The DEM package constructs bit strings bound for registers on the ACD, CAL, & TKR, as well as the TEM and AEM**
  - **The DAB package constructs the bit strings for registers on the CRU, EBM, GEM, and PDU**



# Instrument Configuration: Testing

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- **PCI layer:**
  - Test software's ability to read and write PCI memory registers on the LCB
  - Test software's ability to detect and recover from DMA errors by deliberately introducing DMA errors
- **Command/response layer:**
  - Test software's ability to fill in payload bits of a command item
  - Test software's ability to add and remove command items from a command list
  - Test software's ability to transfer command lists by DMA operation
  - Test software's ability to respond to LCB interrupts
  - Test software's ability to receive results lists by DMA operation
  - Test software's ability to iterate through a results list
  - Test software's ability to extract status word, time stamp, and result payload from result items
  - Test that the command and results lists can handle the maximum 4 KB load
- **DEM/DAB package layer:**
  - Test software's ability to perform register writes and verify that software constructs bit string correctly
  - Test software's ability to decode response bit strings correctly



# Instrument Configuration: Consumers

	Test Stands		ISIS	I&T	FSW Test-bed	FSW Deliverable
	TKR,CAL	ACD				
Configure TKR, CAL, and TEM front end electronics	Y			Y	Y	Y
Configure ACD front end electronics		Y		Y	Y	Y
Configure CRU, GEM, EBM, AEM		Y	Y	Y	Y	Y
Configure PDU			Y	Y	Y	Y

- **Status:**
  - Coding of LCB, DEM, and DAB packages is complete.
- **Test Stands:**
  - For debugging purposes, the Test Stand engineers can fully configure registers on LAT subsystems as they are added.
- **ISIS:**
  - The GSE can read registers on the CRU, EBM, GEM, and PDU (for example, retrieve temperature data from the PDU)
- **I&T:**
  - I&T is able to fully configure all integrated subsystems.
- **FSW Test-bed:**
  - FSW is able to test its code against various configurations of LAT hardware.