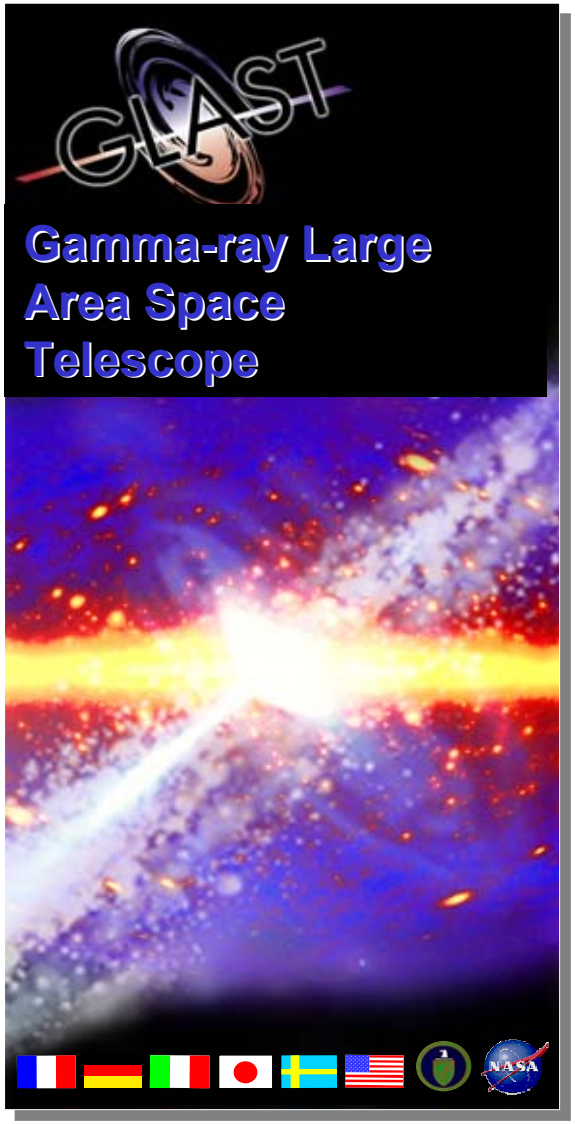

GLAST Large Area Telescope:

Electronics, Data Acquisition & Instrument Flight Software

Flight Software – Overview

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LAT Chief Electronics Engineer

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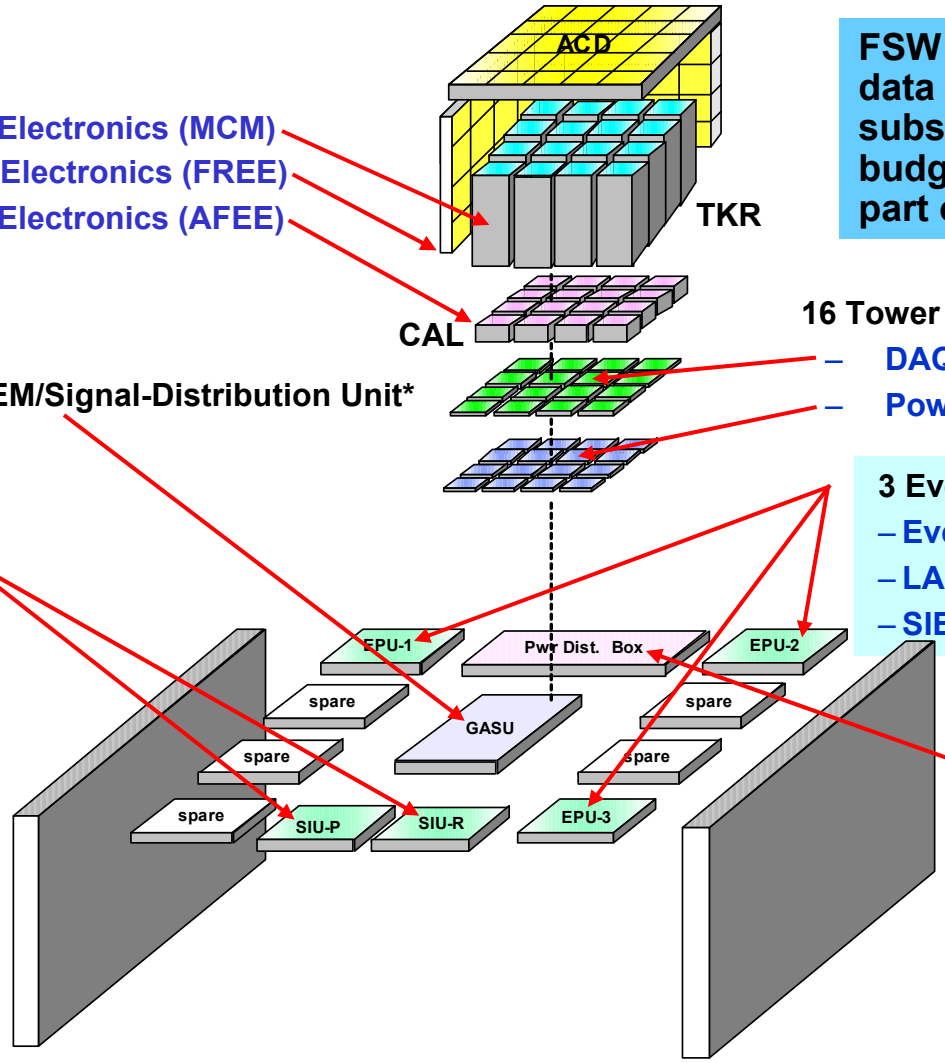
Outline

- DAQ vs. FSW
- FSW Overview
- Team
- Development Plan
- Schedule & Milestones
- Resource Profile
- Documents
- Interfaces
- Risk Analysis
- Changes since PDR
- Resource monitoring

LAT Electronics

TKR Front-End Electronics (MCM)
ACD Front-End Electronics (FREE)
CAL Front-End Electronics (AFEE)



FSW is an integral part of the data acquisition (DAQ) subsystem and is managed, budgeted and scheduled as part of the DAQ subsystem

16 Tower Electronics Modules
- DAQ electronics module (DAQ-EM)
- Power-supplies for tower electronics

3 Event-Processor Units (2 + 1 spare)
- Event processing CPU
- LAT Communication Board
- SIB

Spacecraft Interface Units
- Spacecraft Interface Board (SIB): Spacecraft interface, control & data
- LAT control CPU
- LAT Communication Board (LCB): LAT command and data interface

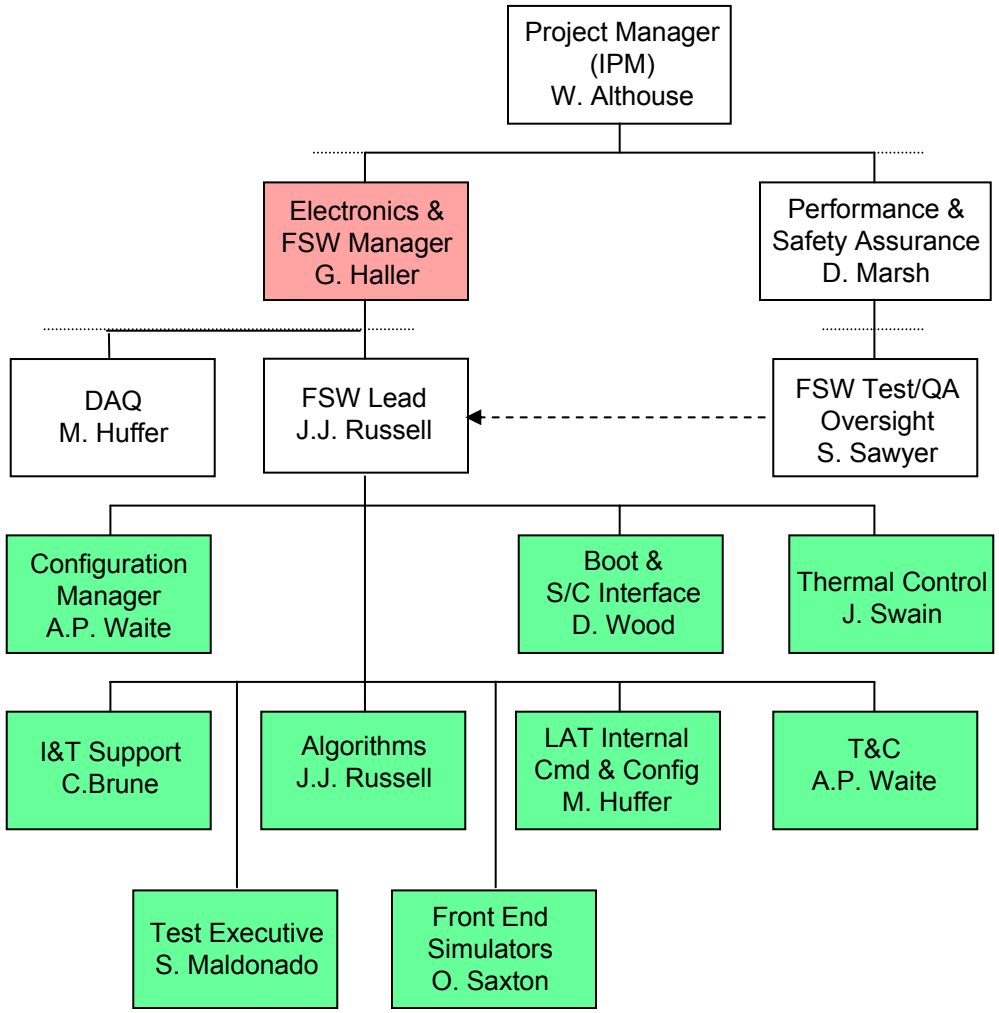
Power-Distribution Unit (PDU)*
- Spacecraft interface, power
- LAT power distribution
- LAT health monitoring

* Primary & Secondary Units shown in one chassis

FSW Overview

- **LAT FSW is divided into two components**
  - **SIU FSW**
    - **LAT command and control from SC via 1553**
      - **LAT hardware configuration and data collection control**
      - **LAT hardware power control**
      - **LAT thermal control system**
    - **Gathering and distribution of LAT TLM via 1553 and SSR**
    - **Low rate science**
      - **Event monitoring for performance information**
    - **Transient detection (GRB / AGN)**
      - **Alert messages to ground**
      - **Repoint requests to SC**
    - **Calibration / diagnostics**
  - **EPU FSW**
    - **LAT event data processing / filtering**
    - **Calibration / diagnostics**

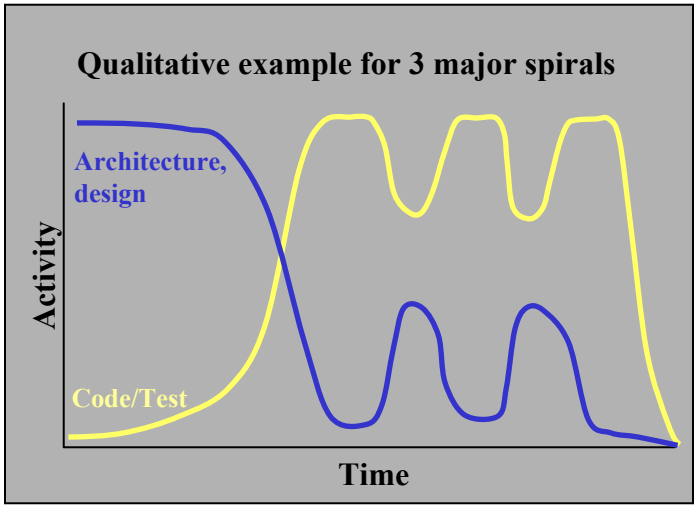
Team



- Small effective group
- Very experienced
- Excellent track record
- Employ highly interactive development process
- All members are expert in LAT architecture, able to contribute in many areas
- Leads are highly qualified scientists
- Leads are also developers
- Independent oversight provided by systems engineering
- Produce fully documented design
- Process allows/requires software to be in use from early subsystem development/testing to full LAT verification

Development Process

- Initial design effort
  - Define hardware interfaces and architecture
  - Build stable development infrastructure
  - Generate high-level requirements (SRS) that capture scope of project
  - Generate high-level design that captures basic architecture and interfaces



- For each FSW release
  - Generate detailed design of new functionalities
  - Employ iterative design/code/test process to converge on the detailed design ("little spirals")
    - Allows experienced developer to proceed more rapidly to explore the design parameter space, discover issues, and resolve them
    - Ultimately produces a more optimal design than one selected in advance based only on analysis and limited data
    - Extensive documentation of resulting code is produced as it is built
    - Iterative process is a continuous rapid prototyping cycle that supports higher productivity and a higher quality final product

Code Management

- **FSW partitioned into functional blocks based on the SRS**
  - **Functional blocks are then mapped into packages, the fundamental unit of the code management system**

Common code – SIU and EPU

PACKAGE	DESCRIPTION	LOC	RISK FACTOR	CONTINGENCY
PBS	Basic Services	1800	1,2	75
FMP	File Management	1500	3	450
CHP	CPU Housekeeping	1000	3	300
SWD	Software Watchdog	1000	3	300
LIO	LAT LCB I/O driver	3000	5	1500
HUT	Histogrammer	1750	3	525
SSR	SSR services	1000	5	500
SDF	SIU Diag Framework	1000	10	1000
TOTALS		**12050**		**4650**

EPU specific code

PACKAGE	DESCRIPTION	LOC	RISK FACTOR	CONTINGENCY
EDP	Event Dispatch	2100	3	700
EOP	Event Output	3750	3	1125
EMP	Event Monitoring	3500	2	700
ECL	Calibration (client)	4950	5	2475
ECP	Command/Control	3400	3	1020
SOP	Event output	1250	2	250
EFP	Event Filtering	10000	5	1000
TOTALS		**28950**		**7270**

Test and verification code

PACKAGE	DESCRIPTION	LOC	RISK FACTOR	CONTINGENCY
FES	Front end simulator	5600	3	1680
LTX	Test executive	5200	5	2400
TOTALS		**10800**		**4080**

*See next slide for discussion of contingency

SIU specific code

PACKAGE	DESCRIPTION	LOC	RISK FACTOR	CONTINGENCY
GNAT	LAT DAQ cmd/resp	1550	1	155
GCFG	DAQ configuration	5850	1,3	925
LCP	LAT commanding/1553	3600	2	360
SMP	Event output	3100	3	930
SCL	Calibration (server)	3200	5	1600
HSK	Housekeeping	6350	3	1905
THP	Trend/bounds check	1500	2	300
MCP	Mode control	1300	3	390
GPS	GPS services	800	3	240
LAP	SC attitude services	1300	3	390
GBM	Response to GBM data	1550	3	465
GRB	GRB detection	2400	3	720
TCS	Thermal Control	2000	5	1000
TOTALS		**34500**		**9380**

Boot code

PACKAGE	DESCRIPTION	LOC	RISK FACTOR	CONTINGENCY
REV	Reset/exceptions	400	2	40
MEM	Memory test	100	1	10
BSH	Boot shell	1000	3	300
EDV	EEPROM driver	100	1	5
PCI	PCI driver	300	0	0
CCSDS	CCSDS formatter	400	0	0
UPL	Upload parser	1000	3	300
ELF	ELF dynamic loader	500	0	0
ZLIB	ZLIB integration	40	0	0
BUT	Boot Utilities	200	0	0
LCB	LCB driver (polled mode)	400	5	200
CO1553	1553 driver (polled mode)	400	0	0
TOTALS		**4840**		**855**

Contingency

- Document: LAT-TD-01781
- LOC count estimated for each package
  - Bottoms up estimate
  - Based on package content
  - Based on previous experience
- LOC estimates not worst-case
  - Represent most likely length of package
  - Some longer or more complex, some shorter or less complex
  - Total LOC for entire FSW load expected to be more static than individual package estimates

RISK FACTOR	CRITERIA
0	Written
1	Significant coding already complete, also testing or previous experience (e.g. balloon flight)
2	Partial coding already complete, also limited or very well defined scope
3	Well understood scope, possibly some coding completed
5	Scope partially undefined, limited previous experience or high complexity
10	Scope poorly defined

- Contingency estimation based on risk factor
  - Risk factor defined in table above
  - Contingency calculated by multiplying the risk factor by 10% of total estimated LOC in package
  - Contingency represents potential additional lines of code

Releases

- **LAT FSW strategy calls for major FSW releases to coincide with the natural hardware builds as follows:**
  - **R1 – Engineering Model 1 (8/1/03)**
    - **Single tower, single CPU**
  - **R2 – Engineering Model 2 (1/1/04)**
    - **Multiple towers (single tower plus front-end simulators for additional towers), GASU*, single CPU**
  - **R3 – Full LAT (9/1/04)**
    - **Complete set of 16 towers, GASU*, full set of CPU's**

* **GASU includes LAT Global Trigger (GEM), ACD Electronics Module (AEM), LAT Command Response Unit (CRU) and Event-Builder (EB)**

EM1 Release

- Hardware
  - 1 Partially populated tower
  - 1 Tower Electronics Module
  - 1 COTS CPU (VME)
    - Ethernet
    - Serial port
    - LCB communications
      - Command/response
      - Event acquisition

Status:

Development complete against preproduction electronics

Deployed to field in I&T test stands

- Software
  - Interfaces (other than VxWorks)
    - LCB command/response
    - LCB event acquisition
  - TEM configuration setting and read-back
    - Write to and read from all tower registers
    - CAL, TKR, TEM
  - Format and export event data from tower
  - Charge injection calibration
    - Inject a known charge signal directly into the (TKR, CAL) electronics in lieu of the detector output
    - Read the resulting event data output
  - Sample and collect a subset of tower / TEM housekeeping and LRS data
  - Continue EPU filter development and testing separately on desktop machine

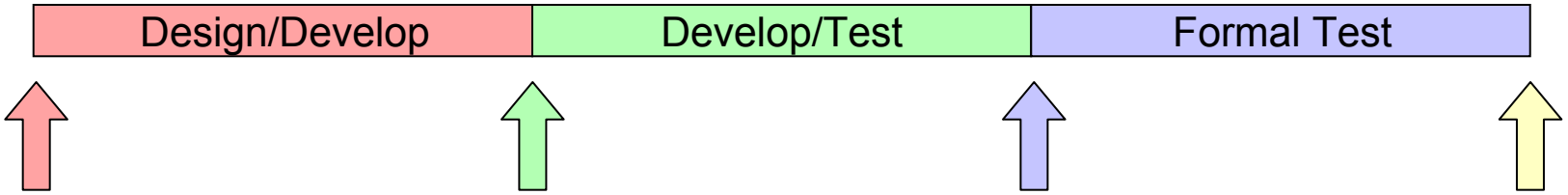
EM2 Release

- Hardware
  - Multiple towers (single tower plus FESs)
  - Multiple TEMs
  - GASU (or simulation)
    - Command Response Unit (CRU)
    - Event Builder Module (EBM)
    - ACD Electronics Module (AEM)
    - Global Trigger Electronics Module (GEM)
  - 1 COTS “SIU/EPU” CPU (cPCI)
    - Ethernet
    - Serial port
    - SIB
    - LCB
- Software
  - All of EM1 functionality
  - Multiple tower capabilities
  - AEM configuration
  - AEM event acquisition
  - Capability to inject marker events into event streams to provide notice of filter parameter changes
  - LAT mode transitions
    - Engineering and safe modes
  - LAT spacecraft interface
    - 1553
    - Command and telemetry
  - File management system
  - “Desktop” EPU for filter testing and troubleshooting

Full LAT FSW Release

- Hardware
  - All towers / TEMs
  - ACD
  - GASU
    - Command Response Unit (CRU)
    - Event Builder Module (EBM)
    - ACD Electronics Module (AEM)
    - Global Trigger Electronics Module (GEM)
  - Development on multiple engineering RAD750s to emulate flight SIU/EPUs
- Software
  - All of EM2 functionality
  - Multiple processor capabilities
    - EPU configuration by SIU
  - Spacecraft message processing
    - Attitude, time, ancillary data
  - Transient detection and reporting
  - LAT hardware power control
  - Thermal control system

A Single Development Cycle



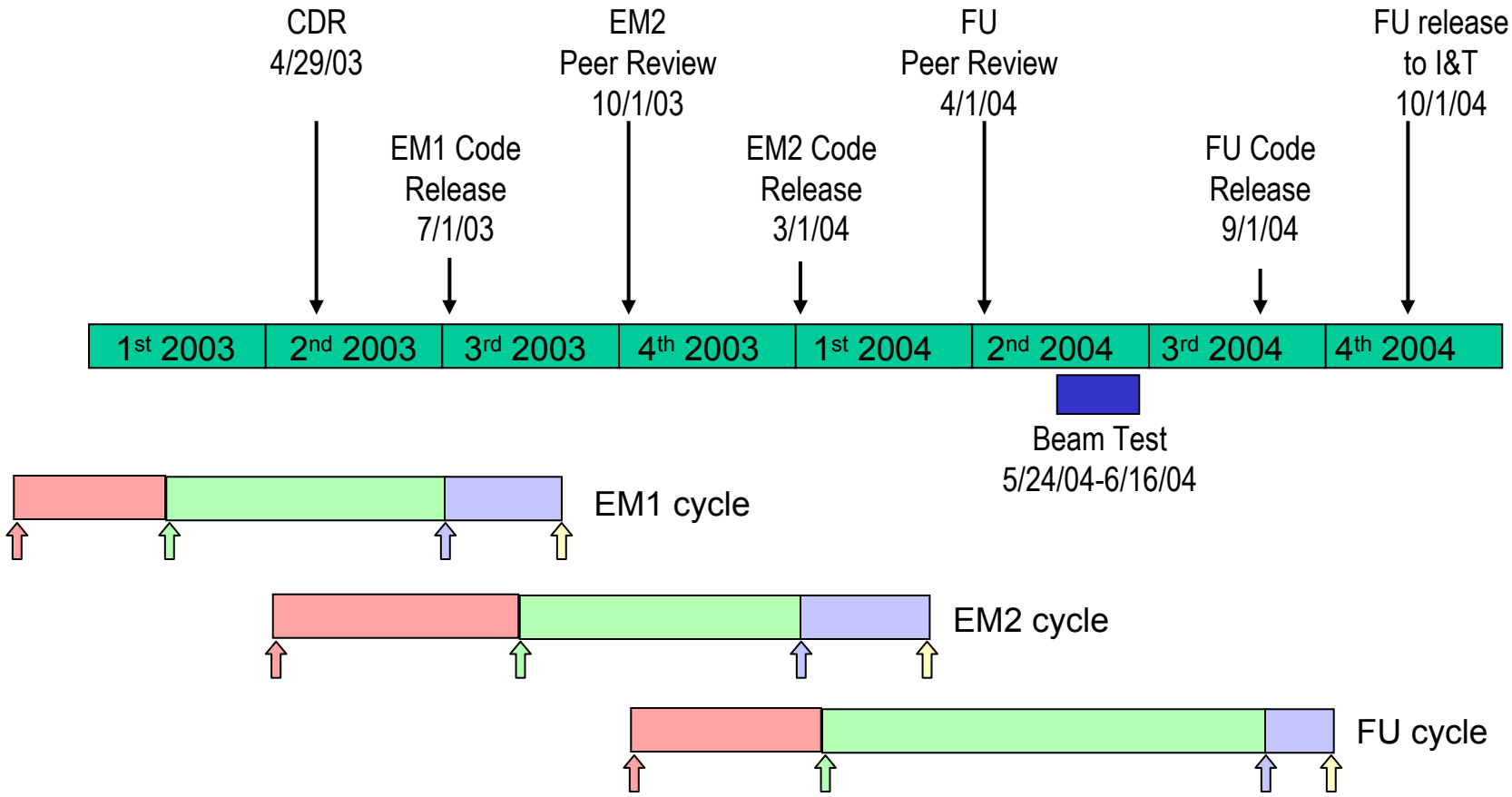
Entrance: Sufficient knowledge/documentation to start design
Activity: Start design, code small prototypes

Entrance: Target hardware becomes available
Activity: Code and test against real hardware (debug both)

Entrance: Development complete, snapshot taken (release is defined)
Activity: Test against the formal test plan

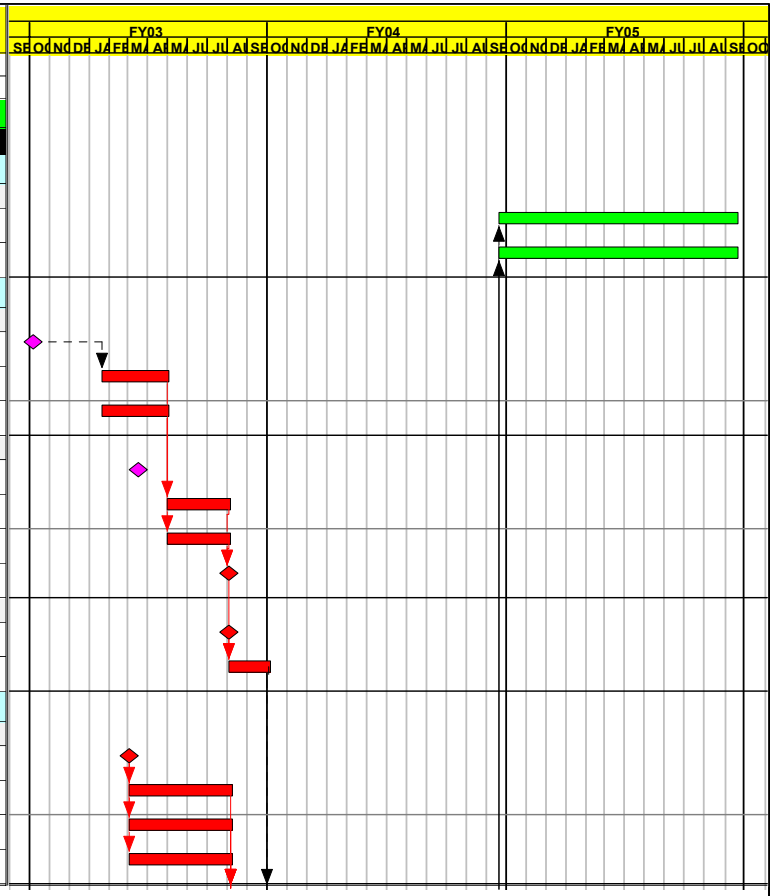
Entrance: Formal test plan completed successfully
Exit: Release to integration

Breakdown of Development Cycles



FSW Summary Schedule

Activity ID	Activity Description	Orig Dur	Early Start	Early Finish	Late Finish	Total Float
4 GLAST INSTRUMENTS						
4.1 GLAST LAT PROJECT						
4.1.7 ELECTRONICS						
4.1.7.9 FLIGHT SOFTWARE						
4.1.7.9.1 INFRA-STRUCTURE DEVELOPMENT/TEST BENCH SUPPOF						
4.1.7.9.1.1 INFRA-STRUCTURE DEVELOPMENT						
7EN7000050	FSW Support during Integration/Testing (SLAC)	247	09/21/04	09/19/05	04/05/07	380
7EN7000060	FSW Support during Integration/Testing (NRL)	247	09/21/04	09/19/05	04/05/07	380
4.1.7.9.3 ENGINEERING MODEL 1						
4.1.7.9.3.8 EM1 Code Design/Develop						
7EN9380000	iN: EM1 Hardware Specification	0		10/07/02*	01/21/03	66
7EN9381000	SIU/EPU Common Application Code	70	01/22/03*	04/30/03	04/30/03	0
7EN9382000	SIU Specific Application Code	70	01/22/03*	04/30/03	04/30/03	0
4.1.7.9.3.9 EM1 Code Develop/Test						
7EN9390000	iN: EM1 Hardware for Develop/Test (Early)	0		03/17/03*	05/07/03	37
7EN9391000	SIU/EPU Common Application Code	65	05/01/03	08/01/03	08/01/03	0
7EN9392000	SIU Specific Application Code	65	05/01/03	08/01/03	08/01/03	0
7EN9393110	AV: EM1 Final Code Release	0		08/01/03	08/01/03*	0
4.1.7.9.3.A EM1 Formal Test						
7EN93A0000	ND: EM1 Mini-Tower (from I&T)	0		08/01/03*	08/01/03	0
7EN93A1000	EM1 Formal Test	42	08/04/03	10/01/03	10/01/03	0
4.1.7.9.4 ENGINEERING MODEL						
4.1.7.9.4.C EM2 CODE DESIGN/DEVELOP						
7EN94C0000	iN: EM2 Hardware Specification	0		03/03/03*	03/03/03	0
7EN94C1000	SIU/EPU Common Application Code	108	03/04/03	08/04/03	08/04/03	0
7EN94C2000	EPU Specific Application Code	108	03/04/03	08/04/03	08/04/03	0
7EN94C3000	SIU Specific Application Code	108	03/04/03	08/04/03	08/04/03	0



Start Date 04/03/00
Finish Date 04/05/07
Data Date 06/01/02

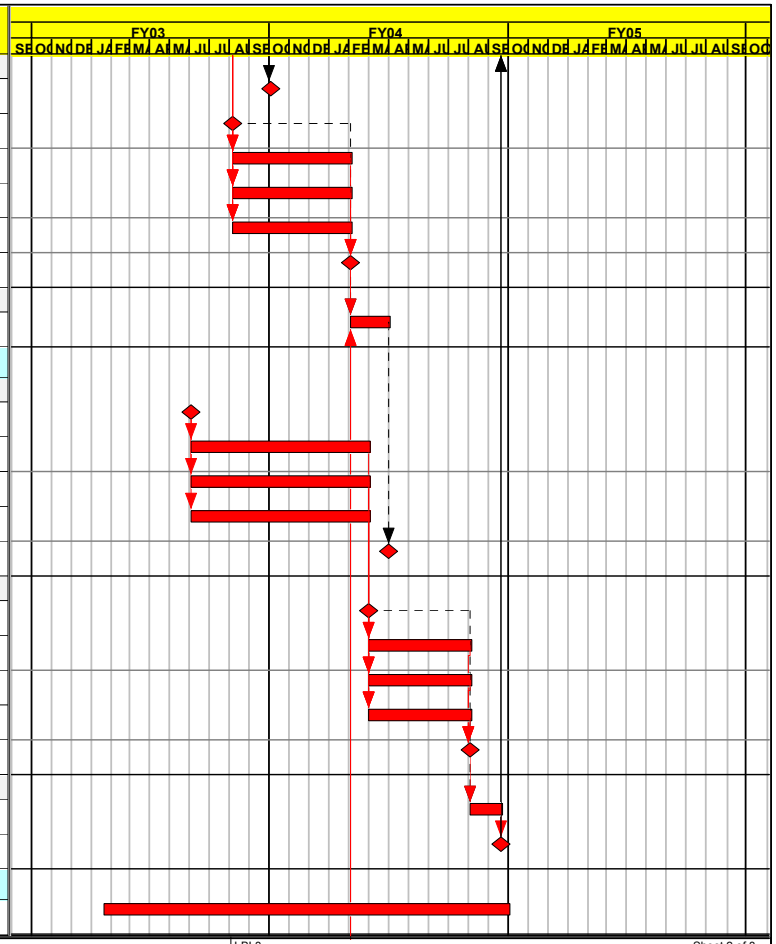
FSW SCHEDULE

LBL3 Sheet 1 of 3

Gamma Ray Large Area Space Tele
FSW Schedule

FSW Summary Schedule (cont.)

Activity ID	Activity Description	Orig Dur	Early Start	Early Finish	Late Finish	Total Float
4.1.7.9.4.D EM2 CODE DEVELOP/TEST						
7EN94D0000	EM2 Peer Review	0		10/01/03*	10/01/03*	0
7EN94D0010	iN: EM2 Hardware for Develop/Test (Early)	0		08/04/03*	08/04/03	0
7EN94D1000	SIU/EPU Common Application Code	119	08/05/03	02/02/04	02/02/04	0
7EN94D2000	EPU Specific Application Code	119	08/05/03	02/02/04	02/02/04	0
7EN94D3000	SIU Specific Application Code	119	08/05/03	02/02/04	02/02/04	0
7EN94D4010	AV: EM2 Final Code Release	0		02/02/04	02/02/04	0
4.1.7.9.4.E EM2 FORMAL TEST						
7EN94E1000	EM2 Formal Test	42	02/03/04	04/01/04	04/01/04	0
4.1.7.9.6 FLIGHT UNIT						
4.1.7.9.6.1 FU CODE DESIGN/DEVELOP						
7EN9610000	iN: Flight Code Inputs Available	0		06/02/03*	06/02/03	0
7EN9611000	SIU/EPU Common Application Code	182	06/03/03	03/01/04	03/01/04	0
7EN9612000	EPU Specific Application Code	182	06/03/03	03/01/04	03/01/04	0
7EN9613000	SIU Specific Application Code	182	06/03/03	03/01/04	03/01/04	0
7EN9614100	FU Peer Review	0		04/01/04*	04/01/04*	0
4.1.7.9.6.2 FU CODE DEVELOP/TEST						
7EN9620000	iN: Flight Hardware for Develop/Test (Early)	0		03/01/04*	03/01/04	0
7EN9621000	SIU/EPU Common Application Code	108	03/02/04	08/02/04	08/02/04	0
7EN9622000	EPU Specific Application Code	108	03/02/04	08/02/04	08/02/04	0
7EN9623000	SIU Specific Application Code	108	03/02/04	08/02/04	08/02/04	0
7EN9624100	iA: FU Code Release	0		08/02/04	08/02/04	0
4.1.7.9.6.3 FU FORMAL TEST						
7EN9631000	FU Formal Test	34	08/03/04	09/20/04	09/20/04	0
7EN9634000	AV: FU Final Code Release to I&T	0		09/20/04	09/20/04*	0
4.1.7.9.7 Science/Spacecraft						
7EN9700000	Science/Spacecraft	424	01/22/03*	09/30/04	09/30/04	0



Start Date 04/03/00
Finish Date 04/05/07
Data Date 06/01/02

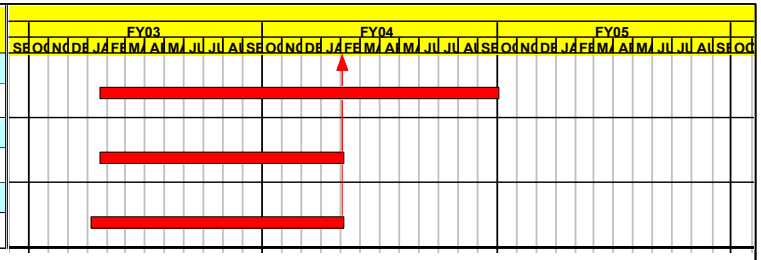
FSW SCHEDULE

LBL3 Sheet 2 of 3

Gamma Ray Large Area Space Tele
FSW Schedule

FSW Summary Schedule (cont.)

Activity ID	Activity Description	Orig Dur	Early Start	Early Finish	Late Finish	Total Float
4.1.7.9.8 FLIGHT CPU BOOTIN(						
7EN9800000	Flight CPU Booting	424	01/22/03*	09/30/04	09/30/04	0
4.1.7.9.9 FRONT END SIMULATOR						
7EN9900000	Front End Simulator	255	01/22/03*	02/02/04	02/02/04	0
4.1.7.9.A TEST EXECUTIVE						
7EN9A00000	Test Executive	264	01/08/03*	02/02/04	02/02/04	0



Start Date 04/03/00
Finish Date 04/05/07
Data Date 06/01/02

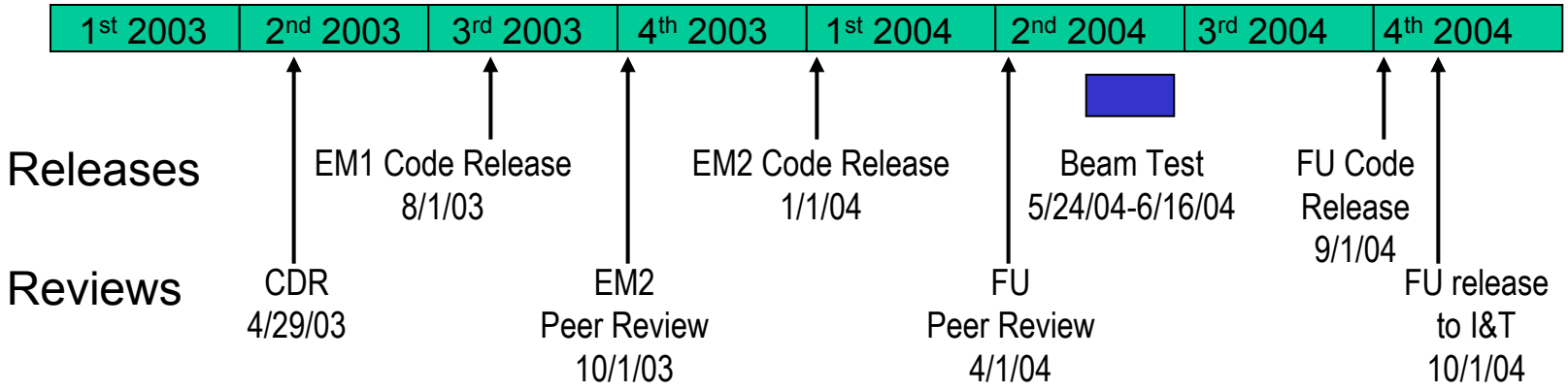
FSW SCHEDULE

LBL3 Sheet 3 of 3

Gamma Ray Large Area Space Tele
FSW Schedule

Milestones

- **Detailed FSW development plan, schedule, and reviews are part of LAT PCMS, down to the task level (WBS 4.1.7.9)**
- **Plan identifies milestones for progress assessment**



- **LAT CDR will serve as review of high-level FSW design and detailed EM1 design**
- **Incremental milestones for each package completion**
  - **Detailed in FSW Development Schedule**
  - **Will additionally be tracked and discussed in**
    - **Weekly LAT-wide project meetings with discussion of each sub-system**
    - **LAT Project Weekly Report**
    - **Monthly LAT-wide PMCS reviews: system-specific past month's accomplishments, plans for following month, risk evaluation, cost and schedule review of last month's scheduled and budgeted versus actual accomplishments**

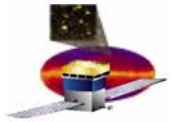
Resource Profile

- Personnel resources
  - SLAC: 6 FTE
  - NRL: 2 FTE (Dan Wood plus two additions)
    - Brian Davis (20%): extensive experience with software requirements and engineering as well as code development
    - Ray Caperoon (80%): coming to us from SECCHI with a background in RAD750 programming for that program
- Period of performance
  - 19 months currently shown until LAT Pre-Ship Review
  - Assume 18 months available for FSW development
- Overhead
  - Schedule assumes
    - LAT FSW Team Leads – 20% maximum
    - LAT FSW Team (SLAC) – 10% maximum
    - LAT FSW Team (NRL) – 15% maximum
    - Above figures reflect levels from previous experiments

Cost by Fiscal Year

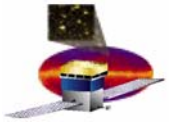
- **Flight Software without contingency**

FY01 in K$	FY02 in K$	FY03 in K$	FY04 in K$	FY05 in K$	Total in K$
70	223	935	713	743	2,684



FSW Documentation

Document	Title	Version	Status	Comment
Specifications				
433-SPEC-0001	Level 2(a): Mission System Specification			
LAT-SS-00010	Level 2(b): LAT Instrument Performance Specification	2	CM	
LAT-SS-00019	Level 3: T&DF Subsystem Specification	2	CM	
LAT-SS-00284	Level 4: Trigger Specifications	0	CM	
LAT-SS-00285	Level 4: Dataflow Specifications	0	CM	
LAT-SS-00399	Level 4: Software Requirements Specifications (SRS)	1	CM	Release prior to CDR
Introductory Documents				
LAT-SS-00287	Conceptual Design of the Electronics, T&DF System	0	PDR	
LAT-TD-00458	GLAST LAT Electronics, DAQ, Flight Software Preliminary Design Report	1	PDR	
LAT-TD-00518	Preliminary Design Report (See 458)	1	PDR	
LAT-TD-331	LAT Flight Software Preliminary Design Report	0	PDR	
External Interface Documents				
GSFC-433-IRD	LAT-SC Interface Control Document			
LAT-SS-00363	ACD-DAQ Interface Specifications	4	CM	
LAT-SS-00238	CAL-DAQ Interface Specifications	4	CM	
LAT-SS-00176	TKR-DAQ Interface Specifications	1	CM	
LAT-SS-00467	CAL-AFEE-TEM Interface Control Document	1	CM	
Software ICDs				
LAT-TD-00860	LAT Communication Board (LCB) Programming ICD	2	100%	Release prior to CDR
LAT-SS-01543	Power Distribution Module Programming ICD Specifications	0	50%	Release prior to CDR
LAT-TD-00639	ACD Electronics Module Programming ICD Specifications	1	90%	Release prior to CDR
LAT-TD-00605	Tower Electronics Module - A Primer ICD Specification	1	100%	Release prior to CDR
LAT-TD-01545	Global Trigger Programming ICD Specification	0	100%	Release prior to CDR
LAT-TD-01546	Event Builder Programming ICD Specification	0	90%	Release prior to CDR
LAT-TD-01547	Command Response Unit Programming ICD Specification	0	90%	Release prior to CDR



FSW Documentation (cont.)

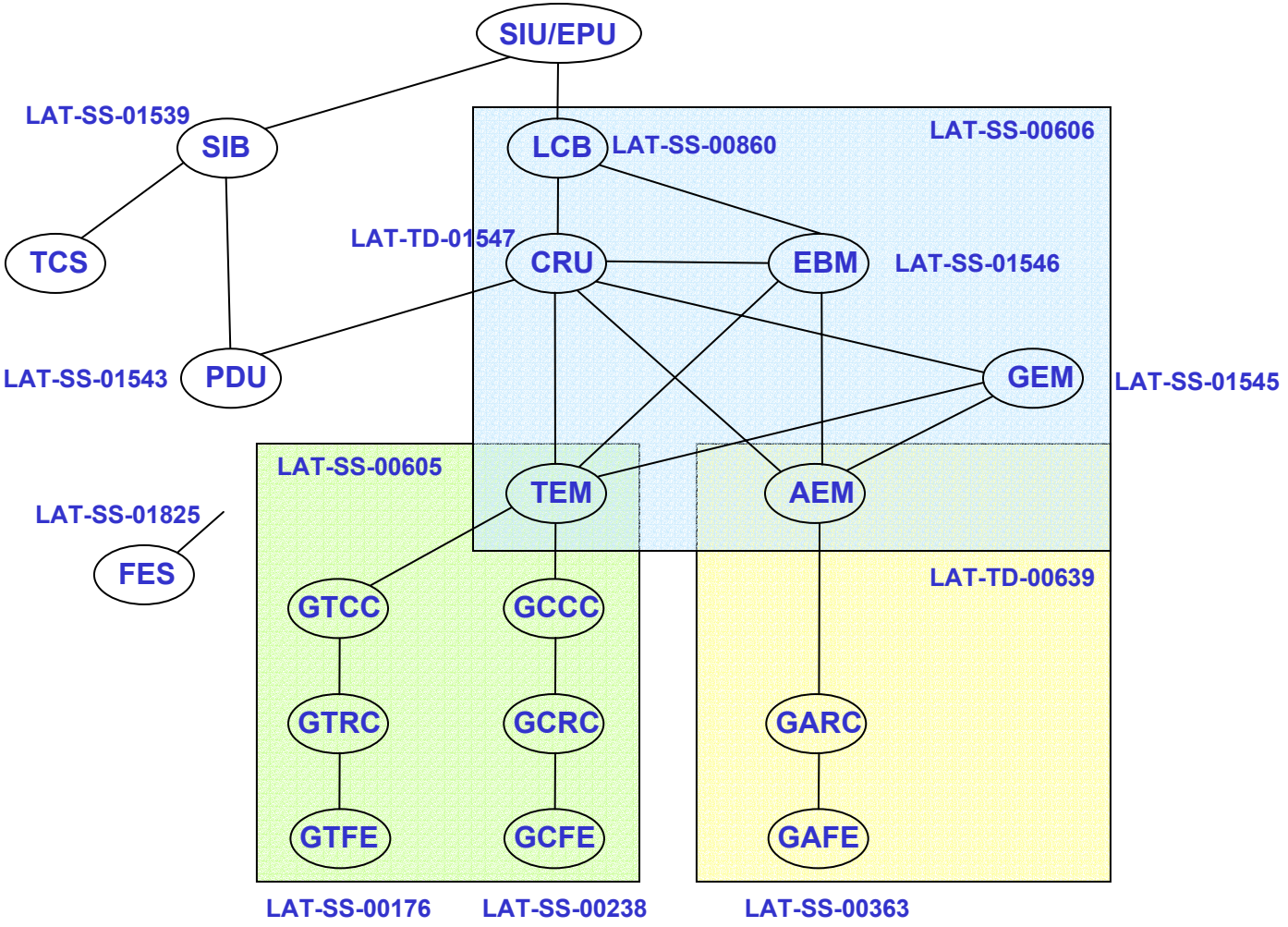
Document	Title	Version	Status	Comment
ICDs				
LAT-SS-01539	LAT Spacecraft Interface Board (SIB) ICD Specifications	0	100%	Release prior to CDR
LAT-SS-01538	LAT Crate Power Supply ICD Specifications	0	100%	Release prior to CDR
LAT-SS-01540	LAT Crate Backplane ICD Specifications	0	100%	Release prior to CDR
LAT-SS-00169	Conceptual Design and Specification of the GLAST Tracker Front-End Electronics (GTFE) ASIC	4	CM	
LAT-SS-00170	Conceptual Design of the GLAST Tracker Readout Controller Electronics (GTRC) ASIC	0	CM	
LAT-TD-01550	Global Tracker Cable Controller (GTCC) ASIC ICD	0	10%	Release prior to CDR
LAT-DS-00087	Conceptual Design of the GLAST Calorimeter Front-End Electronics (GCFE) ASIC	3	CM	
LAT-SS-00208	Conceptual Design of the GLAST Calorimeter Readout Control (GTRC) ASIC	0	CM	
LAT-TD-01549	Global Calorimeter Cable Controller (GCCC) ASIC ICD	1	50%	Release prior to CDR
LAT-TD-01548	Global Trigger Integrated Circuit (GTIC) ASIC ICD	2	Draft	Release prior to CDR
Support Equipment Documents				
LAT-TD-00861	EGSE Test-stand Architecture Redux	1	100%	Release prior to CDR
LAT-TD-00862	EGSE Test-stand Update	1	100%	Release prior to CDR
LAT-TD-00593	EGSE LAT COMM IO Board Response FIFO	4	Draft	Release prior to CDR
LAT-TD-01824	Front-End Data Simulator Description		40%	Release prior to CDR
LAT-TD-01825	Front-End Data Simulator Programming ICD		40%	Release prior to CDR
Plans and Management Documents				
LAT-MD-00104	Flight Software Management Plan	0	CM	Release prior to CDR
LAT-TD-00786	Flight Software Test Plan	0	CM	Release prior to CDR
LAT-PR-01535	Flight Software Development Plan	1	100%	Release prior to CDR
LAT-TD-01826	DAQ/FSW Test/Verification Plan			

FSW Documentation (cont.)

Document	Title	Version	Status	Comment
Other Relevant Documents				
LAT-SS-00286	Global Trigger Description	0	100%	Release prior to CDR
LAT-TD-00606	LAT Intermodule Communication	1	100%	Release prior to CDR
LAT-TD-01380	LAT Communication Board Driver - SW Architecture and Interfaces	2	Draft	Release prior to CDR
LAT-SS-00461	LAT TEM-GASU to CPU Data Formats	1	100%	Release prior to CDR
LAT-TD-01536	LAT ICD for Start-up Procedures	0	100%	Release prior to CDR
LAT-SS-00890	LAT Instrumentation ICD		100%	Release prior to CDR
LAT-TD-00712	LAT Auxiliary Data Survey	0	Draft	Release prior to CDR
LAT-SS-00715	Thermal Control System ICD	0	Draft	Release prior to CDR
LAT-TD-01553	Instrument Damage Protection against LAT Processor Hardware or Software Malfunction	0	90%	Release prior to CDR
LAT-TD-00863	LAT Custom Processor Specifications	1	Draft	
LAT-TD-01781	LAT Flight Software Package Descriptions and LOC Basis of Estimate	0	100%	
	CMX Manual	0	Draft	
LAT-TD-01806	SIU Boot Code	0	90%	
	CCSDS Packet Library User Manual*	0	Draft	
	SIU 1553 Drivers*	0	Draft	
	Telecommand and Telemetry Formats*	0	Draft	
LAT-TD-01121	LAT DAQ Trigger and Dataflow Resource Usage		100%	
LAT-SS-01597	Configuration Data: Storage and Transmission	0	90%	
LAT-SS-00xxx	Software/Algorithm Design Document			EM1 Release

* Documents produced at NRL and not yet entered into CyberDocs

FSW ICD Tree


SIU/EPU
LAT-SS-01539
SIB
LCB
LAT-SS-00860
LAT-SS-00606
TCS
LAT-TD-01547
CRU
EBM
LAT-SS-01546
LAT-SS-01543
PDU
GEM
LAT-SS-01545
LAT-SS-00605
LAT-SS-01825
TEM
AEM
FES
LAT-TD-00639
GTCC
GCCC
GTRC
GCRC
GARC
GTFE
GCFE
GAFE
LAT-SS-00176
LAT-SS-00238
LAT-SS-00363

Risk

- LAT instrument FSW not critical to mission safety
  - No LAT commands or FSW actions can result in damage to hardware
  - All relevant hardware has built-in self-protection
    - Current limiting protects PMTs during SAA if HV reduction not performed in advance by ground command or FSW action
- LAT instrument FSW supports mission success
  - Extensive ground testing (as with balloon flight) prior to flight
  - Use of FSW for electronics and system level testing to achieve more user hours by non-developers
  - Reprogrammability
    - Fully reprogrammable on orbit except for small amount of primary boot code
    - Primary boot code being treated as critical code

Changes Since PDR

- Processor selection
  - BAE RAD750 has become baseline processor
  - Number of processors has been determined
    - 2 SIU (1 cold spare)
    - 3 EPUs (2 active, 1 cold spare)
  - SIU and EPU crates now look alike
- Event Builder has become part of GASU
  - Some SIU code has migrated to EPU or common code
  - SSR is now a node on event fabric

Resource Usage Monitoring

Resource	Available	Used	Margin Factor
SIU Boot Prom	256 KBytes	128 KBytes	2
EPU Boot Prom	256 KBytes	128 KBytes	2
SIU EE Prom	4 MBytes	1.5 - 2.5 MBytes	1.5 - 2.5
EPU EE Prom	4 MBytes	1 - 2 MBytes	2-4
SIU DRAM Code/Data	128 MBytes	4–8 / 32-96[1] MBytes	1.25 - 3
EPU DRAM Code/Data	128 MBytes	4–6 / 32-96[1] MBytes	1.25 - 3
SIU CPU Cycles	100% in 1 CPU	25%	4
EPU CPU Cycles	200% in 2 CPUs	30 - 50%	4 - 6
XEM-to-CPU Bandwidth	20.0 MBytes/sec	10.0 MBytes/sec[2]	2
CPU-to-CPU Bandwidth	2.5 MBytes/sec	50.0 KBytes/sec[2]	50
CPU-to-SSR Bandwidth	5.0 MBytes/sec	40.0 KBytes/sec[2]	125

[1] **Data memory usage is largely a function of how much monitoring data is kept. This is a soft requirement that can be adjusted before and during flight.**

[2] **Physics Data Taking Mode**

Table assumes 1 active SIU (1 cold spare), 2 active EPUs (1 cold spare)
All CPUs BAE RAD750s (133 MHz, 128 MB memory, 256 kB on board PROM for primary boot)