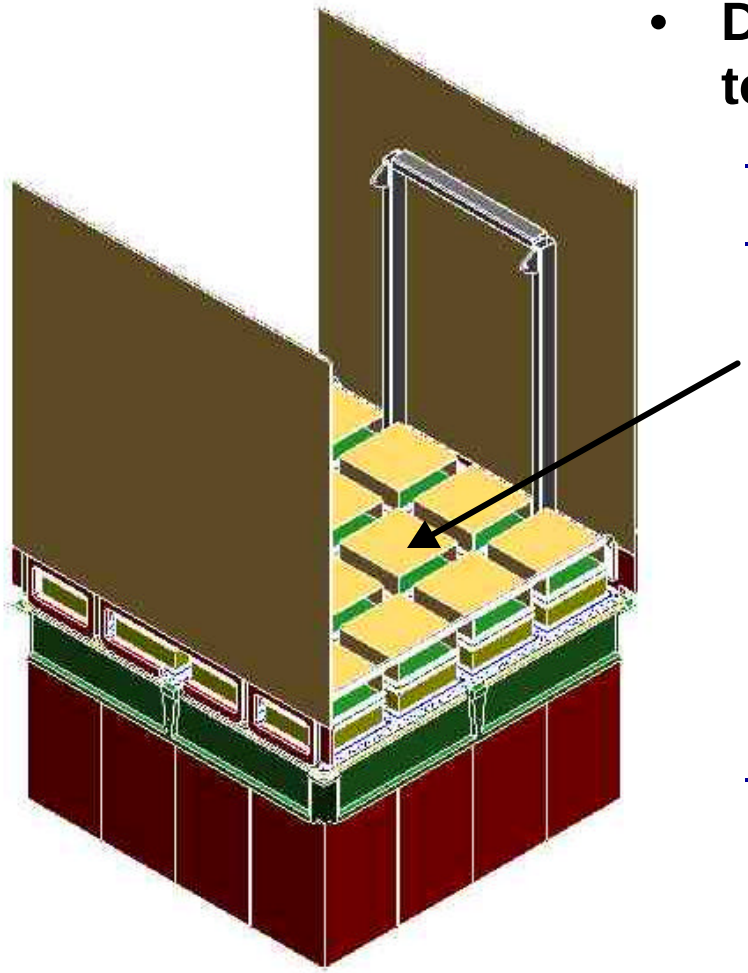
T&DF Modules

Gunther Haller
Stanford Linear Accelerator Center

Location of Modules

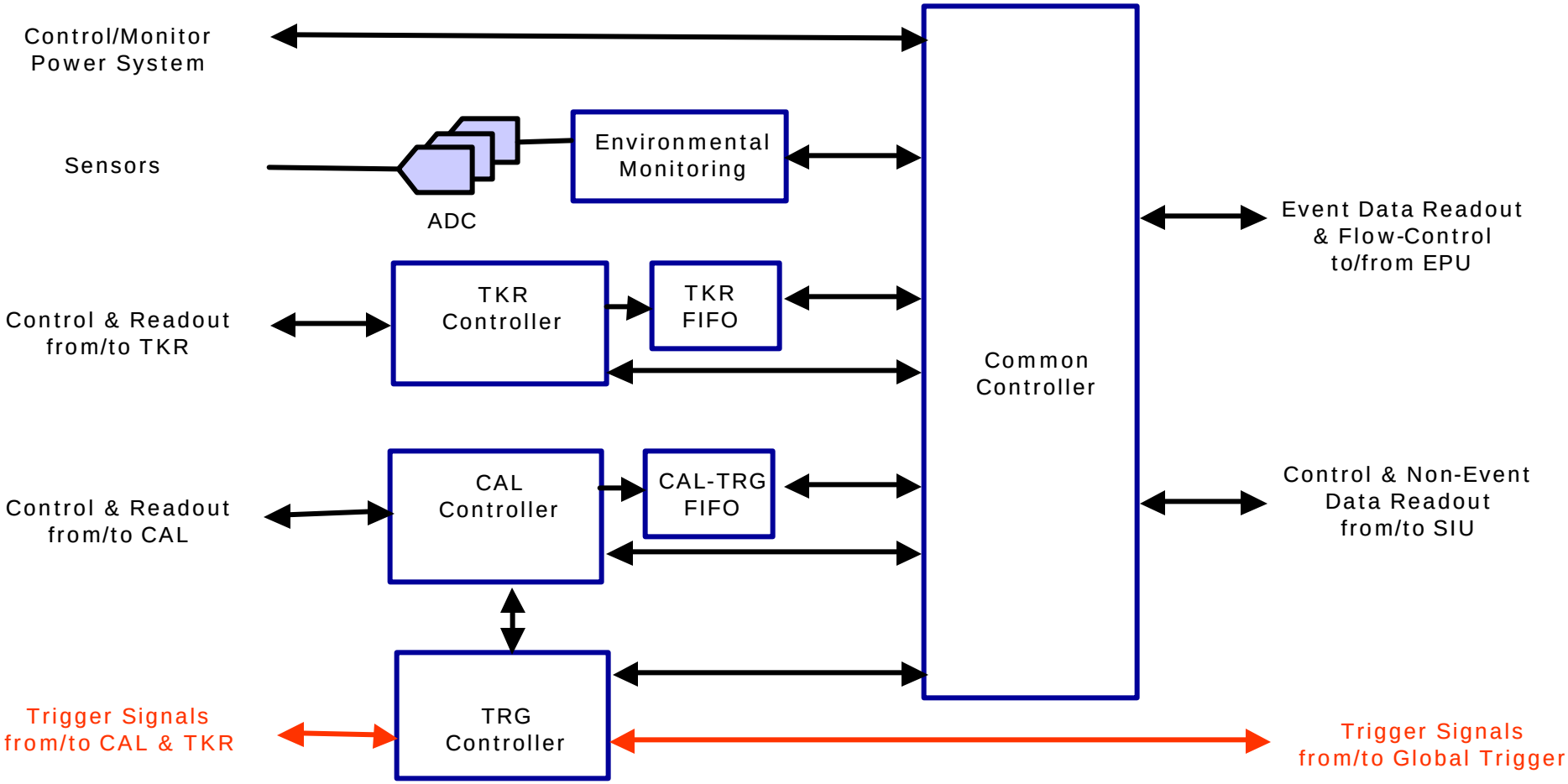


- Distributed in boxes under the 16 towers (LAT shown upside-down):
  - 1st level: TEMs (16 locations)
  - 2nd level
    - Event Processor Units (5)
    - Spacecraft Interface Units (2)
    - Global Trigger Modules (2)
    - Interconnection Modules (2)
    - ACD Modules (2)
    - Power Distribution Modules (2)
  - 3rd level: Power Supply boxes (16)

Flight Modules Deliverables

- 16 (+ 1) TKR-CAL Tower Electronics Modules
- 2 (+ 1) ACD Electronics Modules
- 2 (+ 1) Global Trigger Modules
- 2 (+ 1) Interconnection Modules
- 2 (+ 1) Monitoring Modules
- 5 (+ 1) Event Processor Units
  - LAT-EP communication card
  - Processor Card
  - Backplane
- 2 (+ 1) Spacecraft Interface Units
  - LAT-SIU communcation card
  - Processor Card
  - SC-SIU communication card
  - Backplane
- Need to revisit “spare” numbers

TKR-CAL Tower Electronics Module (1)

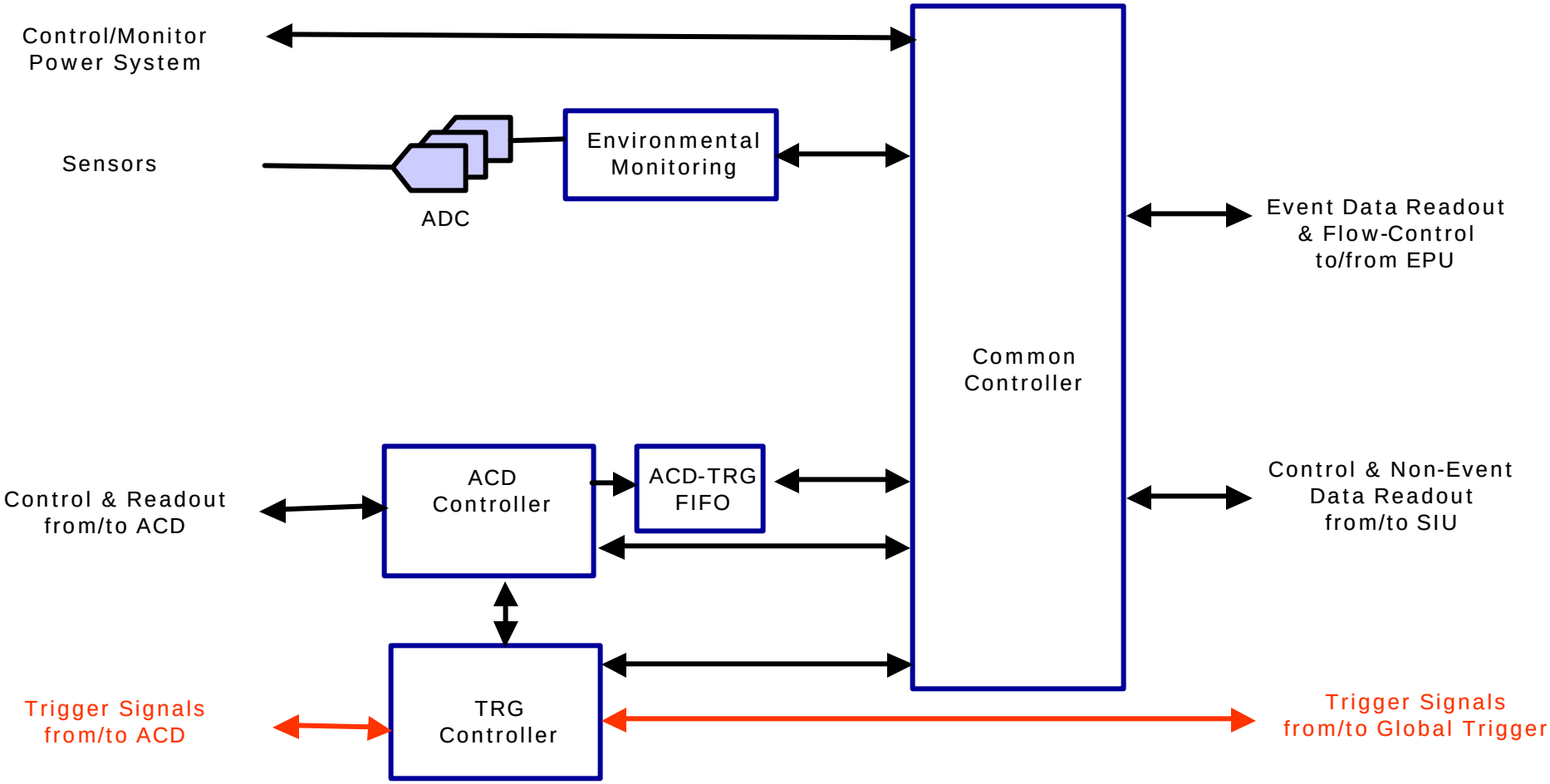


- **TRG primitive generation is contained in TRG Controller**

TKR-CAL Tower Electronics Module (2)

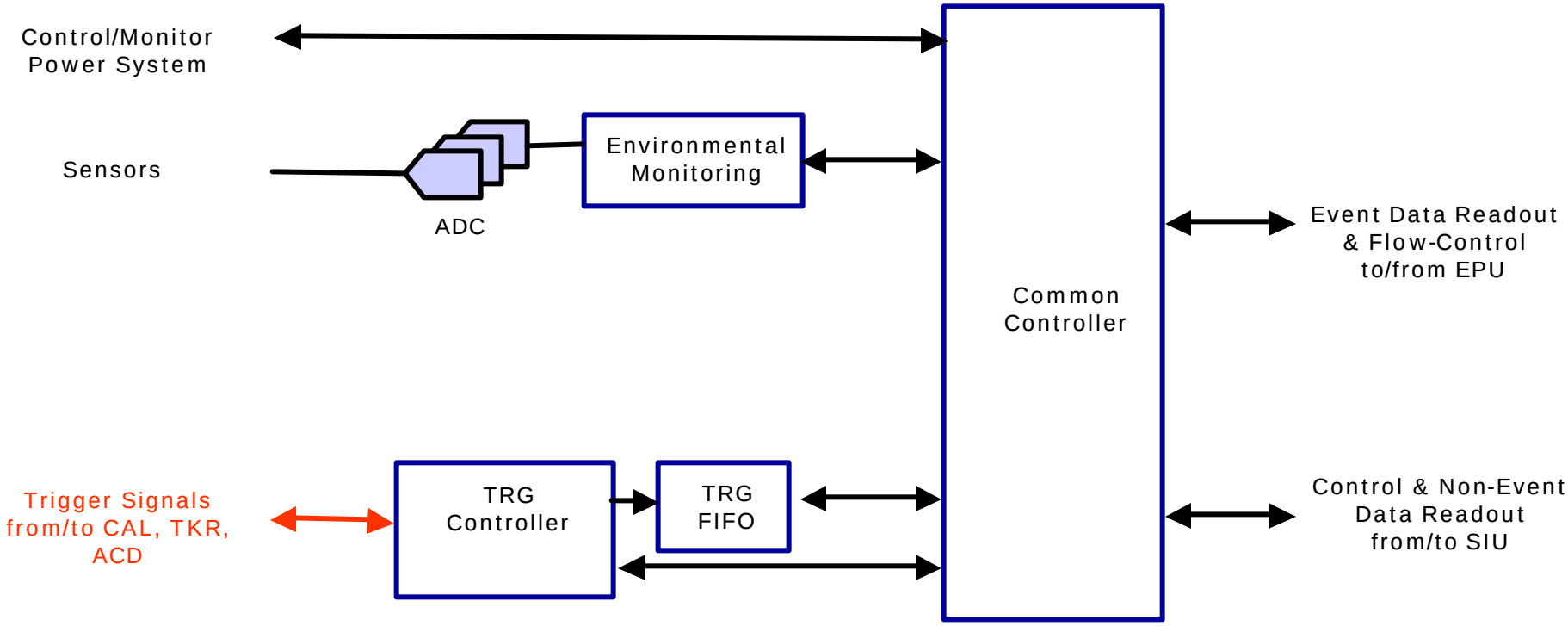
- Digitizes temperatures, voltages, currents, formats data for readout to SIU
- Receives commands from SIU, forwards the commands to TKR, CAL, TRG, or environmental block
- Receives trigger inputs from front-ends and generates trigger primitives, transmits them to GLT
- Receives TACK from GLT system, sends all necessary signals to sub-systems
- Controls acquisition of data from the front-ends, reformats, log-surpresses (CAL), and moves the data into TEM event buffers (FIFO's)
- Builds TEM events from CAL, TKR, TRG data and transmits event to EPU's.

ACD Electronics Module



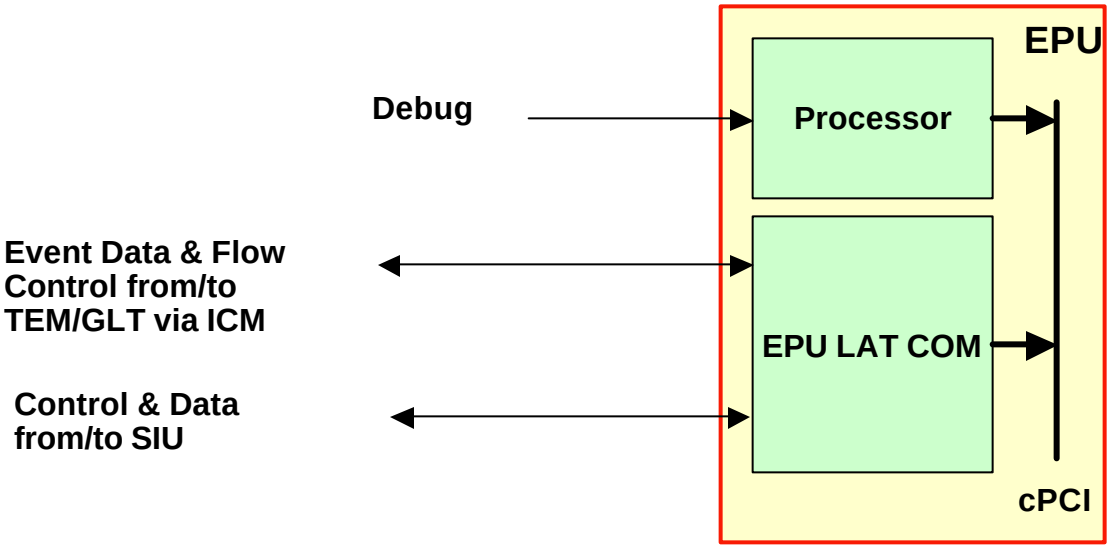
- **TRG primitive generation is contained in TRG Controller**

Global Trigger Electronics Module



- **Global trigger logic is contained in TRG Controller**

Event Processor Unit



- SIU LAT communication card contains
  - Event data & flow control interface to TEM's, ACD EM, GLT (via Interconnection module)
  - Control & Data communication with SIU
- ICM and SIU communciation blocks may be implemented in two cPCI modules, TBR
- Processor options see next slide

Processor Options

- **RAD750 From BAE Systems Is the Baseline Choice for the EPU & SIU**
- **RHPPC From Honeywell Is Also Under Consideration**
- **Adapting Recent CPU Card Designs Developed by the NRL for GLAST and NEMO Using the Temic PowerPC 603e May Be an Option If Availability or Cost Issues Dictate**

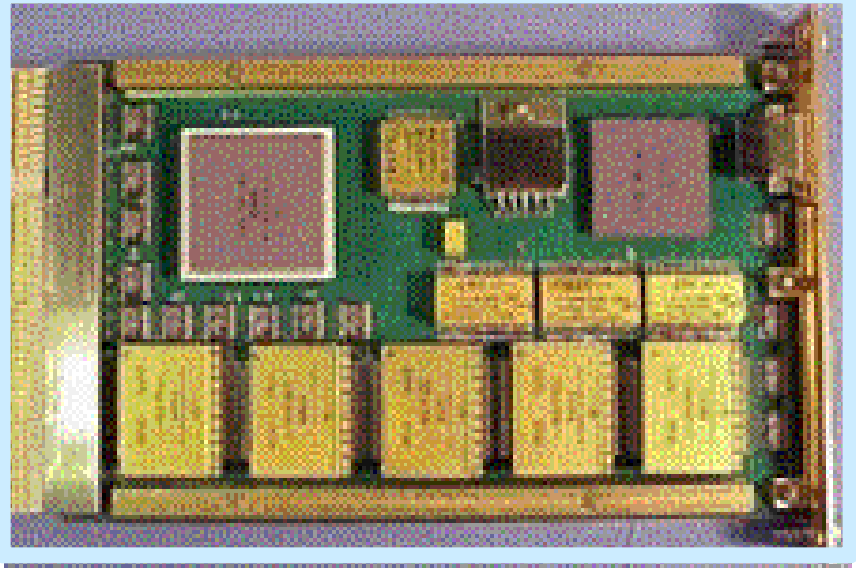
Function	RAD750	RHPPC	TCPU	Remarks
Processor	750	603e	603e	
MIPS	240	210	~140	
RAM	128MB	64MB	256MB	
EEPROM		4MB	4MB	
SUROM	256kB	512kB	64kB	
cPCI Format	3U	6U	6U VME	
1553 Bus	No	Yes	No	
Voltage	3.3	[TBR]	3.3, 5	
Power	<12W	<8W	<10W	
L1 Cache/kbytes (I/D)	32/32	16/16	16/16	

Slide provided by Greg Clifford, Silver Engineering & Michael Lovellette, Kent Wood, NRL

RAD750 Processor

- Off The Shelf Processor Card From BAE Systems
- 240 MIPS at 133 Mhz, Less Than 12W
- Total Dose > 100 kRad (Si), Latchup Immune, SEU Rate < 1E-5 Upsets/processor-day @ 90% GEO
- 3U Compact PCI Module Format
- VxWorks Operating System
- Requires EEPROM & 1553 Bus Interface To Be Included On SIU SC COM Card

PowerPC™



Courtesy: BAE Systems Inc.

Slide provided by Greg Clifford, Silver Engineering & Michael Lovellette, Kent Wood, NRL

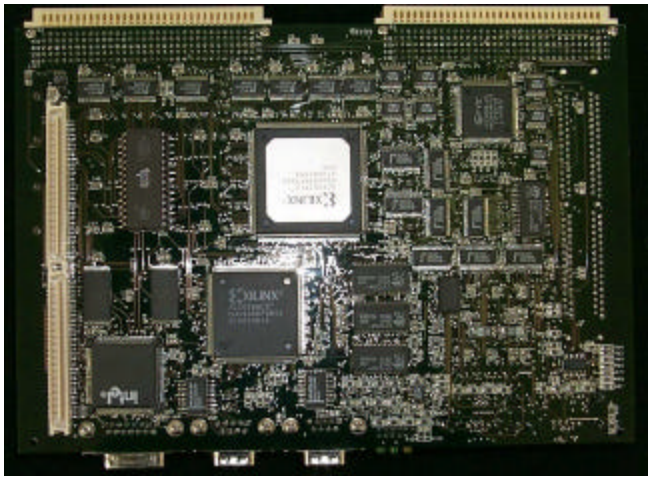
SIU Honeywell RHPPC Option

- RHPPC 150 MHz, 210 DMIPS, 16kbyte I&D Caches
- Memory With EDAC and Scrubbing:
  - 4 Mbyte Hard SRAM or 64MB SDRAM (Optional)
  - 4 Mbyte ROM or EEPROM
  - 512 Kbyte SUROM
  - 1 Mbyte L2 Cache (Parity)
- cPCI Backplane Bus (Optional Dual Configuration), 32-bit, 33 MHz
- Dual Redundant 1553B Upgrade-able to Dual Rate AS1773
- PCI Mezzanine Bus
- 6U X 160 Form Factor, 2.5 Lb., 8W (Nom)
- -40°C to 80°C Rail Temperature
- Ps>0.99, 15 Years, 35°C (With Cold Spare)
- TID >500 kRad, No SEL, SEU Rate < 3e-5/day (Adams 90 Percent WC, GEO)

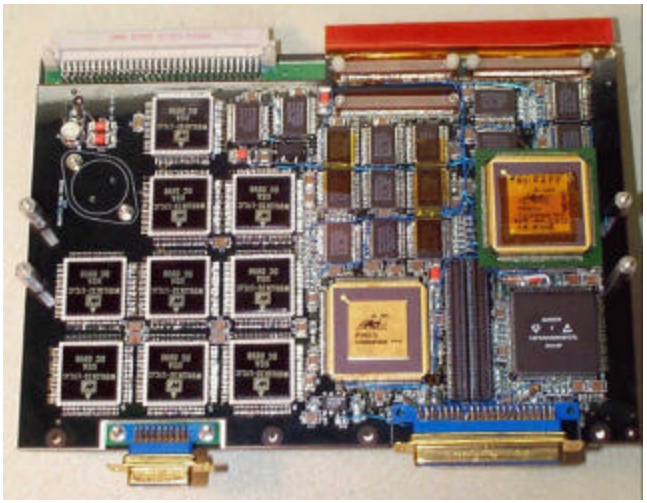
Slide provided by Greg Clifford, Silver Engineering & Michael Lovellette, Kent Wood, NRL

NRL PowerPC CPU Cards

- Two PowerPC PC603e CPU Cards Have Been Developed By NRL Over the Last 3 Years
- Both Designs Are Based On the Temic PowerPC 603e Processor
- The NEMO Program Developed and Tested a Flight Brassboard Design
  - 30krad(Si) TID, 16MB SRAM, 1553 Bus, 4MB EEPROM, VMEbus, VxWorks
- The GLAST Program Developed the Tower CPU Card, Flight Breadboard for an Advanced Design
  - L2 Cache, 256MB DRAM, 4MB Flash, 64kb SUROM, Ethernet, VMEbus, VxWorks and Linux In-process



GLAST Tower CPU Card



NEMO NPC CPU Card

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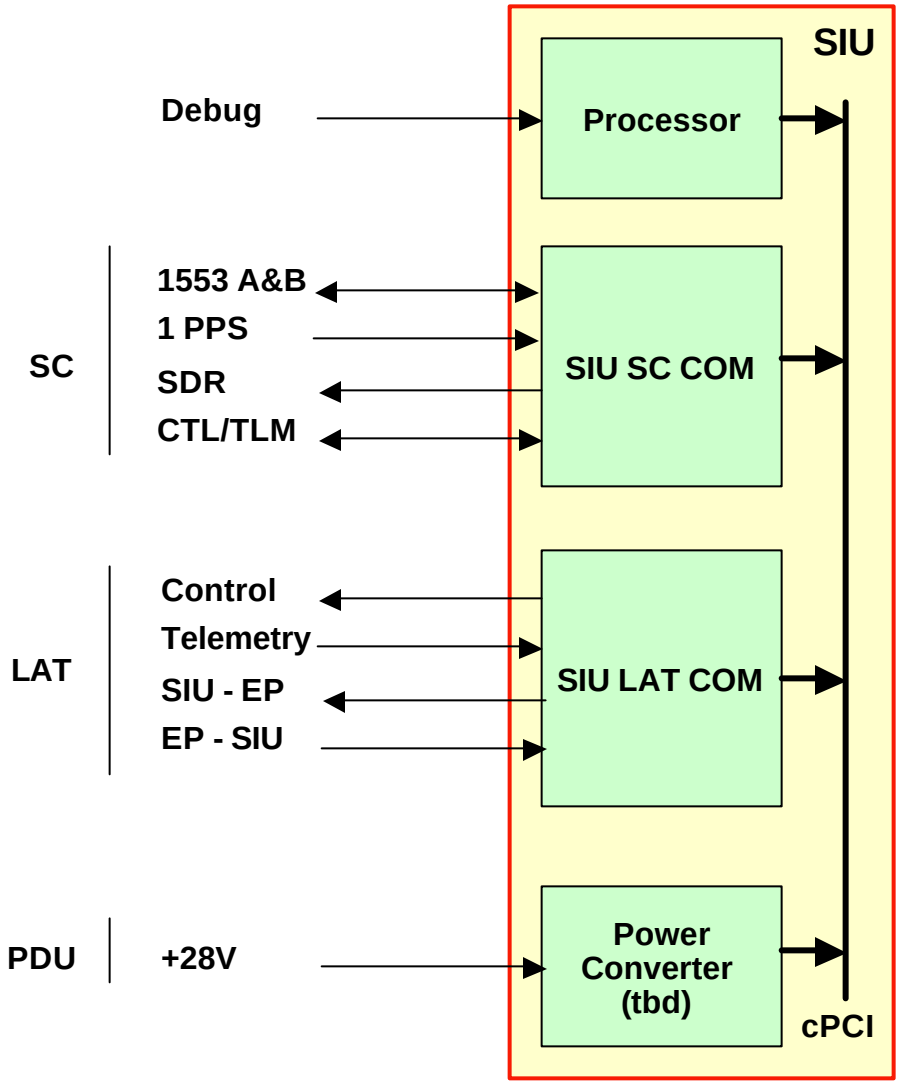
Spacecraft Interface Unit



- SIU Consists Of 4 Modules:
  - SIU processor maintains control over the Instrument
    - PowerPC processor, PCI bus bridge, memory
    - On-going trade study pending availability & cost issues
  - SIU SC COM card provides interfaces to SC
    - 1553 Bus A&B, SDR, 1 PPS, CTL/TLM
  - SIU LAT COM card provides interfaces to remainder of LAT subsystems
    - Control/telemetry/event processor communication
  - Power converter (tbr, see power system presentation)
- Software: see flight software presentation

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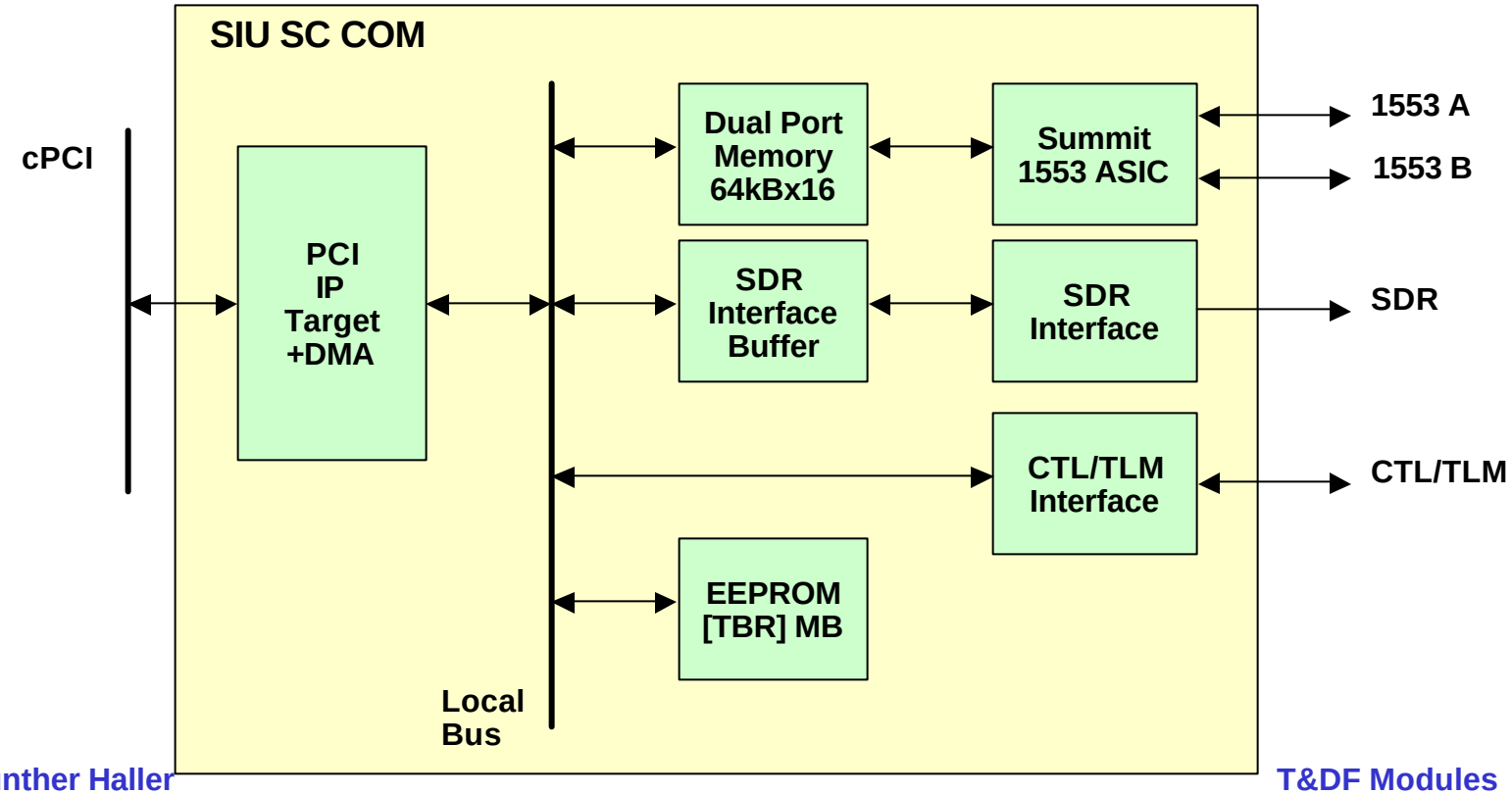
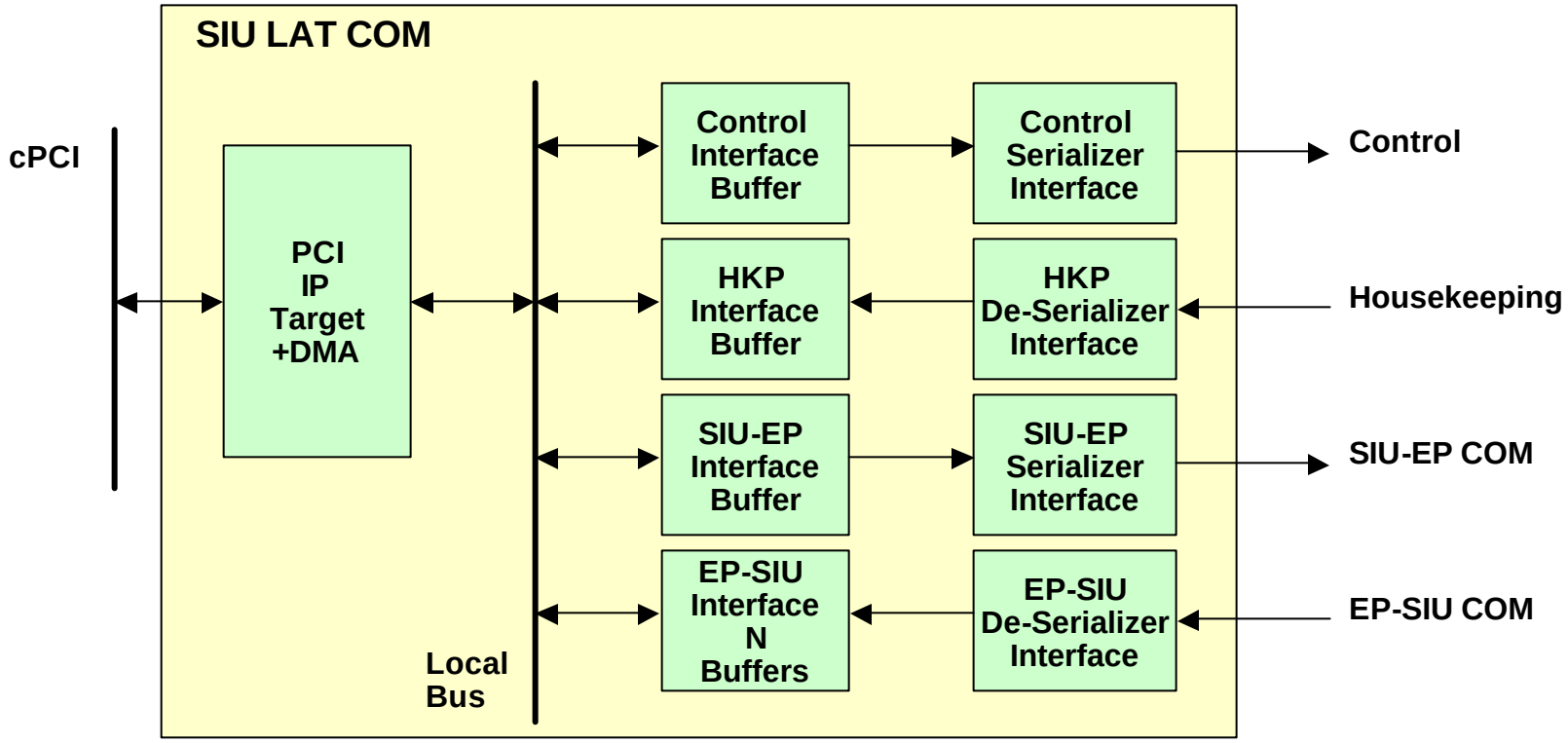
SIU SC COM Card

- SIU SC COM Card Includes a cPCI Interface, SC Data Recorder Interface, SC Control/telemetry Interface
  - May Also Require EEPROM and 1553 Bus Interface If RAD750 Processor Is Selected
- PCI DMA Supported to 1553 Bus Dual Port Memory and SDR Buffer



SIU LAT COM Card

- SIU LAT COM Card May Be Identical or Similar to the Event Builder Card Resident in Each Event Processor
- DMA Supported For SIU-EP and EP-SIU Interfaces



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Issues

- Processor choice
- CPU-CPU communication details
- Physical packaging of modules (space/weight)
- Interconnection