AI: 1 Electronics & Flight Software **By: Norman Rioux**

Question: For both electronics and flight software (FSW) provide a schedule and milestones for the traceability analysis of requirements down through verification.

Reason: Demonstrate the right system is being built and the system is being built right.

Response: The following is a list of FSW milestones and when we hope to have them accomplished:

Software Requirements Specification (ASAP)
This enumerates all the major software modules and their expected impact on system resources. It should also include at least a listing of all the tasks, demonstrating that a complete system is being designed and that we are not completely neglecting smaller issues.

Demonstration of feasibility (before PDR)
This should demonstrate that all major processing tasks outlined in the Software Requirements Specification can be accomplished, with acceptable margins, within the limitations of the memory and CPU cycles. This should also address that the aggregate number of smaller tasks is not so large as to adversely impact system resources.

Complete Software Requirements (between PDR and CDR)
Definition of all software modules including interfaces between modules and hardware/software interfaces.

Demonstration of module functionality (before CDR).
Demonstrate that major software functions work correctly and within allowable system capabilities. For example, demonstrate that the filtering algorithm will correctly reject charged particles and albedo gammas while preserving an acceptable fraction of gammas. This test will be performed using Monte Carlo generated events as input. The results will include both efficiency and purity numbers along with performance numbers.

Software FQT (before integration tests start)
This proves that the whole software system functions and encompasses more than just flight software. In particular, this test should integrate the Ground Support Environment software. Mock data challenges should be included in this phase. Here, data is prepared by a third party and given to the FSW. The data may have various abnormalities artificially introduced (such as slightly misaligned towers or hot track strips). The goal is to prove that the FSW calibration and diagnostic procedures can uncover these abnormalities. Another test is to simulate an orbit in the life of the instrument. This should cover both performance and operational issues.

AI: 2 Electronics & Flight Software **By: Norman Rioux**

Question: Clarify the role of the GBM in generating burst alert messages when viewed from the GBM side of the interface. In some quarters it is believed that the GBM burst alert is strictly a data, rather than a control, function. It may be that the GBM sees itself in no way requesting a re-pointing of the LAT under any circumstances. The GBM burst alert data generated by the GBM is merely data provided to the LAT for the LAT to use in its own internal decision to request the observatory to re-point the LAT.

Reason: It may be that the terminology "GBM re-pointing request" is an unfortunate choice of words that may be open to misinterpretation.

Response: GBM only issues information thus it is a data function. This comes in the form of a candidate with supporting data. This is further processed by the LAT.

AI: 3 Event Path – JJ **By: Elliott Bloom**

Question: GBM does not request LAT to re-point. They inform us of a possible TOO. It is totally up to the LAT to decide to re-point (JJ's software).

Reason: Delicate NASA issue. LAT (JJ's software) should maintain control of LAT physics actions. This is my understanding from discussions in NASA GLAST Science Working Group.

Response: No response. Comment only.

AI: 4 T&DF - JJ **By: Elliott Bloom**

Question: For CAL only trigger: How was the 3-in-a-row strategy modeled? What is the efficiency of this trigger versus E_γ (θ)? How effective is this trigger against backgrounds, e.g. show rate versus E_γ (θ).

Reason: (1) Need for bias-free CAL only trigger for $E_\gamma > E_T$ (TBD). (2) Demonstrate connection between instrument design, implementation and physics requirements.

Response:
Please refer to the Calorimeter PDR material at http://gamma.nrl.navy.mil/glast/calpdr/index.htm for information regarding the Bias Free Cal only trigger.

AI: 5 T&DF Modules – Gunther **By: Elliott Bloom**

Question: Are the processors of choice export-restricted? (Figure 9)

Reason: Non-US collaborators use of processors.

Response: Plans are no non-US collaborator has access to flight modules. The modules will never be shipped abroad.

AI: 6 Command, Control & Configuration – Tony **By: Elliott Bloom**

Question: What defines the length of a run?

Reason: End of run may release summary info for the run and involve overhead for restart. Other actions that are beneficial may be taken at the beginning of a new run. The beginning of a run may signal a configuration change.

Response: It is the intent of FSW that run changes are operational or policy decisions; that is FSW does not prescribe when run changes should occur. It is also noted that a run is somewhat of a High Energy Physics concept. All that is meant by a run is that it delimits a set of data taken under known conditions. Analysis can assume that these conditions apply to all data within a run. Having said that, FSW can provide suggestions and parameters that loosely constrain the policy. The low end of the run duration is constrained by the overheads, both the time and the data volume, incurred in stopping an old run and starting a new run. For the LAT the run change time should be less than one second and the data volume should be no more than the equivalent of 3 seconds (anticipated to be considerably less) worth of normal data.

The high end of the run time is constrained by how long a configuration is fixed. Single Event Upsets (SEUs) can and will occur in the front-end configuration registers. If preliminary calculations can be believed, this should be so rare as to be a non-problem. However, reality may be otherwise. The dataflow architecture prohibits verifying the configuration during running, so the triggers must be stopped, the contents of the configuration registers verified, and, assuming the configuration is as expected, the triggers restarted. Whether one calls this a new run or pause or a verification check is a matter of semantics. The run duration should be less than mean time between loss of configuration, since the data taken between the time of the last verification and the discovery of an error may be unusable because it is unknown when the loss of configuration occurred.

Operationally what is important is that this stop/verify/restart activity should occur at least on a time scale commensurate with the lifetime of the configuration register contents and that it will take about 1 second to complete. Voluntary changes of the configuration, such as mode changes (calibration/diagnostics/triggering changes) and entry/exit of the SAA will also demand a similar sequence.

AI: 7 Data Flow **By: S. Ritz**

Action:
A. Let's update the estimates of the number of crystals and strips per event and show a distribution.
B. Define the magnitude of the problem at L1T, L3T for a dead ACD tile.

Reason:

Response:
A. Agreed. These numbers need to be updated to reflect the current noise estimates in both the CAL and the TKR, the two subsystems that dominate the data volume. GLASTSIM is now in a position to give realistic and believable distributions. Conversations with TKR group have been initiated to understand the expected performance of the TKR and its impact on both false triggers and data volume.
B. Steve Ritz has promised to help with this issue. FSW needs to first address the broader question (and easier, but still difficult) question of how much CPU is needed to do event filtering. This must be done before dealing with the effects of a dead ACD tile. (See AI 9.)
The tactic will be to use Monte Carlo data that has various detector maladies artificially introduced. Since it is impossible to test every combination of such problems, only those deemed likely to happen will be simulated. An important consideration is not only how to handle these problems, but how the solutions impact the amount of CPU time. For example, it may be that the very fast algorithms being considered for event filtering are effective if and only if the data are free of these problems and that much slower algorithms must be used when problems are present.

AI: 8 Dataflow System **By: Arlin Bartels**

Question: At the baseline/PDR review, will results be presented for development risk reduction? In particular, Simulations and Breadboard?

Reason: Areas of highest risk should be shown to have been viably addressed by the baseline review.

Response: Yes. The T&DF System consists 99.9% of digital circuits which can be VHDL simulated. The simulations are part of the design before the Engineering Models are fabricated. The engineering models as called out in PCMS are fully integrated PCB's.

<u>AI: 9</u>   <u>T&DF Modules</u>   **<u>By:</u> <u>Arlin Bartels</u>**

<u>Question:</u> If other options are still being considered, will more detailed information be presented? For the CPU trade study include: CPU Utilization, CPU Cost and other concerns raised from the telecon participants.

<u>Reason:</u> Important to have a baseline CPU by PDR. If questions remain, they should be noted.

<u>Response:</u> The short answer is that these issues are high on T&DF and FSW priority list. It is expected that answers to these questions will be ready by PDR time. What follows is a brief discussion on where we stand and the methods that will be used in determining the answers.

CPU Cost

The cost of each CPU is likely to be in the $200-400K range. The number of CPUs is capped at the upper end by cost, power and space considerations. At the lower end, the number of CPUs is constrained by the number needed to do the job (addressed in the second part of this question) and the number of redundant CPUs needed. Current estimates put the number of Event Processing CPUs at 4 PowerPC 750 @ 133 MHz plus 1 cold spare. (In addition 1 Spacecraft Interface CPU plus a cold space are also needed. This gives a total of 5 active and 2 cold spares.)

CPU Utilization

CPU utilization is recognized within the FSW group as perhaps the most important outstanding question. Studies are now underway to answer this question. Since the number of CPU cycles needed is driven almost entirely by the event filtering, efforts are concentrated on this process. (We have considered the needs of other aspects such as diagnostics and calibration, but these are not drivers.)

The approach is to use data from previous beam tests, the recent balloon flight and Monte Carlo as input when evaluating filtering algorithms. Preliminary stabs at this problem have shown how difficult it is to get a clean answer. The answer is very sensitive to: the memory bus speed of the processor, the number of noise hits in the TKR, the exact data format of the TKR and the noise in the ACD.

Current uncertainties in these numbers render any results meaningless. Because of this, the effort has shifted to firming up these defining numbers. As an example, consider the time needed to unpack the TKR data into a usable form to find and project tracks back to the ACD. The unpacking was prototyped on 2 different CPUs, one a PowerPC 604 @ 333MHz and the other a PowerPC 603e @ 200MHz. A straightforward scaling using the published performance numbers indicates the 604 is factor of 2-3 faster than the 603e. The measured difference was only 15-30%. The reason is that the algorithm is dominated by the memory bus speed, which is the same for each processor.

The same studies indicated that the unpacking dominates by a factor of 4 over the rest of the algorithm and that this time scales with the number of noise hits. With this in mind, the study shifted to exploring what could be done at the hardware level to make the unpacking cheaper. Given the long lead time in implementing a hardware change, it was critical to address this issue immediately.

In a completely different direction, alternate, faster filtering algorithms have been examined. For the most part, these algorithms trade speed for robustness. If the noise of the TKR and ACD are low enough, these are viable candidates. However, noise in either the TKR or ACD could render these algorithms useless.

Other important issues are the vulnerability of the algorithms to detector problems, such as a dead ACD tile. (See AI 7) The answers to these questions are even more dependent on a firm understanding of the parameters previously discussed.

AI: 10 Development, Test and Failure Modes **By: Arlin Bartels**

Question:
Will a more complete picture of EMI/EMC verification from the box to the instrument level be presented at the baseline review?
In particular, for space applications (whether NASA, DoD or commercial), a detailed verification per MIL-STD-461 and MIL-STD-462 is almost always performed, usually in an anechoic chamber.

Reason: Historically, EMI/EMC is the instrument-level environmental test which fails most often (especially radiated emissions). Examples of issues include: SC transponders, launch site radars, self-compatibility and especially clock lines. These issues can sometimes require late retrofit and/or effect instrument operability.

Response: We will measure compliance with GSFC-005 at the box level. These are our specific EMI requirements (see link). EMI/EMC is extremely important because of the high sensitivity of the detection limits. We will perform the tests on the EM boxes.

AI: 11 Development, Test and Failure Modes **By: Arlin Bartels**

Question: Will a more complete picture of the electrical GSE be presented at the baseline review, including: Any assumptions on simulator/design information from the SC Integrated picture of how T&DF E-GSE gets incorporated into the instrument-level test station?

Reason: The scope (and resulting Cost/Budget) of E-GSE is frequently underestimated. It appears that the GSE is budgeted at about 5% of the overall costs which seems low to me.

Response:
Yes. This is being addressed by Elliot Bloom and Scott Williams as part of the I & T effort. A review of the EGSE plans, architecture and approach will be given on September 17th.

AI: 12 Development, Test and Failure Modes **By: N. Johnson**

Question: How many Test Beds will there be? The VME Front-End Com Card needs to support GLT function and needs to sync trigger external data sources for Ground test. What Sun Sparc software environment e.g. GUI, database, end parsing etc. will there be?

Reason:

Response: There will be 1 Test Bed. There will be between 10 and 20 E-GSE Test stations(TBR) to support subsystem testing. The exact number will be determined by PDR. The Front-End Com Card does support GLT and external trigger. We are aware of it. Synching of the external data source is being worked. The Sun Sparc is being worked by I&T/IOC effort. Results will be reported at the September 17th review.

AI: 13 Development, Test and Failure Modes **By: Bill Anderson**

Question: Selection of GSE control software needs to be coordinated with the project, i.e. Oasis, Epoch etc.?
.
Reason: Instrument to SC and SC to instrument simulators need to be common among LAT and SC vendors.

Response:
A trade of candidate software is being performed by the I&T group. The simulators will support the Lat and S/C interfaces. A determination will be made as to the degree of commonality with the control software for the simulators.

AI: 14 Housekeeping Analysis **By: Bill Anderson**

Question: How is the “initiate real time ground contact” managed by the SC and Ground System?

Reason: This function does not currently exist in project documentation.

Response: This statement was the result of a misunderstanding. Presently we have no requirement to “initiate real time ground contact” for any reason other than GBM alerts. This is a subject that should be revisited, particularly given the 2 per day contact scenario. Problems that could stop data taking will have to be dealt with either in an autonomous fashion or by waiting for the next contact. Lack of ‘real time contact’ could result in unacceptably long downtime.

<u>AI: 15</u> <u>Software Schedule/Manpower</u> **<u>By:</u> <u>Bill Anderson</u>**

<u>Question:</u> How is the Flight Software going to be verified and validated?
.
<u>Reason:</u> The program has IV&V requirements.

<u>Response:</u> Flight software has a test plan that is documented in the PDR Report and the LAT Flight Software Management Plan (LAT-MD-104). To reiterate:

1. Low level routines will be unit tested using both white box and black box techniques
2. Packages, or what are referred to as CSCIs, will also be tested using similar techniques.
3. Large scale mock data challenges and operation scenarios will be used to exercise the complete system.

Tests involve both correctness and performance criteria. To the degree possible, testing will be automated. A unit test program designed to test each software component will be maintained. The results of the test program will be archived and used a benchmark.

It is recognized that the above methods have their limitations. Designing well-focused tests becomes increasingly difficult as one moves up the code hierarchy. Building reliable and reproducible tests to probe real time synchronization boundaries is very difficult. Because of this, FSW will use well-established techniques and rigid inspection/analysis to check real time behavior. Continuing on this same path, FSW will enforce strict rules on resource usage. For instance, memory allocation methods will be chosen to avoid fragmentation problems.

FSW also recognizes that their code may be subjected to inspection by Independent Verification and Validation teams. Such inspection may include gathering statistics from the FSW code base, from simple Lines Of Code counts to complexity metrics. FSW has also been informed that such groups may wish to have a full model of the LAT to test the code on. Although FSW has no objections to this, the economic feasibility of this is not clear.

AI: 16 All **By: Martin Nordby**

Question: Add thermal control system and interfaces in architecture and schematics.

Reason: Thermal control system is for instrument protection so it is critical for mission performance.

Response: The requirement is still being generated. When it is clear, it will be addressed. It must be completed before PDR.

AI: 17 Development, Test and Failure Modes **By: F. Blanchette**

Question: Provide documentation to show that the flat conductor cable (≈ 1 m long) going up the tower is flight qualified. Is a test planned (environmental) to verify workmanship of the cables? This would include attaching the cable to the tower. Review with Code 300.
.
Reason: GSFC does not normally support the use of a long flat conductor cable.

Response: Only flat cable will meet our requirements of physical space and mass for the Tracker tower instrument power distribution, commanding and data readout. Each cable handles approximately 14,000 channels of the instrument.

We are following the Mission Assurance Requirements (MAR), for designing the flat cables per IPC-2223 and IPC-2221 Class 3. The qualification and performance testing will be performed per IPC-6013, which is also required in the MAR.

The mass of the flat cable including the nine tray connectors is about 20 grams. There are nine connectors spaced approximately 65 mm and one connector at the end of the cable that connects to the TEM. The cable is captured in the XY plane by the Tracker close outs, sidewalls, Grid and Calorimeter. The clearance, i.e. the ability to move, is less than 1 mm in all but the last ten mm where it connects to the TEM. The cable is restrained between each of the nine connectors that are spaced at 65 mm with kapton tape. The 200 mm section that penetrates the Grid is also restrained with kapton tape. All connectors have jackscrews that will be locked with glue.

Flat cable is used in nearly every automobile and cellular phone in use today. Parlex, which is making our prototypes, routinely manufacture flat cables for space applications.

Nick Virmani will provide a complete document for the procedures to qualify the cables.

AI: 18 Development, Test and Failure Modes **By: F. Blanchette**

Question: Provide rationale/supporting documentation for passing the cable through the box and connecting directly to the PCB. Show flight heritage. Is there a plan to do a complete environmental test or a prototype to prove that it will meet all requirements? This should also be reviewed with Code 300 at GSFC.

Reason: GSFC does not normally support connecting cables directly to PCBs.

Response: See AI # 22

AI: 19 Development, Test and Failure Modes **By: Bill Anderson**

Question: Please provide more details on qualification plans. What is going to be tested and when? Component qualification (board level)? Box qualification? Subsystem level?

Reason: The I&T schedule is aggressive and LAT plans need to show how they are going to get to SC I&T on time.

Response:
Please see http://www.slac.stanford.edu/exp/glast/flight/docs/PDR/ppt/QA-PDR1.ppt for the presentation of the box and subsystem level qualification and design verification.

AI: 20 Power System **By: Martin Nordby**

Question: Need realistic/conservative power fluctuation values for use in thermal design. Is 1000 W for 10 minutes realistic? Is 68 W realistic?

Reason: This drives design of the thermal control system and needs finalizing.

Response: We are aware of this issue and it is being worked on. It will be available before PDR

AI: 21 Mechanical, Thermal and Electrical **By: Louis Fantano**

Question: Provide board level electronic thermal analysis plan and associated schedule. Qualitatively outline the thermal design strategy to transport heat from the piece parts to the radiator heat sink. Specifically address how the 12 W CPU dissipated heat load will be managed and how piece part junction temperature requirements will be satisfied. Also discuss the box level thermal qualification strategy. Will stacks of boxes be simultaneously qualified or will each box be individually qualified?

Reason: Stacking electronic boxes on top of each other provides for tortuous heat transport paths for components located distant from the heat sink. The 12 W processor heat load is likely distributed over a relatively small footprint area and happens to be located in a box separated from the heat sink by another box. This is a cause for concern which needs to be addressed. The stacked box configuration also convolutes the thermal qualification strategy of an individual box since its thermal characteristics are dependent upon other boxes to which it is attached.

Response: We will provide complete thermal analysis for all of the electronics. The CPUs are generally the most difficult devices to cool properly. The general requirements are that the junction temperature of silicon must be kept less than 110 °C. Our candidate design for the CPU uses a standard wedge-lock clamping device to remove the heat through the edge of the board. This design has been tested and meets the 110 °C junction temperature requirement with the wedge-lock kept at 70 °C.

The Grid and the cooling plates for the electronics are designed to be kept at 13 °C during operation. We easily meet the 57 °C temperature rise from the cooling plate to the wedge-lock. This can be seen, for example, by considering that if an aluminum plate 5 mm thick and 100 mm wide is used, the 12 W CPU causes only a 10 °C temperature rise.

AI: 22 Mechanical, Thermal and Electrical **By: Joy Bretthauer**

Question: Why will there be floating connectors within boxes, e.g. a cable connector not attached directly to the box via a connector mounted on the box? Rather the cable is connected directly to a connector on the card through a hole in the box.

Reason: GSFC Hardware Reliability and/or Mechanical may not agree with flying this configuration. The concerns are regarding potential vibration loads induced on the PCB and EMI entering the box through the hole.

Response: Our approach to this is to have the connectors mount to the PWB much like the printer and serial port connectors on the average lap top computer. The connector protrudes through the box so the mating connector can be attached.
The reason for mounting the connector to the PWB instead of to the bulkhead and then to the PWB is for reliability reasons. Connections are always one of the main failure items. More connections constitute more potential failures.
One of the proposed methods is to mount the connector with pigtail wires to the bulkhead and then hand solder the individual wires onto the PWB. The MIL-HDBK217F shows that a 50-pin connector hand soldered will have a failure rate of 0.0325 failures per million hours and that a connector which has been directly soldered to the PWB will yield 0.001 failures per million hours.

The concerns expressed about potential vibration loads are valid. The PWB mounted connectors are restrained in the X-axis with the through-hole pins and the mounting screws. The PWB is restrained in all directions with mounting screws. The custom machined aluminum box limits the connector movement. The gap between the connector and the box 'may' be filled with EMI shielding material as determined by EMI testing of the prototypes.

There is no concern of EMI entering the TEM box, but there is EMI that can exit the box through the hole. Again as stated above, the may be EMI shielding around the connectors. There WILL be additional shielding covering the entire Electronics system to prevent EMI from being transmitted to the spacecraft. We have built a one-to-one scale mockup of the entire LAT partially for performing EMI testing to ensure required performance. These tests start within the next few months.

AI: 23 Mechanical, Thermal and Electrical **By: Louis Fantano**

Question: Provide detailed heat pipe and VCHP layout that shows that the proposed heat pipe thermal control system performance can be verified at the instrument level of integration.

Reason: A significant disadvantage of a heat pipe thermal control system is that it affords very little flexibility in terms of mechanical layout. Heat pipes need to be located precisely in order to function and be ground test verifiable. Detailed heat pipe layouts were not included in the thermal/mechanical presentation. Therefore, although the proposed thermal control system is conceptually viable, it is not possible to assess whether the proposed system is in fact viable.

Response: We are currently finalizing this design and will provide complete thermal design analysis at PDR time.

AI: 24 T&DF **By: Nick Virmani**

Question: Connectors mounted on card assemblies will not be connected to boxes. If that is true, questions about reliability during mate/demate, vibration and connectors should be addressed. There are more reliability concerns with the present thinking. I feel we should secure the connectors through the box. Bulkhead connectors are a good policy.

Reason:

Response: See response to AI: 22.

AI: 25 T&DF Modules, Event Filtering, Trigger **By: Hiro Tajima**

Question: We should make TEM and GLT as flexible as possible with regard to Trigger and Event Filtering algorithms.

Reason: Event filtering requires 1/300 reduction which is very demanding. This requires flexibility of data format and trigger algorithm since real data could be different from what we expect. Optimization of trigger and event filtering needs to be done using the real data. Simulation does not give us the real world.

Response:

GLT

The GLT will be programmable to a certain level. Certainly prescalers can be adjusted. It may be possible to reprogram the combinatorial logic that combines the trigger primitives. However, this does not provide much additional capability. Flexibility in the GLT is constrained by a small and rigidly defined set of trigger primitives. The number of combinations of trigger primitives that are interesting is extremely limited. For example:

1. 3-in-a-row
2. 3-in-a-row & No-ACD-Veto
3. CAL HI
4. CAL LO
5. Etc.

Combinations like 3-in-a-row & No-ACD-Veto & CAL LO may be marginally of interest, but that may about it.

The trigger primitives are very ‘digital’ in nature, i.e. there are not many ‘knobs’ that can be turned. The CAL LO and HI discriminator thresholds can be adjusted. It may be possible to select which ACD tiles are used to veto a specific tower.

The message here, is, while there will be some degree of flexibility in the GLT, it is more in the form of minor adjustments or tweaks. Physical constraints prohibit wholesale changes.

Event Filtering

Steps are being taken to allow flexibility in the filtering algorithm. Given that the event filtering is implemented in software, modifications to the event filtering are much easier and can be more extensive than in the GLT. This reasoning motivates the arguments to keep the L1 trigger as open as possible.

The parameters controlling the cuts in the filtering algorithm may be changed by table uploads. It is expected that distributions gathered both on the LAT and by the ground software would be used in determining the values of these parameters.

Second, if the logic of the filtering algorithms needs to be changed, new code may be uploaded from the ground. This is a more drastic step than merely changing parameters. Given the very small upload bandwidth, the on-board software will be constructed in a modular fashion so that only what absolutely needs to be replaced is uploaded.

In both uploading new parameters and new algorithmic codes, steps must be taken to document and record these changes. Mechanically it is much easier to automatically record and track the effects of parameter changes. Ground software likely can just read the event filtering parameters and react appropriately. Automatically absorbing the effects of code changes is harder. Such changes will likely cause a matching set of code changes in the offline software as well.

Data Format

It will not be possible to change the input data format from the front-end electronics. The front-end data formatting engines, whether implemented in FPGAs or ASICs, will not be reprogrammable. Even if one could reprogram the formatting engines, most substantive changes to the data formatting would likely involve other resources, such as buffer memories to hold the data during a sort operation. It is unlikely that such resources exist and if they did, that their organization would be suitable. Design cushions are built in to accommodate the inevitable mismatch between Monte Carlo and reality, but the Monte Carlo must be relied upon to be at least close.

It will be possible to adjust the output data format, but, given the number of software components that depend on the format, it is highly undesirable to do this.

Summary

Fortunately, the vulnerability is directly correlated with the ease of making the correction. That is, the parameters for the filtering algorithms are the most likely to be in need of adjustment and, operationally, are the easiest to adjust. At the other end of the spectrum, changing the front-end data format is impossible, but, fortunately, likely unnecessary.

AI: 26 Flight Software **By: Darren Marsh**

Question: Show how software assurance requirements of the LAT MAR and PAIP will be fulfilled. Specifically, a software quality management system that complies with ISO 9001 must be in place.

Reason:

Response: See response to AI 15.

AI: 27 T&DF **By: Neil Johnson**

Question: If ACD is an active veto to event trigger, do you know how to compute dead time?

Reason:

Response: Calculating the deadtime and in particular, the deadtime as a function of time, in a system with an asynchronous trigger using vetoes is non-trivial and the answer given here is not complete. This question deserves careful thought.

It is expected that playing independent triggers off against each other will be at least part of the answer. For example, the TKR-3-in-a-row & no ACD vetoing tile can be compared with a prescaled version of a bare TKR 3-in-a-row. Events that come in under the bare TKR 3-in-a-row will contain both events that have an ACD veto and those with no ACD veto. The fraction of events of gamma events inadvertently vetoed by the ACD can be calculated from this information.

Practical issues may limit the accuracy of this method in two ways. The prescaling of the bare 3-in-a-row may be so high as to limit the number of photons and, therefore, limit the statistical accuracy. The deadtime may be tower specific, particularly if the ACD noise is not uniform, forcing one to calculate the dead time on a tower-by-tower basis. Given that some tracks cross tower boundaries, one is forced to consider the correlations, changing the calculation of the dead time from a simple arithmetic problem to a matrix problem. Gathering statistics on the off-diagonal elements may be hard.

Many times the Monte Carlo can help extract the efficiency numbers, but this technique is weakened if the effect is time dependent as it would be with pile-up.

Conclusion

Further work is necessary to clear up this issue. A clean statement of the desired accuracy of the dead time measurement is needed.