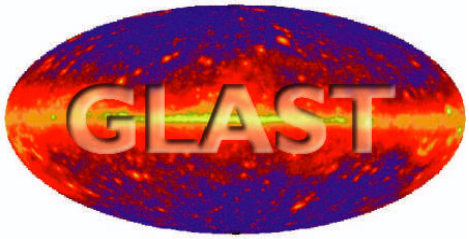

LAT Flight Software

TPG Developer's Guide

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A developer’s guide for the Trigger Pattern Generator software, mostly for my own benefit

Contents

0 Introduction

The Trigger Pattern Generator (TPG) is a combination of hardware and software that provides trigger input signals to the GEM. The TPG simulates one quarter of the LAT, 3 ACD FREE boards and four TEMs, using five VME COMM boards.

1 Trigger Input Signals

Each TEM produces four input signals:

1. Tracker three-in-a-row (TIAR)
2. Calorimeter low energy (CALLO)
3. Calorimeter high energy (CALHI)
4. Busy signal

Each FREE produces nineteen trigger input signals:

1. Eighteen veto signals (VETO00 … VETO17)
2. CNO signal

Each signal can be specified as asserted (on) or de-asserted (off) for each tick of the system clock (a period of fifty nanoseconds for a twenty megahertz clock).

1.0 Signal Assignments

Each COMM board has twenty-four LVDS transmitters connected to a socket on the front panel. Eighteen of these are driven by a playback FIFO on the board. The pin-pairs are assigned to the various trigger inputs as follows

1.0.0 TEM

The TEM trigger inputs are provided by board number four.

Pin-Pair	TEM Trigger
0	0 Busy
1	0 TIAR
2	0 CALHI
3	0 CALLO
4	1 Busy
5	1 TIAR
6	1 CALHI
7	1 CALLO
8	
9	
10	2 Busy
11	2 TIAR
12	2 CALHI
13	2 CALLO
14	3 Busy
15	3 TIAR
16	3 CALHI
17	3 CALLO

All the rest of the pin-pairs are unused.

1.0.1 CNO

The CNO trigger inputs are provided by board number three.

Pin-Pair	CNO
0	0
1	1
2	2

All the rest of the pin-pairs are unused.

1.0.2 ACD VETO

The three FREE boards are simulated by COMM boards zero, one and two.

Pin-Pair	Veto
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	
9	
10	8
11	9
12	10
13	11
14	12
15	13
16	14
17	15
18	
19	
20	
21	
22	16
23	17

2 Playback FIFO

The COMM board services are provided by Curt Brune's GNAT library. Eighteen of the twenty-four output pin-pairs on the front panel of the COMM board are driven by the playback FIFO, which is thirty-two times one thousand and twenty-four bits deep. Simultaneous playback of all five COMM board playback FIFOs is achieved by chaining the COMM boards together through the start out/in sockets on the front panels. Clock skew of up to ?? nanoseconds can be removed by setting a delay period on each board. Large differences in timing must be removed by setting

the first several words of the playback FIFO to 0. Of course, this reduces the usable FIFO depth. Playback is initiated by setting the playback bit on the master board.

The playback FIFOs are filled from pattern buffers residing in the SBC RAM. There are five arrays of thirty-two times one thousand and twenty-four unsigneds, once for each board. The TPGstart function sets the clock delays, fills the five FIFOs and sets the start bit.

It should be noted that the last word from the FIFO “sticks” on the output pin-pairs, so should normally be all zero.

3 Pattern Buffers

Virtually all of the TPG core code is concerned with management of the five pattern buffers. The various functions for creating patterns for each trigger input are described in the User Manual, but they are all just thin wrappers around a single function. These wrappers provide input validation and convert a user specified trigger description (TEM or FREE ID, VETO etc.) into a board and line number pair. The board number obviously identifies which pattern buffer is to be manipulated. A start number, pattern length and number of time the pattern is to be repeated combine to identify which words of the buffer need to be modified, while the line number identifies the bit to be changed in each word.