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Document Title

Storage Interface Board – Specification and ICD

Change History Log

Revision	Effective Date	Description of Changes
original	29 July 2003	
	25 August 2003	Corrected Figure 12, Enlarged Resistor Fonts on Fig 4 & 7
	04 Feb 2004	Revised to show differences between SIU and EPU versions. Also, the Left and Right bit in the Heater Register in 4.2.2.18.1.4 were swapped

DOCUMENT APPROVAL

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1. SCOPE

There are two versions of the Storage Interface Board (SIB): the Spacecraft Interface Unit (SIU) version and the Event Processor Unit (EPU version.

The same printed circuit board and FPGA design are used for the two versions. Only the circuit card assemblies are different. The SIB-SIU version is populated with all components. The SIB-EPU version does not have the Mil 1553 interface. Specifically, the SIB-EPU version does not have the following components installed on the circuit card assembly (See Figure 1 SIB Block Diagram):

SUMMIT chip
SRAMs (2)
48 MHZ Osc
AHCT74 (flip-flop used to divide 48MHZ clock)
1553 Transformers (2)

The Storage Interface Board (SIB) provides four (4) major functions.

- MIL-STD-1553B interface to the GLAST/LAT spacecraft. (SIU version only)
- Up to 8 Mbytes of EEPROM program storage accessible from cPCI bus.
- Controls Heater Control Boxes
    - 12 Control Signals to Left Heater Control Box (12 open collector, active high)
    - 12 Control Signals to Right Heater Control Box (12 open collector, active high)
- Controls PDU/GASU
    - Four Control Signals to Primary PDU/GASU (4 open collector, active low)

Four Control Signals to Redundant PDU/GASU (4 open collector, active low)
This specification includes a functional description of the SIB, memory maps, the allocation of PCI configuration space, system interface, and electrical connector interface.

2. DEFINITIONS AND ACRONYMS

The following terms, abbreviations, and acronyms are used in this document:

2.1 Definitions

MHz Megahertz, 10^6 Hz

ns nanosecond, 10^{-9} Second

µa Microamp 10^{-6} amps

V Volt

2.2 Acronyms

cPCI Compact PCI

DMA Direct Memory Access

DWORD Double word

EEPROM Electrically erasable programmable read only memory

EPU Event Processor Unit

FPGA Field Programmable Gated Array

GASU Global trigger, Anti coincidence, Spacecraft interface Unit

GLAST Gamma Ray Large Area Space Telescope

LAT Large Area Telescope

PCI Peripheral Component Interface

PDU Power Distribution Unit

RAM Random Access Memory

SIB Storage Interface Board

SIU Spacecraft Interface Unit

3. REFERENCE

The following documents are relevant to the design and implementation of the SIB.

LAT-DS-01674 Circuit Card Assembly, SIB (SIU version)

LAT-DS-02533 Circuit Card Assembly, SIB (EPU version)

LAT-DS-01675 Printed Wiring Board, SIB

LAT-DS-01676 Schematic Diagram, SIB

LAT-DS-01678 Test Procedure, SIB (TBS)

LAT-DS-01817 Parts Stress/Worst Case Analysis, SIB (TBS)

LAT-DS-01540 Specification, SIU/EPU Backplane

LAT-DS-01654 Specification, EPU (TBS)

LAT-DS-01685 Specification, SIU (TBS)

4. SPECIFICATION

The SIB is a compact PCI (cPCI) 6U card. The SIB is conduction-cooled and incorporates multi-segmented wedgelocks and card stiffeners. The SIB block diagram is illustrated in Figure 1. The cPCI is 33Mhz, 32-bit, 3.3v Signaling target only card.

The 1553 interface, in the SIU version, provides both channels A and B, and operates as a Remote Terminal. The Remote Terminal address is 3_{10}. The SIB utilizes an Aeroflex UTMC Summit DXE chip as the primary interface to the 1553 bus.

The SIB provides up to 8 Mbytes of EEPROM for non-volatile program storage. The EEPROM is divided into two (2) equal parts of 4 Mbytes. Each of the two (2) EEPROM banks has separate write-protect schemes implemented in the FPGA.

The SIB provides 12 control signals to the Left Heater Control Box and 12 control signals to the Right Heater Control Box. These output signals are open collector and are defined as active high. The SIB provides a software register to control these signals. A 1 min watchdog timer circuit activates these signals in the event the processor fails to respond. If the SIB is powered off or during a reset condition, the 24 control signals must be allowed to float high.

The SIB provides four control signals to the Primary PDU/GASU and four control signals to the Redundant PDU/GASU. These output signals are open collector and are defined as active low. The SIB provides a software register to control these signals. The software register (PDU/GASU Register) is not affected by the cPCI RESn signal. The software register (PDU/GASU Register) is cleared by the EXT_POR_L signal. The EXT_POR_L signal is an input signal to the SIB.

All I/O for the SIB is via the backplane connectors. The J1 connector is for the cPCI interface and J4 and J5 are for the I/O. There are no front panel connectors on the SIB.

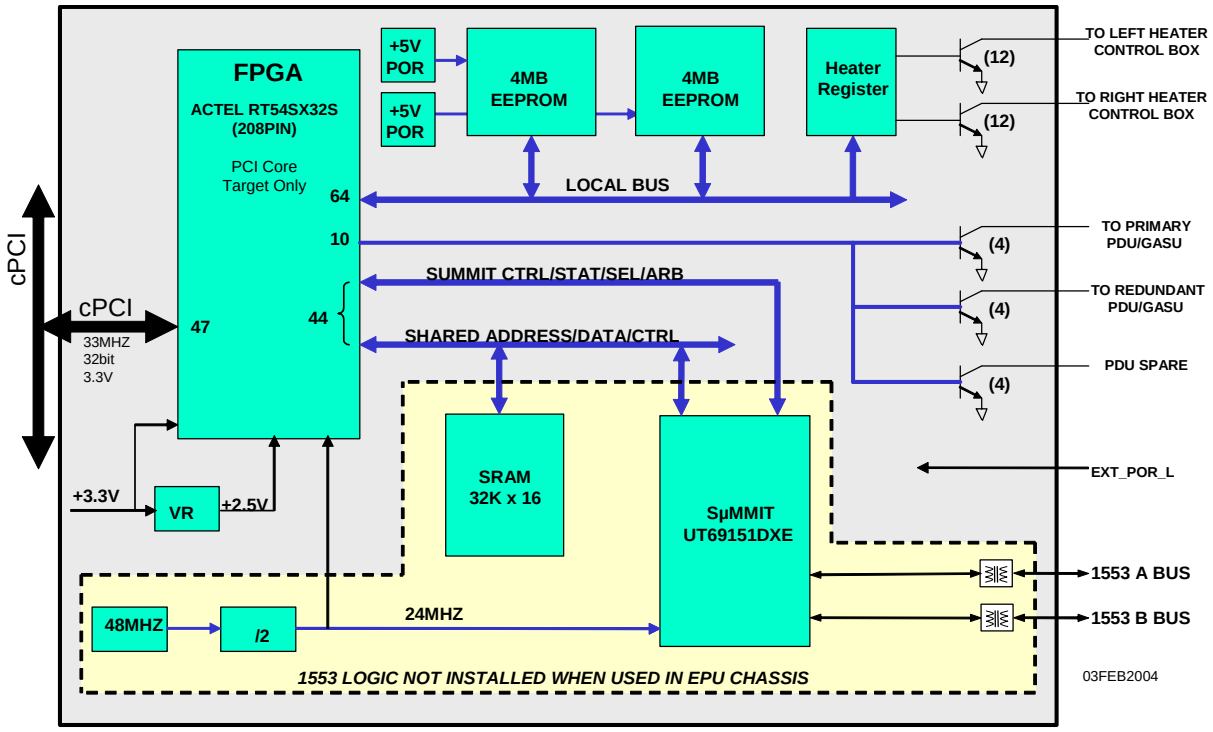

Figure 1 SIB Block Diagram

4.1 External Hardware Interface description

The following paragraphs describe the external interfaces of the SIB including:

- Mil-Std-1553B (SIU version only)
- PDU/GASU
- Heater Control
- External Power On Reset

4.1.1 MIL-STD-1553B Interfaces

The SIB communicates with GLAST/LAT spacecraft through a 1553 Serial Bus. The SIB operates as a Remote Terminal (RT Address 3_{10}), acting only upon valid commands received from a 1553 Bus Controller. Data received from the Bus Controller will be indexed and stored in shared Random Access Memory (RAM). Data to be transmitted via the 1553 Bus will be accessed from the shared RAM.

The shared RAM is 64 Kbytes. The Summit Chip accesses the shared RAM as 32K x 16bit. The SIB processor shall access the shared RAM as 32K x 32bit (DWORD). The upper 16-bits of the RAM do not exist. Please refer to the memory map in section 4.2.2.18.4

Arbitration is required to handle shared RAM access between the cPCI and the Summit chip. Arbitration is also required for the cPCI to access the Summit Registers. The Summit has a higher priority to access Shared RAM than the cPCI bus. Once the Summit Chip requests access by driving the DMAR- signal, all Summit RAM transactions must be completed within 7μs or a Direct Memory Access (DMA) FAIL will occur. If the cPCI requests the RAM while the Summit has access, a PCI Target Retry termination will occur. If the cPCI has access to the RAM and the Summit requests access (DMAR- true), the FPGA will finish the current data transaction and a PCI Target Disconnect with data termination will occur.

The MIL-STD-1553B detail interface is illustrated in Figure 2. The SIB provides Long-Stub transformer coupling on the A and B buses. The 1553 buses are accessible on the J5 backplane connector.

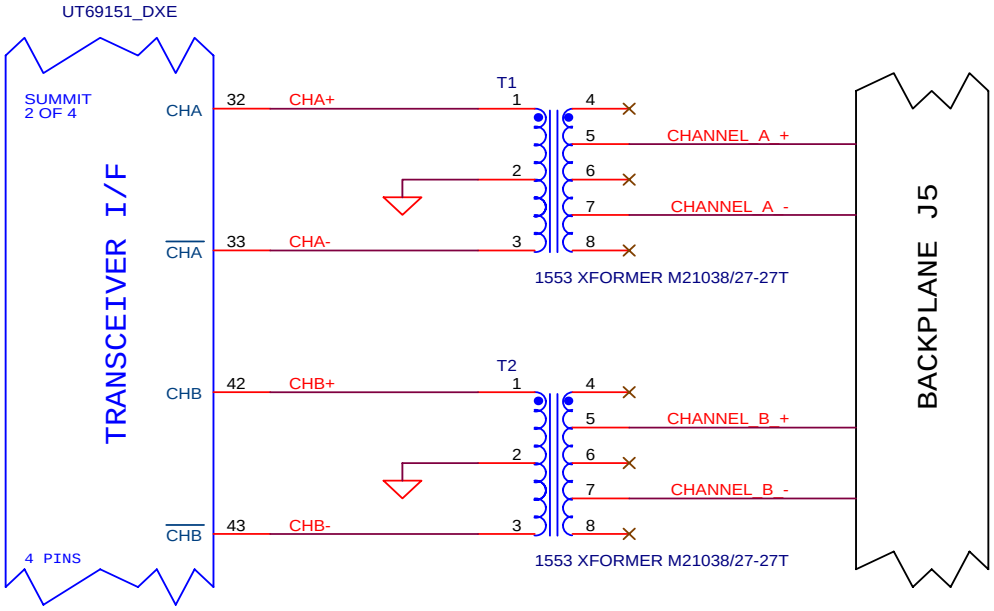

Figure 2 1553 Bus Detail Interface

4.1.2 PDU / GASU Interface

The SIB provides control of the Primary and Redundant PDU/GASU. The SIB provides four open collector outputs to the Primary PDU/GASU and four open collector outputs to the Redundant PDU/GASU. The SIB includes four spare output signals. The open collector output signals are active low logic. The cPCI processor writes the PDU_GASU Register. The PDU_GASU register is cleared at power up by the EXT_POR_L signal. The PDU_GASU register is not affected by the cPCI RESn signal. Figure 3 illustrates the primary and redundant interfaces. Figure 4 illustrates the PDU/GASU typical electrical interface.

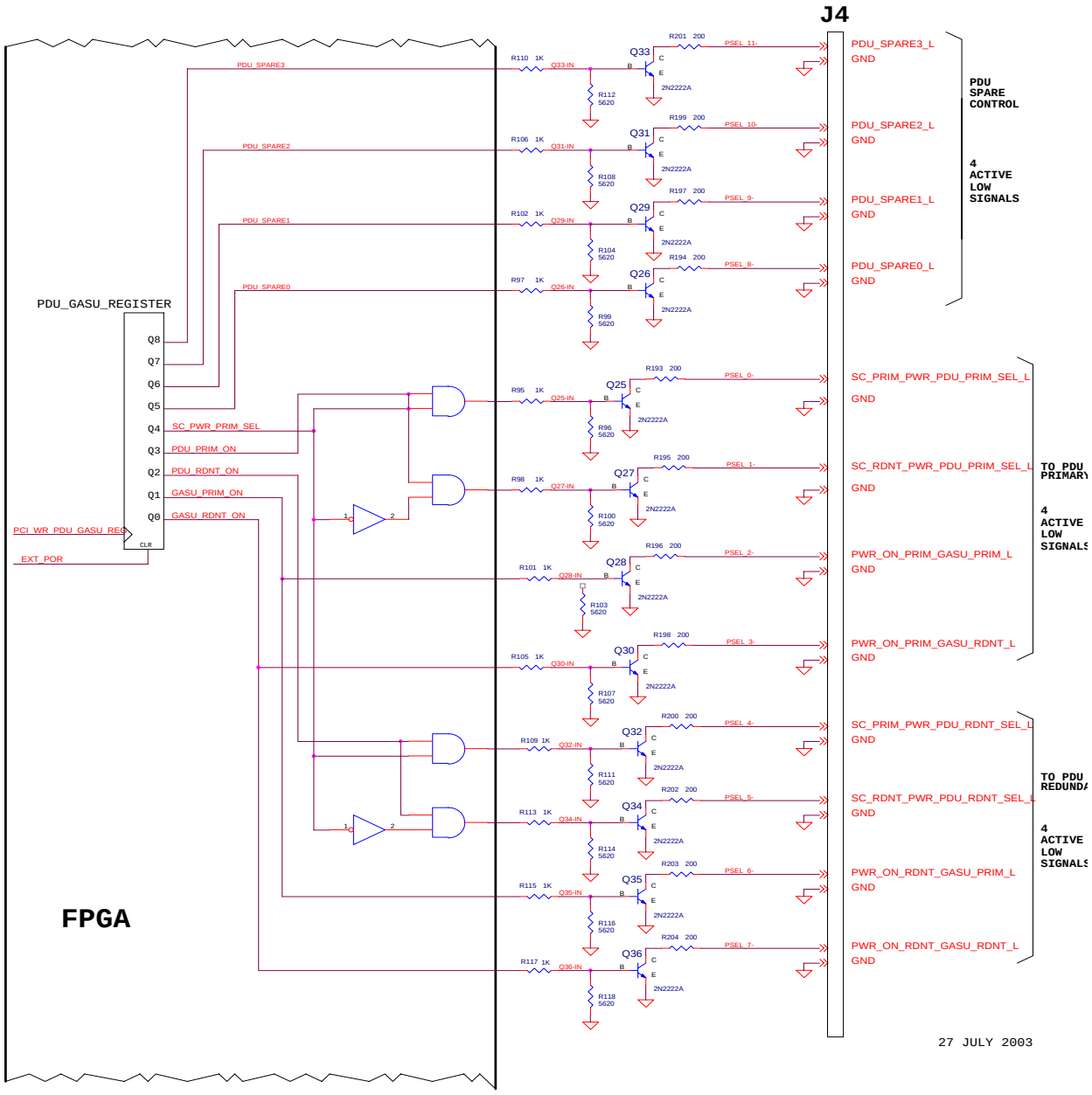

Figure 3 PDU/GASU Primary and Redundant Interfaces

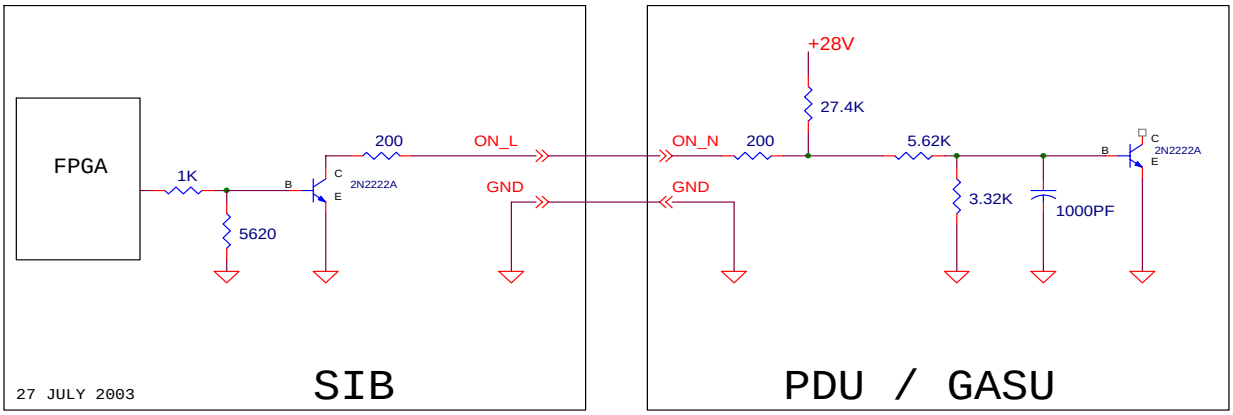

Figure 4 PDU/GASU Typical Electrical Interface

The PDU/GASU signals are required to sink 1ma (nominal) @ 0.3volts with respect to the SIB. The expected off state open collector voltage is 6V (nominal).

4.1.3 Heater Control Interface

The SIB provides control of the Left and Right Heater Control Boxes. The SIB provides 12 open collector outputs to the Left Heater Control Box and 12 open collector outputs to the Right Heater Control Box. The open collector output signals are active high logic. The cPCI processor writes the Heater Control Register. The Heater Control Register is located on the SIB board, but is not inside the FPGA. The Heater Control register is cleared at power up by the EXT_POR_L signal or by the cPCI RESn signal. A 1-minute watchdog timer circuit also clears the Heater Control Register. Figure 5 illustrates the Left Heater Control interfaces. Figure 6 illustrates the Right Heater Control interfaces. Figure 7 illustrates the typical electrical interface.

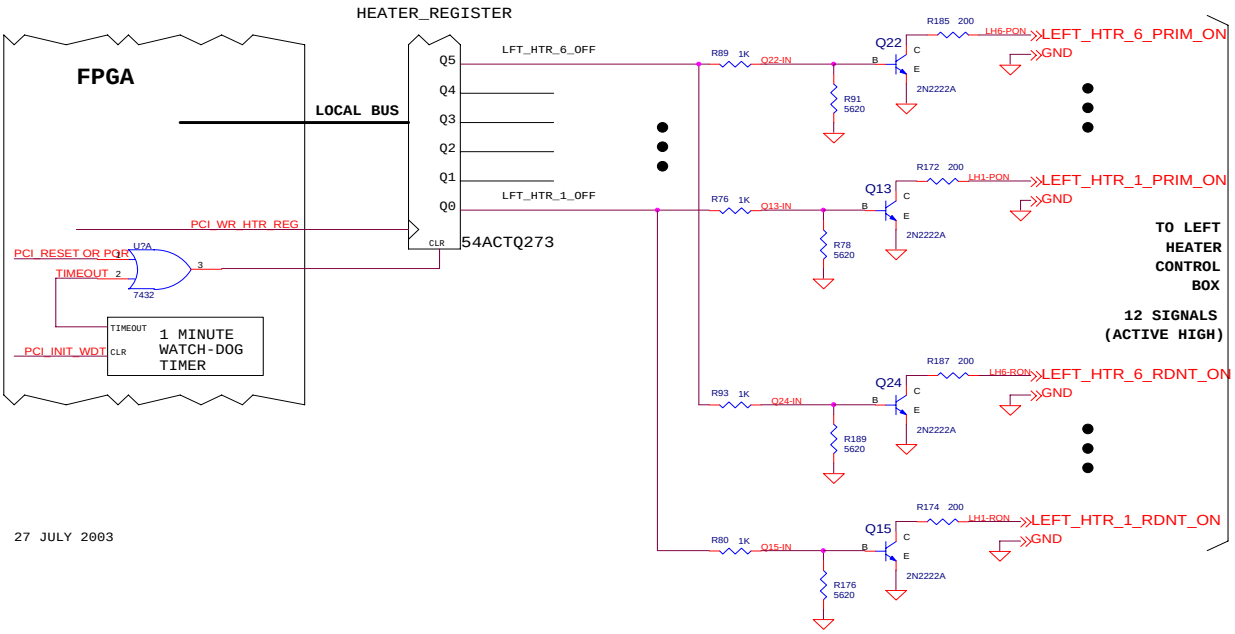

Figure 5 Left Heater Control Box Interface

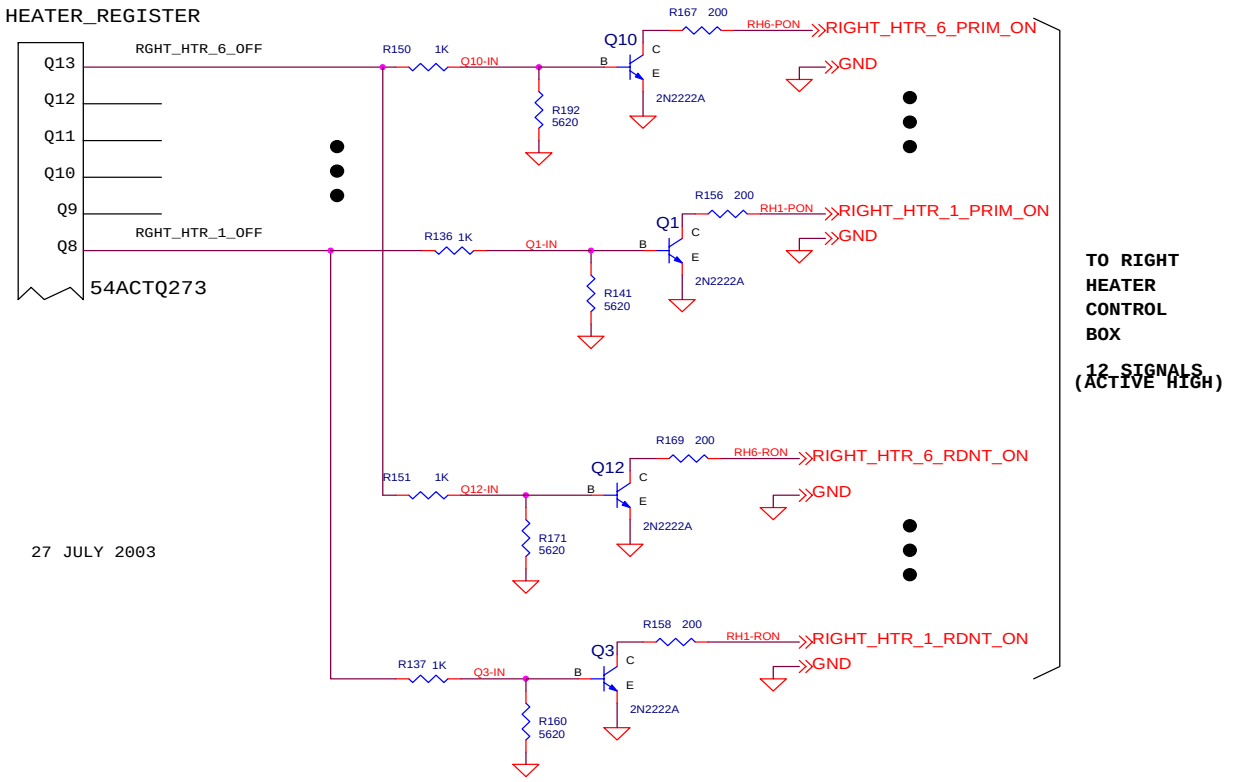

Figure 6 Right Heater Control Box Interface

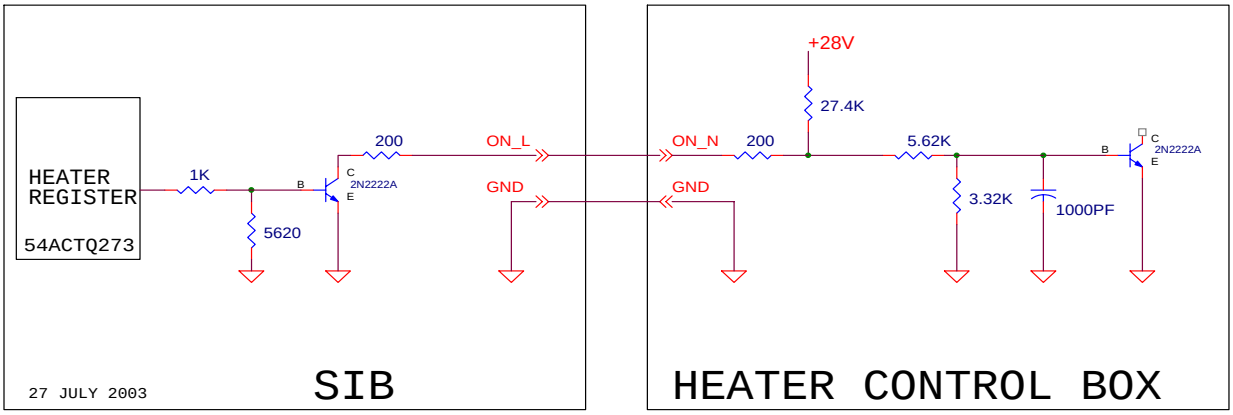

Figure 7 SIB to Heater Control Box Typical Electrical Interface

The Heater Control signals are required to sink 1ma (nominal) @ 0.3volts with respect to the SIB. The expected off state open collector voltage is 6V (nominal).

4.1.4 Heater Control Operation

When the SIB is powered off, all 24-output transistors will be off. The open collector outputs can be pulled high by the Heater Control Boxes.

During cPCI Reset, the Heater Control Register will be held in reset. All 24-output transistors will have zero base current and therefore the open collector outputs can be pulled high by the Heater Control Boxes.

During a SIB power up or power down transition, the Heater Control Signals may or may not glitch. After a power up transition, the EXT_POR_L signal will reset the Heater Control Register allowing the output signals to be pulled high by the Heater Control Boxes.

If software fails to initialize the 1-minute watchdog timer, then the Heater Control Register will be reset. All 24-output transistors will have zero base current and therefore the open collector outputs can be pulled high by the Heater Control Boxes.

The only time a Heater can be turned off is if software writes a '1' in the Heater Register.

4.1.5 External Power On Reset (EXT_POR_L)

The EXT_POR_L is an input signal to the SIB. EXT_POR_L signal is used to clear the Heater Control Register and the PDU_GASU Register. Figure 8 illustrates the EXT_POR_L interface.

With Respect to J4 connector pins:

V_{IL} = 0.8V max

V_{IH} = 2.0V min

I_{IL} = 350ua @ Vin 0V (10K + FPGA)

I_{IH} = -20ua @ Vin 3.3V (current into FPGA)

Minimum pulse width (active low) = 300ns

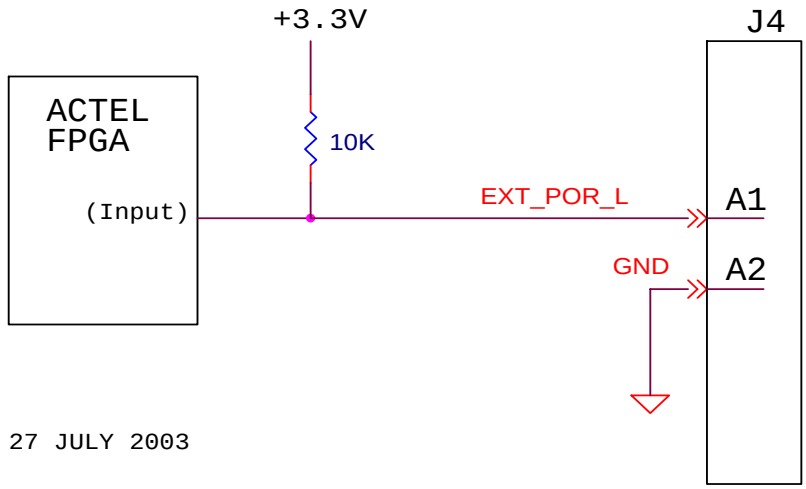

Figure 8 EXT_POR_L Interface

4.2 Internal Interface Description

4.2.1 cPCI Backplane

The SIB conforms to cPCI standards. The Card is compatible with a 32-Bit bus width, a clock speed of 33MHz, and +3.3V signaling.

4.2.2 Configuration Registers

The configuration space (Figure 9) is divided into a predefined header region (00h to 3Fh) and a device dependent region (40h to FFh). Address 48h is the Interrupt Control/Status Register.

31-24	23-16	15-8	7-0	Address
Device ID		**Vendor ID**		00h
Status		**Command**		04h
Class Code			**Revision ID**	08h
BIST	**Header Type**	**Latency Timer**	Cache Line Size	0Ch
Base Address #0 (Memory Location for Baseline Target)				10h
Base Address #1 (Optional Memory or I/O)				14h
Base Address #2 (Optional I/O for DMA Register Mapping)				18h
Base Address #3				1Ch
Base Address #4				20h
Base Address #5				24h
CardBus CIS Pointer				28h
Subsystem ID		**Subsystem Vendor ID**		2Ch
Expansion ROM Base Address				30h
Reserved			**Capabilities Pointer**	34h
Reserved				38h
Max_Lat	Min_Gnt	**Interrupt Pin**	**Interrupt Line**	3Ch
Interrupt Control/Status Register				48h

Figure 9 Configuration Registers

4.2.2.1 Address 00h Device ID Vendor ID

Device ID = 0844h, Vendor ID = 11AAh, Vendor ID of 11AAh is registered to Actel Corp.

4.2.2.2 Address 04h Status Command

Software must write a 0003h to enable Memory and I/O transfers

4.2.2.3 Address 08h Class Code Revision ID

Class Code = FF0000, Revision ID, increments for each new revision of the PCI FPGA, range is 00 to FFh.

4.2.2.4 Address 0Ch BIST Header Type Latency Timer Cash Line Size

0hex

4.2.2.5 Address 10h BAR0

Writing a FFFF,FFFFh will be read back as FF00,0000h. 16Mbyte of memory space, non-prefetchable, locate anywhere in 32-bit address space. Software should write xx000000h where xx is the base address.

4.2.2.6 Address 14h BAR1

Not used

4.2.2.7 Address 18h BAR2

Not used

4.2.2.8 Address 1Ch BAR3

Not used

4.2.2.9 Address 20h BAR4

Not used

4.2.2.10 Address 24h BAR5

Not used

4.2.2.11 Address 28h CardBus CIS Pointer

Not used

4.2.2.12 Address 2Ch Subsystem ID Subsystem Vendor ID

0000h and 0000h

4.2.2.13 Address 30h Expansion ROM Base Address

Not enabled, 0h

4.2.2.14 Address 34h Capabilies Pointer

0h

4.2.2.15 Address 38h Reserved

0h

4.2.2.16 Address 3Ch Max_Lat Min_Gnt Interrupt Pin Interrupt Line

INTA# used, 01h

4.2.2.17 Address 48h Interrupt Control/Status Register (Table 1)

This register enables interrupts, indicates card is driving an interrupt, and where interrupts are cleared. Writing a 200h will enable interrupts.

Table 1 Interrupt Control/Status Register

BIT	TYPE	DESCRIPTION
7:0	R/0	Read Only zeros
8	R/W	Interrupt Active, Logic 1 indicates an active interrupt condition. The interrupt is cleared by writing a '1' . This bit is cleared (=0) after a reset condition. There are three events which cause interrupts: Setting Software Interrupt Bit , Refer to Control Register bit **GSW_INTR** YF_INTR from the SuMMIT Chip MSG_INTR from the SuMMIT Chip
9	R/W	Interrupt Enable, Active 1 enables interrupts. Active 0 disables interrupts.
31:10	R/0	Read Only zeros

4.2.2.18 Memory Map

All accesses to the SIB are memory. All memory I/O accesses are 32 bits wide. No byte or word accesses are supported. The SIB uses a contiguous memory area of 16-Mbyte. The top memory map view for the SIB is shown in Figure 10.

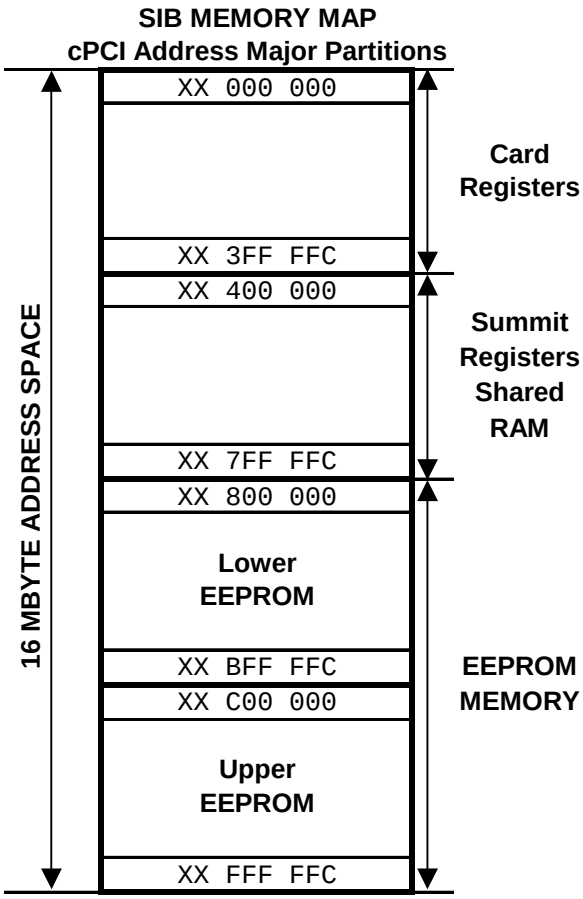

Figure 10 SIB Memory Map top view.

4.2.2.18.1 SIB Registers

There are five card registers. The top view of the Card Registers is shown in Figure 11.

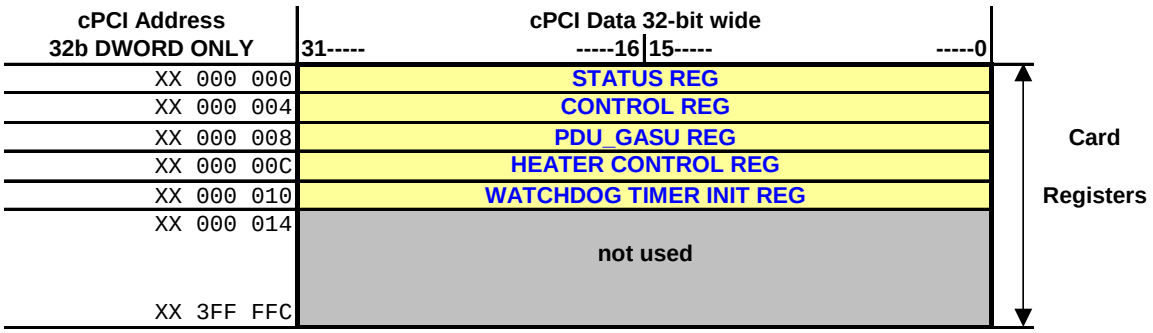

Figure 11 Card Registers Top View

4.2.2.18.1.1 SIB Status Register (Table 2)

XX 000 000 READ ONLY STATUS REG

BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24
BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UEEP_WER	LEEP_WER	UEEP_WE	LEEP_WE	MISS_DPS	WDT_TO	READY	TERM ACT

Table 2 SIB STATUS REGISTER

BIT	MNEMONIC	DESCRIPTION
31:8		not defined
7	**UEEP_WER**	UPPER EEPROM WRITE ERROR, Active 1 indicates that the PCI BUS attempted to write the Upper EEPROM while not enabled. UEEP_WER is cleared cPCI Reset or after reading the Status Register. This error indicates a software coding error. Writing to an unlocked EEPROM will be ignored.
6	**LEEP_WER**	LOWER EEPROM WRITE ERROR, Active 1 indicates that the PCI BUS attempted to write the lower EEPROM while not enabled. LEEP_WER is cleared by the cPCI Reset or after reading the Status Register. This error indicates a software coding error. Writing to an unlocked EEPROM will be ignored.
5	**UEEP_WE**	UPPER WRITE ENABLED, Active 1 indicates that the upper EEPROM bank can be written. Active 0 indicates writing to upper EEPROM is prohibited.
4	**LEEP_WE**	LOWER WRITE ENABLED, Active 1 indicates that the lower EEPROM bank can be written. Active 0 indicates writing to upper EEPROM is prohibited.

BIT	MNEMONIC	DESCRIPTION
3	**MISS_DPS**	MISSED DATA PHASE START, Active 1 indicates that the PCI backend state machine missed the backend DP_START pulse. This bit is cleared after reading the Status Register. When the DP_START is driven by the Actel PCI core and the State Machine is not in the Idle state, the Busy signal is driven to the PCI core, Busy signal will cause the PCI core to issue a Target Retry. MISS_DPS bit is used to aid hardware testing and debug. This bit can be ignored by software and may be removed without notice. When removed, this bit will be always logic 0.
2	**WDT_TO**	Watchdog Timer Timed Out, Active 1 indicates the 1-minute (65sec) watchdog timer expired. Writing to the Watchdog Timer Init Register clears WDT_TO status bit.
1	**READY**	SUMMIT READY SIGNAL
0	**TERMACT**	SUMMIT TERMACT SIGNAL

4.2.2.18.1.2 SIB Control Register (Table 3)

XX 000 004 RD/WR CONTROL REG

BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24
BIT 23	**BIT 22**	**BIT 21**	**BIT 20**	**BIT 19**	**BIT 18**	**BIT 17**	**BIT 16**
BIT 15	**BIT 14**	**BIT 13**	**BIT 12**	**BIT 11**	**BIT 10**	**BIT 9**	**BIT 8**
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
SUM_RES	**GSW_INTR**	**U_EPWE_LTCH**	**U_EPWE_SD**	**U_EPWE_INIT**	**L_EPWE_LTCH**	**L_EPWE_SD**	**L_EPWE_INIT**

Note: Power up default value is: 00000000_{16}

Table 3 SIB CONTROL REGISTER

BIT	MNEMONIC	DESCRIPTION
31:8		not defined
7	**SUM_RES**	SUMMIT HARDWARE RESET Drives the reset signal to the Summit Chip. The minimum period for SUM_RES=1 is 500ns. Software should set=1, wait 500ns minimum, then set=0. There is no maximum period. Note, the Summit Chip is also held in Reset by the CPCI RST_N signal. SUM_RES is a read/write bit.
6	**GSW_INTR**	GENERATE SOFTWARE INTERRUPT Writing a 1 will generate a Software interrupt if interrupts are enabled in the configuration register. This bit is for test purposes. GSW_INTR bit is R/W. GSW_INTR is read/write.
5	**U_EPWE_LTCH**	UPPER EEPROM WRITE ENABLE LATCH, Active 1 updates the Serial Data stream compare logic. Refer to Section 3.2.18.2 U_EPWE_LTCH is write only.
4	**U_EPWE_SD**	UPPER EEPROM WRITE ENABLE SERIAL DATA, Serial Data stream used during the unlock sequence. Refer to Section 3.2.18.2. U_EPWE_SD is read/write.
3	**U_EPWE_INIT-**	UPPER EEPROM WRITE ENABLE INIT- Active 0 holds the Upper EEPROM enable logic in reset. Active 1 allows the unlock sequence. At power up or after a System Reset U_ EPWE_INTR- = 0. . U_EPWE_INIT- is read/write.
2	**L_EPWE_LTCH**	LOWER EEPROM WRITE ENABLE LATCH, Active 1 updates the Serial Data stream compare logic. Refer to Section 3.2.18.2 L_EPWE_LTCH is write only.
1	**L_EPWE_SD**	LOWER EEPROM WRITE ENABLE SERIAL DATA, Serial Data stream used during the unlock sequence. Refer to Section 3.2.18.2. L_EPWE_SD is read/write.
0	**L_EPWE_INIT-**	LOWER EEPROM WRITE ENABLE INIT- Active 0 holds the Lower EEPROM enable logic in reset. Active 1 allows the unlock sequence. At power up or after a System Reset L_ EPWE_INTR- = 0. L_EPWE_INIT- is read/write.

4.2.2.18.1.3 PDU/GASU Register (Table 4)

XX 000 008 RD/WR ONLY PDU_GASU REG

BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24
BIT 23	**BIT 22**	**BIT 21**	**BIT 20**	**BIT 19**	**BIT 18**	**BIT 17**	**BIT 16**
BIT 15	**BIT 14**	**BIT 13**	**BIT 12**	**BIT 11**	**BIT 10**	**BIT 9**	**BIT 8**
							PDU_SPR_3
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
PDU_SPR_2	**PDU_SPR_1**	**PDU_SPR_0**	**SPPSEL**	**PPON**	**PRON**	**GPON**	**GRON**

Table 4 PDU_GASU REGISTER

BIT	MNEMONIC	DESCRIPTION
31:9		not defined
8	**PDU_SPARE3**	PDU SPARE OUTPUT 3, Active 1 causes the open collector signal PDU_SPARE3- to be driven low. Active 0 causes the open collector signal to float.
7	**PDU_SPARE2**	PDU SPARE OUTPUT 2, Active 1 causes the open collector signal PDU_SPARE2- to be driven low. Active 0 causes the open collector signal to float.
6	**PDU_SPARE1**	PDU SPARE OUTPUT 1, Active 1 causes the open collector signal PDU_SPARE1- to be driven low. Active 0 causes the open collector signal to float.
5	**PDU_SPARE0**	PDU SPARE OUTPUT 0, Active 1 causes the open collector signal PDU_SPARE0- to be driven low. Active 0 causes the open collector signal to float.
4	**SPPSEL**	SPACECRAFT POWER PRIMARY SELECT, see Table 5
3	**PPON**	PDU PRIMARY ON, see Table 5
2	**PRON**	PDU REDUNDANT ON, see Table 5
1	**GPON**	GASU PRIMARY ON, When = 1, the PWR_ON_PRIM_GASU_PRIM_L will be active low and the PWR_ON_RDNT_GASU_ PRIM _L active low When = 0, the PWR_ON_PRIM_GASU_ PRIM _L will float and the PWR_ON_RDNT_GASU_ PRIM _L will float.
0	**GRON**	GASU REDUNDANT ON, When = 1, the PWR_ON_PRIM_GASU_RDNT_L will be active low and the PWR_ON_RDNT_GASU_RDNT_L active low When = 0, the PWR_ON_PRIM_GASU_RDNT_L will float and the PWR_ON_RDNT_GASU_RDNT_L will float.

At power up, all bits = 0 via the EXT_POR_L signal, No bits are cleared by cPCI RESn signal

Table 5 PDU SELECT TRUTH TABLE

REGISTER BITS			OUTPUT SIGNALS (OPEN COLLECTOR ACTIVE LOW)			
SC_PWR_PRIM_SEL (SPPSEL)	PDU_PRIM_ON (PPON)	PDU_RDNT_ON (PRON)	SC_PRIM_PWR_ PDU_PRIM_SEL_L	SC_RDNT_PWR_ PDU_PRIM_SEL_L	SC_PRIM_PWR_ PDU_RDNT_SEL_L	SC_RDNT_PWR_ PDU_RDNT_SEL_L
0	0	0	F	F	F	F
0	0	1	F	F	F	LOW
0	1	0	F	LOW	F	F
0	1	1	F	LOW	F	LOW
1	0	0	F	F	F	F
1	0	1	F	F	LOW	F
1	1	0	LOW	F	F	F
1	1	1	LOW	F	LOW	F

F=FLOAT, A float can be pulled high

4.2.2.18.1.4 Heater Control Register (Table 6)

The Heater Control Register controls the Left and Right Heater Control Boxes. This register is read/write.

XX 000 00C RD/WR HEATER CONTROL REG

BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24
BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
		LH_6_OFF	LH_5_OFF	LH_4_OFF	LH_3_OFF	LH_2_OFF	LH_1_OFF
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		RT_6_OFF	RT_5_OFF	RT_4_OFF	RT_3_OFF	RT_2_OFF	RT_1_OFF

Table 6 HEATER CONTROL REGISTER

BIT	MNEMONIC	DESCRIPTION
31:14		Not defined
13	LH_6_OFF	=1 turns off LEFT Heater 6 Primary and turns off LEFT Heater 6 Redundant =0 turns on LEFT Heater 6 Primary and turns on LEFT Heater 6 Redundant
12	LH_5_OFF	=1 turns off LEFT Heater 5 Primary and turns off LEFT Heater 5 Redundant =0 turns on LEFT Heater 5 Primary and turns on LEFT Heater 5 Redundant
11	LH_4_OFF	=1 turns off LEFT Heater 4 Primary and turns off LEFT Heater 4 Redundant =0 turns on LEFT Heater 4 Primary and turns on LEFT Heater 4 Redundant
10	LH_3_OFF	=1 turns off LEFT Heater 3 Primary and turns off LEFT Heater 3 Redundant =0 turns on LEFT Heater 3 Primary and turns on LEFT Heater 3 Redundant

BIT	MNEMONIC	DESCRIPTION
9	LH_2_OFF	=1 turns off LEFT Heater 2 Primary and turns off LEFT Heater 2 Redundant =0 turns on LEFT Heater 2 Primary and turns on LEFT Heater 2 Redundant
8	LH_1_OFF	=1 turns off LEFT Heater 1 Primary and turns off LEFT Heater 1 Redundant =0 turns on LEFT Heater 1 Primary and turns on LEFT Heater 1 Redundant
7:6		Not defined
5	RH_6_OFF	=1 turns off RIGHT Heater 6 Primary and turns off RIGHT Heater 6 Redundant =0 turns on RIGHT Heater 6 Primary and turns on RIGHT Heater 6 Redundant
4	RH _5_OFF	=1 turns off RIGHT Heater 5 Primary and turns off RIGHT Heater 5 Redundant =0 turns on RIGHT Heater 5 Primary and turns on RIGHT Heater 5 Redundant
3	RH _4_OFF	=1 turns off RIGHT Heater 4 Primary and turns off RIGHT Heater 4 Redundant =0 turns on RIGHT Heater 4 Primary and turns on RIGHT Heater 4 Redundant
2	RH _3_OFF	=1 turns off RIGHT Heater 3 Primary and turns off RIGHT Heater 3 Redundant =0 turns on RIGHT Heater 3 Primary and turns on RIGHT Heater 3 Redundant
1	RH _2_OFF	=1 turns off RIGHT Heater 2 Primary and turns off RIGHT Heater 2 Redundant =0 turns on RIGHT Heater 2 Primary and turns on RIGHT Heater 2 Redundant
0	RH _1_OFF	=1 turns off RIGHT Heater 1 Primary and turns off RIGHT Heater 1 Redundant =0 turns on RIGHT Heater 1 Primary and turns on RIGHT Heater 1 Redundant

The EXT_POR_L signal clears (=0) all heater control bits. The One-Minute Watchdog timer also clears (=0) all heater control bits and the cPCI RESn clears the heater control bits.

Note: The WDT holds the heater register in clear. Software should write the WDT register, then write the Heater register.

4.2.2.18.1.5 Watchdog Timer Init Register

The Watchdog Timer is used to clear the Heater Control Register in the event the cPCI processor becomes unstable. The Watchdog timer uses the 33Mhz cPCI clock to increment a 2^{31}-bit counter. The Watchdog timer period is actually 65.07sec (1/33Mhz x 2^{31}= 65.07sec). Writing to the Watchdog Timer Init Register will reset the Watchdog Counter = 0. If the Watchdog Timer times out, the WDT_TO status bit will be set. The WDT counter and status bit are initialized (cleared) by the CPCI RES_N signal.

XX 000 010 WR ONLY WATCHDOG TIMER INIT REG

BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24
BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

All bits are don't care. Writing anything to this register resets the One-Minute Watchdog timer.

4.2.2.18.2 1553 EEPROM

The SIB has up to eight (8) Megabytes of EEPROM. The EEPROM uses up to sixteen Austin Semiconductor AS8ER128K32-150-883C multi-chip module (MCM). Each MCM is configured as a 128K x 32 array. Each MCM is comprised of four 128K x 8 dies.

The EEPROM can only be accessed as a 32-bit DWORD. The EEPROM is divided into two (2) segments. These two (2) segments are referred to as Lower and Upper EEPROM. There are several levels of protection from inadvertently writing to EEPROM.

The SIB printed circuit card is designed to accommodate eight (8) Megabyte of EEPROM, however, the planned configuration is to only install six (6) Megabytes. There are three (3) Megabytes in the Lower bank and three (3) Megabytes in the Upper bank.

Upper and Lower EEPROM also require a special unlock sequence that is implemented in the Field Programmable Gate Array (FPGA). The processor writes a simple 12-bit sequential serial code to a bit in the Control Register. Each EEPROM bank (2) has a unique code. Either bank or both may be unlocked.

- Upper Bank Serial Code is: $CA9_{16}$
- Lower Bank Serial Code is: $D6B_{16}$

In the Control Register, There are three (6) bits used for the "unlock" sequence. Three (3) bits are used for Upper EEPROM and three (3) are used for the Lower EEPROM. They are:

- **U_EPWE_LTCH** UPPER EEPROM WRITE ENABLE LATCH
- **U_EPWE_SD** UPPER EEPROM WRITE ENABLE SERIAL DATA
- **U_EPWE_INIT-** UPPER EEPROM WRITE ENABLE INITIALIZE- (active low)

- **L_EPWE_LTCH** LOWER EEPROM WRITE ENABLE LATCH
- **L_EPWE_SD** LOWER EEPROM WRITE ENABLE SERIAL DATA
- **L_EPWE_INIT-** LOWER EEPROM WRITE ENABLE INITIALIZE- (active low)

In the Status Register, There are two (2) bits that indicate a successful "unlock" sequence and two (2) bits that indicate an access Write Error. They are:

- **UEEP_WE** UPPER EEPROM WRITE ENABLED, Upper EEPROM may be written
- **LEEP_WE** LOWER EEPROM WRITE ENABLED, Lower EEPROM may be written
- **UEEP_WER** UPPER EEPROM WRITE ENABLE ERROR
- **LEEP_WER** LOWER EEPROM WRITE ENABLE ERROR

The following sequence describes how to unlock the Upper EEPROM;

```
@ PowerUp or RESET the EEPROM is write protected
Write U_EPWE_LTCH = 0
Write U_EPWE_INIT- =1 (powerup default = 0)
Write U_EPWE_SD=1,1,0,0,1,0,1,0,1,0,0,1
Write U_EPWE_LTCH = 1
Write U_EPWE_LTCH = 0
Read UEEP_WE = 1
Write Upper EEPROM (1 to 1048576 DWORDS)
Write U_EPWE_INIT- =1
Read UEEP_WE = 0
EEPROM is write protected
```

The EEPROM allows for 1 to 128 locations to be written in a single Page Write cycle. A Page Write cycle takes 10 msec to complete. Please refer to the Austin Semiconductor AS8ER128K32 multi-chip module (MCM) data sheet. The SIB utilizes sixteen MCM’s as illustrated in Figure 12. Figure 13 illustrates the EEPROM memory map top view. Figure 14 illustrates the EEPROM Block Diagram.

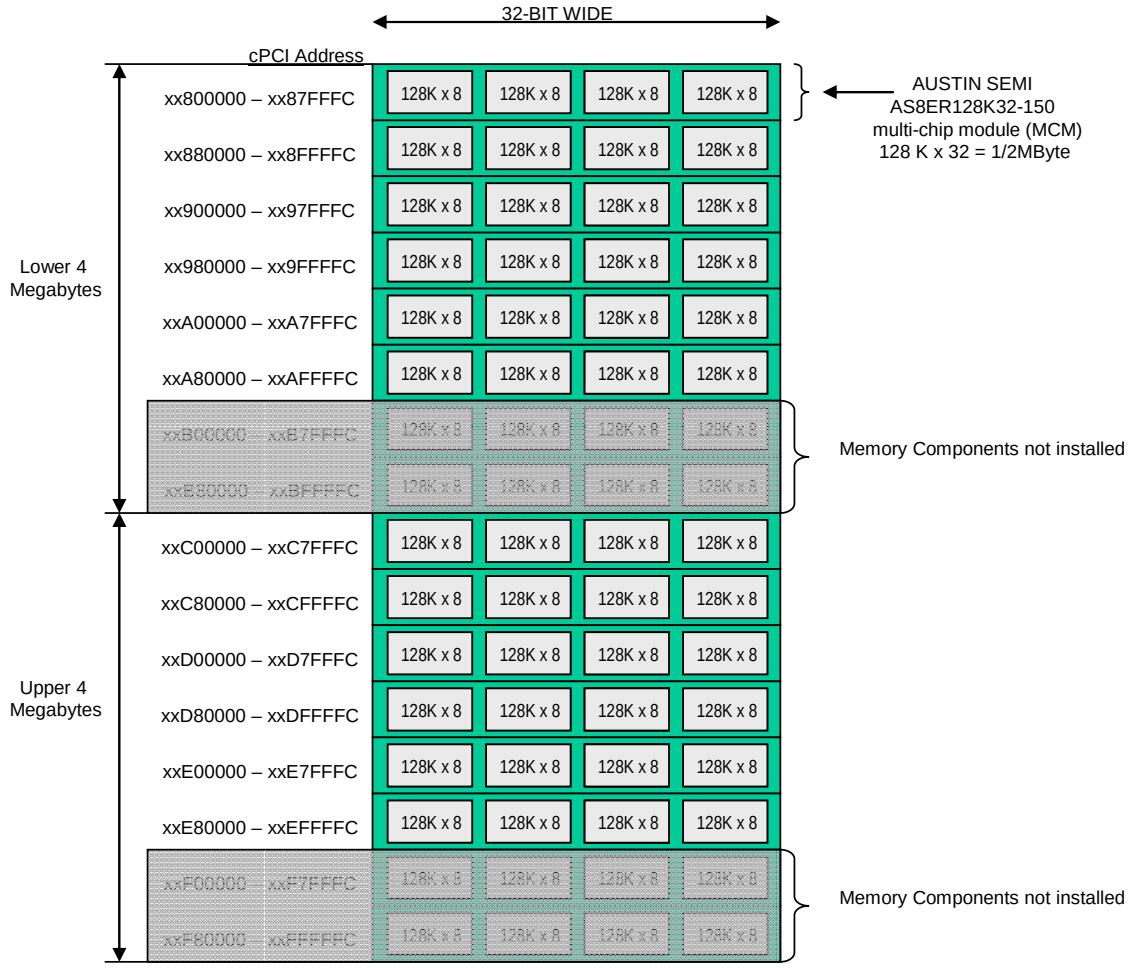

Figure 12 8-Megabyte EEPROM Layout

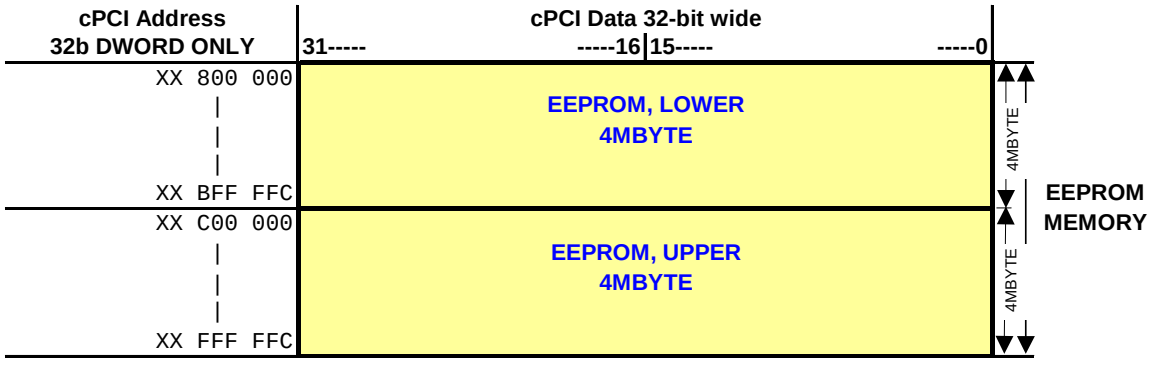

Figure 13 EEPROM Memory Map Top View

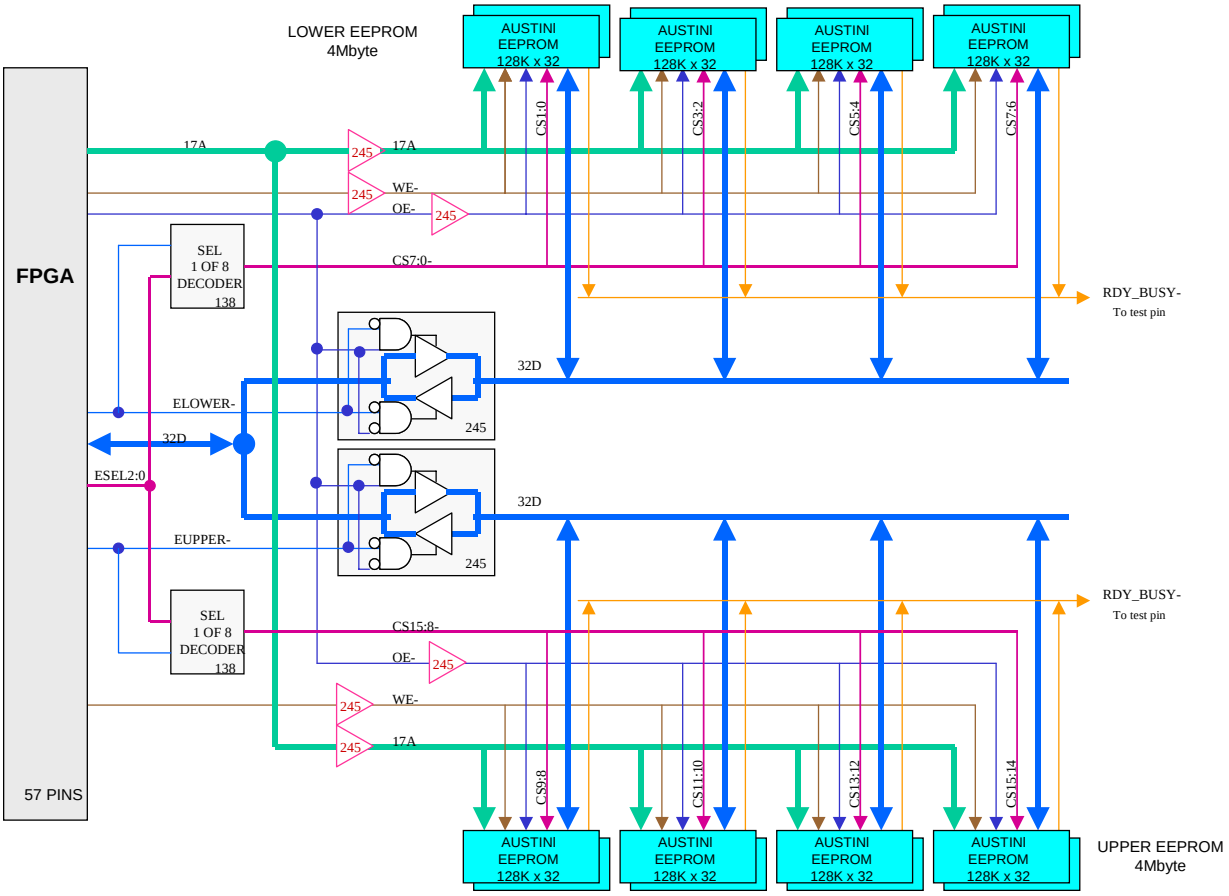

Figure 14 EEPROM BLOCK DIAGRAM

4.2.2.18.3 1553 Summit Registers

The Summit Remote Terminal register addresses are illustrated in Figure 15. Please refer to the Aeroflex UTMC Summit Family Product Handbook for bit definitions. All accesses to the

Summit registers are DWORD (32-bit) with the upper 16-bits are undefined. The Summit shall only operate in Remote Terminal Mode. The Summit 1553 Terminal Address is 3_{10}.

If the Summit is held in reset by the SUM_RES control bit, then access to the SUMMIT and the SRAM will be denied. A target abort will be issued by the SIB. The SUM_RES control bit drives the SUMMIT reset pin and also resets the FPGA's Arbiter state machine.

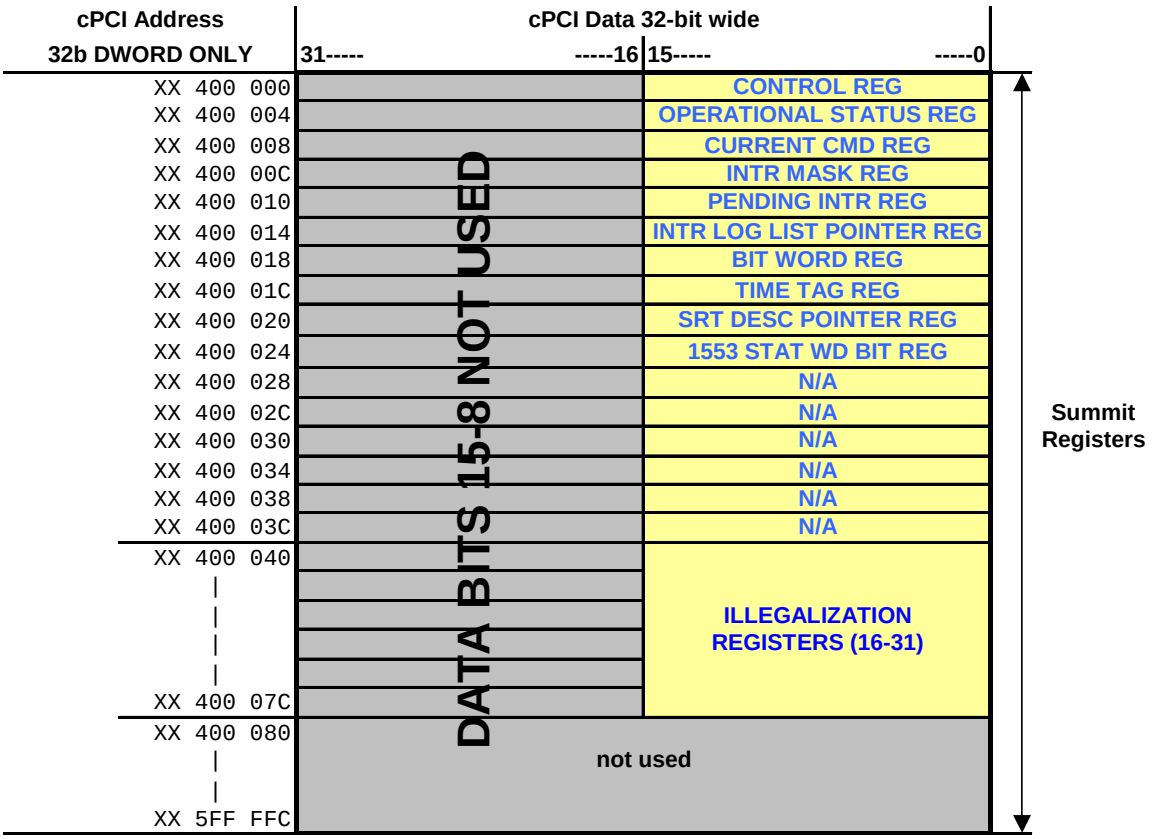

Figure 15 Summit Register Locations

4.2.2.18.4 1553 Shared RAM (Figure 16)

The SIB shares 64K Bytes of RAM between the Summit Chip and the cPCI Bus. The Summit accesses the Shared RAM as 32K x 16bit. The cPCI Bus accesses the Shared RAM as 32K x 32bit where the upper 16-bits are not used. The cPCI side can only access the Shared RAM as a DWORD (32bit). Access to the SRAM will be denied if the SUM_RES control bit is active. Access to the SRAM while SUM_RES is active will result in a target abort.

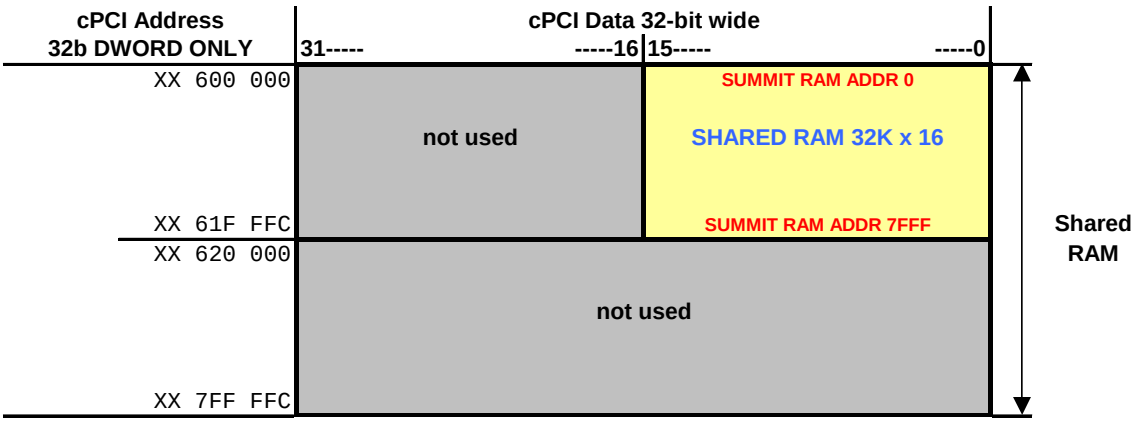

Figure 16 SUMMIT and cPCI Bus Shared RAM

5. CONNECTOR PINOUTS

5.1 J1 cPCI Interface Connector

The SIB uses J1 for the cPCI bus. The SIB is a 32-bit type. Pin assignments for the J1 cPCI interface are not listed in this document.

5.2 J2 cPCI Interface Connector (Table 7)

The SIB uses J2 for additional ground signals. The J2 connector uses a Type B 22 position connector as defined by the cPCI specification. The SIB does not require any of the 66-bit cPCI signals.

	CPCI J2/P2 TYPE B (POS 1-22)					
PIN	A	B	C	D	E	F
22						GND
21						GND
20						GND
19						GND
18						GND
17						GND
16						GND
15						GND
14						GND
13						GND
12						GND
11						GND
10						GND
9						GND
8						GND
7						GND
6						GND
5						GND
4						GND
3						GND
2						GND
1						GND

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Table 7 J2 CONNECTOR PINOUTS

5.3 J3 User I/O Interface Connector (Table 8)

The SIB uses J3 for additional power and ground signals. The J3 connector uses a Type B 19 position connector as defined by the cPCI specification.

	CPCI J3/P3 TYPE B (POS 1-19)					
PIN	**A**	**B**	**C**	**D**	**E**	**F**
19	GND	GND	GND	GND		GND
18	GND	GND	GND	GND		GND
17	GND	GND	GND	GND		GND
16	GND	GND	GND	GND		GND
15	GND	GND	GND	GND		GND
14	GND			GND		GND
13	GND	+3.3V	+3.3V	GND		GND
12	GND	+3.3V	+3.3V	GND		GND
11	GND	+3.3V	+3.3V	GND		GND
10	GND	+3.3V	+3.3V	GND		GND
9	GND	+3.3V	+3.3V	GND		GND
8	GND	+3.3V	+3.3V	GND		GND
7	GND			GND		GND
6	GND	+5V	+5V	GND		GND
5	GND	+5V	+5V	GND		GND
4	GND	+5V	+5V	GND		GND
3	GND	+5V	+5V	GND		GND
2	GND	+5V	+5V	GND		GND
1	GND	+5V	+5V	GND		GND

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Table 8 J3 CONNECTOR PINOUTS

5.4 J4 User I/O Interface Connector (Table 9)

The SIB uses J4 for the various user I/O signals. The J4 connector uses a Type A 25 position connector as defined by the cPCI specification.

	CPCI J4/P4 TYPE A (POS 1-25)					
PIN	**A**	**B**	**C**	**D**	**E**	**F**
25	SP_1	GND	GND	SP_3	GND	GND
24	SP_2	GND	GND		GND	GND
23	PDU_SPARE0_L	GND	GND	PDU_SPARE1_L	GND	GND
22	PDU_SPARE2_L	GND	GND	PDU_SPARE3_L	GND	GND
21	SC_PRIM_PWR_PDU_PRIM_SEL_L	GND	GND	SC_PRIM_PWR_PDU_RDNT_SEL_L	GND	GND
20	SC_RDNT_PWR_PDU_PRIM_SEL_L	GND	GND	SC_RDNT_PWR_PDU_RDNT_SEL_L	GND	GND
19	PWR_ON_PRIM_GASU_PRIM_L	GND	GND	PWR_ON_RDNT_GASU_PRIM_L	GND	GND
18	PWR_ON_PRIM_GASU_RDNT_L	GND		PWR_ON_RDNT_GASU_RDNT_L	GND	GND
17	RIGHT_HTR_6_RDNT_ON	GND	+3.3V	LEFT_HTR_6_RDNT_ON	GND	GND
16	RIGHT_HTR_5_RDNT_ON	GND	+3.3V	LEFT_HTR_5_RDNT_ON	GND	GND
15	RIGHT_HTR_4_RDNT_ON	GND	+3.3V	LEFT_HTR_4_RDNT_ON	GND	GND
14	KEY AREA					
13						
12						
11	RIGHT_HTR_3_RDNT_ON	GND	+3.3V	LEFT_HTR_3_RDNT_ON	GND	GND
10	RIGHT_HTR_2_RDNT_ON	GND	+3.3V	LEFT_HTR_2_RDNT_ON	GND	GND
9	RIGHT_HTR_1_RDNT_ON	GND	+3.3V	LEFT_HTR_1_RDNT_ON	GND	GND
8	RIGHT_HTR_6_PRIM_ON	GND	+3.3V	LEFT_HTR_6_PRIM_ON	GND	GND
7	RIGHT_HTR_5_PRIM_ON	GND		LEFT_HTR_5_PRIM_ON	GND	GND
6	RIGHT_HTR_4_PRIM_ON	GND	+5V	LEFT_HTR_4_PRIM_ON	GND	GND
5	RIGHT_HTR_3_PRIM_ON	GND	+5V	LEFT_HTR_3_PRIM_ON	GND	GND
4	RIGHT_HTR_2_PRIM_ON	GND	+5V	LEFT_HTR_2_PRIM_ON	GND	GND
3	RIGHT_HTR_1_PRIM_ON	GND	+5V	LEFT_HTR_1_PRIM_ON	GND	GND
2	GND	GND	+5V	GND	GND	GND
1	EXT_POR_L	GND	+5V			GND

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Table 9 J4 CONNECTOR PINOUTS

5.5 J5 User I/O Interface Connector (Table 10)

The SIB uses J5 for the various user I/O signals. The J5 connector uses a Type B connector as defined by the cPCI specification.

	CPCI J5/P5 TYPE B (POS 1-22)					
PIN	**A**	**B**	**C**	**D**	**E**	**F**
22	CH_GND	CH_GND		CH_GND	CH_GND	GND
21	CH_GND	CH_GND		CH_GND	CH_GND	GND
20	CH_GND	CH_GND		CH_GND	CH_GND	GND
19	1553_CHANNEL_A+	CH_GND		CH_GND	CH_GND	GND
18	1553_CHANNEL_A-	CH_GND		CH_GND	CH_GND	GND
17	CH_GND	CH_GND		CH_GND	CH_GND	GND
16	CH_GND	GND	+5V	CH_GND	CH_GND	GND
15	CH_GND	GND	+5V	CH_GND	CH_GND	GND
14	CH_GND	GND	+5V	CH_GND	CH_GND	GND
13	CH_GND	GND	+5V	CH_GND	CH_GND	GND
12	CH_GND	GND	+5V	CH_GND	CH_GND	GND
11	CH_GND	GND	+5V	CH_GND	CH_GND	GND
10	CH_GND	GND	+5V	CH_GND	CH_GND	GND
9	CH_GND	GND	+5V	CH_GND	CH_GND	GND
8	CH_GND	GND	+5V	CH_GND	CH_GND	GND
7	CH_GND	CH_GND		CH_GND	CH_GND	GND
6	1553_CHANNEL_B+	CH_GND		CH_GND	CH_GND	GND
5	1553_CHANNEL_B-	CH_GND		CH_GND	CH_GND	GND
4	CH_GND	CH_GND		CH_GND	CH_GND	GND
3	CH_GND	CH_GND		CH_GND	CH_GND	GND
2	CH_GND	CH_GND		CH_GND	CH_GND	GND
1	CH_GND	CH_GND		CH_GND	CH_GND	GND

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Table 10 J5 CONNECTOR PINOUTS

5.6 J6 Test Connector

The J6 Test Connector provides access to the JTAG and probe pins on the ACTEL FPGA. J6 will be installed on the EDM card and not installed on the flight card.

J6 is an array of 'Berg' type post arranged on a 2 x 6 on 0.1inch centers. Pin assignments are shown in Table 11 J6 CONNECTOR PINOUTS.:

	SIGNAL NAME	FUNCTION
PIN 1	TDI	JTAG
PIN 2	TMS	JTAG
PIN 3	TRST	JTAG
PIN 4	TDO	JTAG
PIN 5	TCK	JTAG
PIN 6	GND	
PIN 7	PROBE B	ACTEL PROBE
PIN 8	PROBE A	ACTEL PROBE
PIN 9	no connect	
PIN 10	GND	
PIN 11	EL_RDY_BSY-	EEPROM LOWER READY_BUSY-
PIN 12	EU_RDY_BSY-	EEPROM UPPER READY_BUSY-

Table 11 J6 CONNECTOR PINOUTS