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Test-stand architecture redux

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Abstract

Historically, "the GLAST test-stand" is divided at the "wire" between the embedded and host environments. This note describes a new generation of the test-stand architecture *upstream* of, and including the embedded system. This version is intended to rectify problems uncovered in the experience gained in using the present system. The goals of this new version are to:

- both rationalize and minimize the cable plant
- provide an long-term solution to power supply needs
- provide a more realistic environment in which to test subsystem electronics

These goals are intended to be realized without impacting the user's software investment in the current system.

1 References

1 "LAT Comm I/O Board - Response FIFO", LAT-TD-00593-04, by Curt Brune

2 "LAT Comm I/O Board - Triggering", LAT-TD-00597-03, by Curt Brune

3 "The LAT Communications Board: LCB design specification", LAT-TD-xxxx-D1[1], by Michael Huffer

4 Data sheet for the "MAXIM 5120 3V, 12-Bit Serial Voltage-Output DACs with Internal Reference". `hhtp://www.maxim-ic.com`

1. Cyper-docs number yet to be assigned

5 Data sheet for the “MAXIM 145 2.7V, Low-Power, 2-channel 108ksps Serial 12-Bit ADCs in 8-Pin uMAX”. hhtp://www.maxim-ic.com

1.1 The big picture

The conceit of the new architecture is that it represents a single-node version of the LAT. As such, it consists of the following components:

One module: This may include either a TEM or (engineering prototype) AEM. It of course, also includes the appropriate set of sub-system electronics connected to either the TEM or AEM.

One Power Supply Assembly (PSA): The PSA has two purposes: to emulate a tower power supply and to satisfies the power needs of the ACD. In the current test-stands there is no direct analogy for this component, as it was expected to be provided by the user. Physically, the PSA will match its flight counterpart, allowing the TEM to be mated directly to its power-supplies. The *engineering* version of the AEM will follow the physical form factor of the TEM to also allow mating to a PSA.

LAT supply: The current test-stand has no equivalent functionality, again, because power supplies requirements were satisfied by the user. The LAT expects power to supplied to it from the spacecraft to be 28 volts. This component will simply convert wall-power to 28 Volts.

One transition board: This board provides an emulation of the functionality (for a one-node LAT), normally satisfied by the PDU and GASU. This board has no direct analogy within the current test-stand configurations, however, the functionality of the mini-GLT provided currently by *one* of the comm-boards will be moved to this board. This board will be implemented as a VME module inserted into the crate currently used by your test-stand.

One LCB: A LAT Communication Board. This is an engineering board implemented on a PMC form factor rather then its flight form factor, cPCI. It occupies the PMC slots of the *Motorola* MVME 2306 currently used in your test-stand. The LCB replaces the functionality now spread across the *two* comm-boards. It provides an exact functional representation of the LCB used in flight.

One processor board: This board is (and serves the same functionality as) your test-stand’s *Motorola* MVME 2306. In addition, it will serve as the carrier for the LCB.

One VME crate: Reused from the test-stand. From an electronics perspective it need only contain two cards: a *Motorola* MVME 2306 and a transition board, both as described above.

Finally, of course, all the cabling to interface these components together will be provided. A diagram which shows these components, cables, and connections is found in Figure 1.

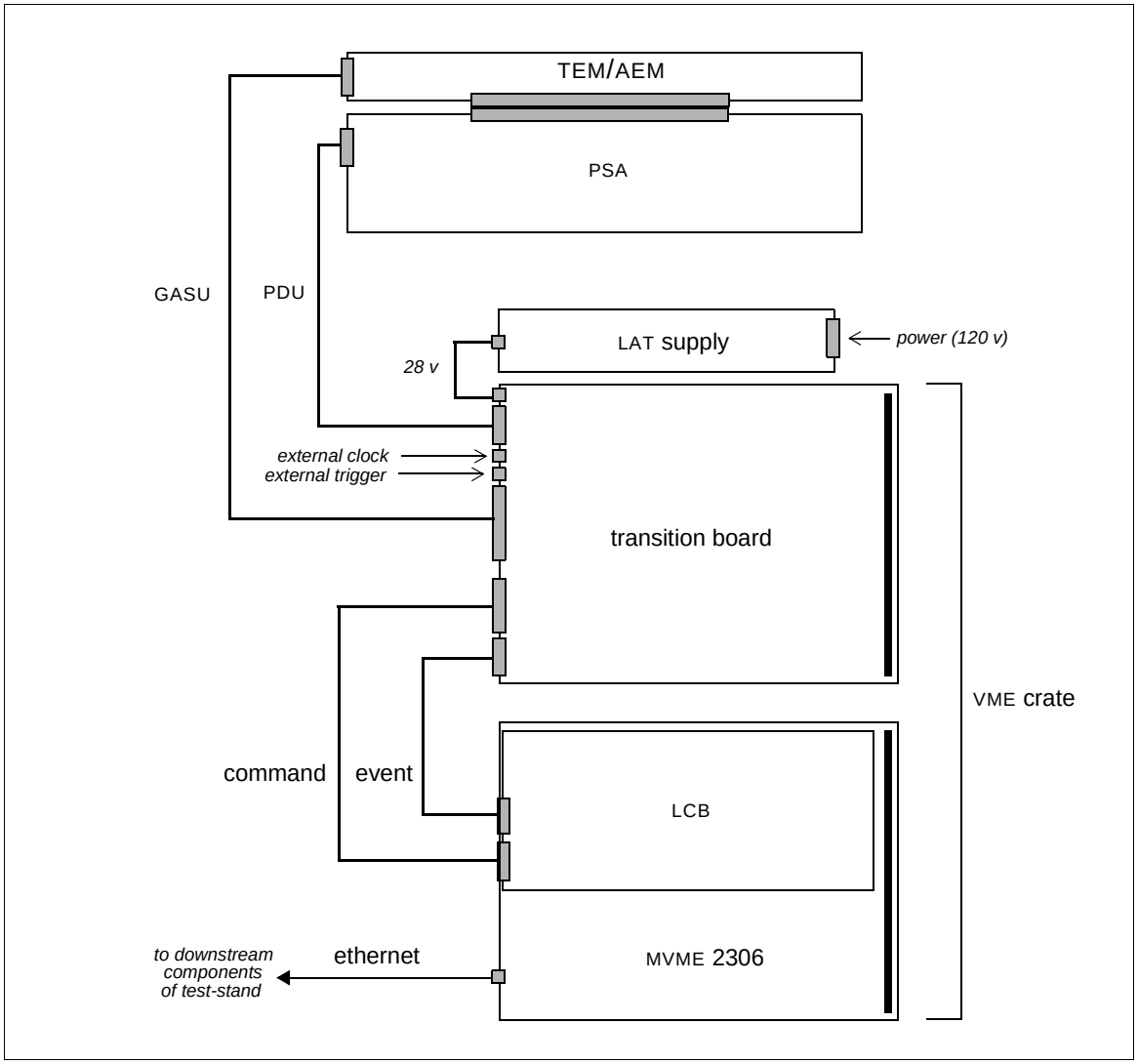

Figure 1 Test stand arraignment

1.1.1 Wrinkles

- Depending on the exact application targeted by a particular test-stand, the PSA may be only partially loaded in order to minimize costs. For example, on a test-stand targeted for NRL, it makes no sense to load power-converters for tracker related supplies. The PSA is designed such that partial loading is easy to realize and will not have any side-effects on the functionality which *is* present.

- The test-stand as described here is designed to support the *engineering* model of the AEM, not its corresponding flight article. One simply replaces the box of Figure 1 labelled TEM / AEM with the engineering version of the AEM. Everything downstream of the AEM remains unchanged and unaffected. Note, the overriding function of the *engineering* model of the AEM is to support ACD development. In flight, the functionality of the AEM is incorporated, (in some, yet not completely determined fashion) in the GASU, along with the GLT and Event Builder. From the perspective of the ACD this fact is irrelevant, as the AEM's functionality remains the same, only its physical realization and location is changed.
- The test-stand as described here will *not* support the "pseudo AEM". First, because the additional functionality provide by the new test-stand architecture is not *currently* as critical or appropriate for the ACD as it is for TEM users, and second (and more important) the time-frame for the delivery of the new test-stand articles described here is co-incident with the arrival of the "real" AEM. Thus it is intended that the ACD make the transition to the new architecture when the engineering version of the AEM arrives.

1.2 Power Supply Assembly

The Power Supply Assembly (PSA) has two functions: First, it is used as an emulation of a tower's Power Supply and second, is used to satisfy the (engineering) power supply needs of the ACD. From the perspective of the tower, the PSA has the following characteristics:

- Satisfies all the tower power supply needs, including: the TEM, calorimeter digital / analog, and tracker digital / analog. It also includes HV supplies for both calorimeter and tracker. The HV is managed through the TEM in the exact fashion as the flight article.
- Has the same mechanical and electrical characteristics as its corresponding flight article, including mechanical dimensions, placement and type of connectors. A TEM mates to the PSA in the same fashion as the flight article. Input power is 28 Volts (matching flight).
- Satisfies the same "noise" requirements as required for flight.
- May operate in thermo-vac. Thermal management can be satisfied in a fashion analogous to the flight article. Temperature of the PSA can itself be monitored.

There are however, two functional differences between the flight article and the PSA:

i. 28 Volts is brought up on an unused pin of the connector between TEM and power supply. This allows the PSA to satisfy both TEM and AEM power supply requirements.

ii. The power supply margins can be adjusted under program control. The signals necessary for this control are brought out on unused pins of the PDU connector, whose cable brings them to the transition board (see Figure 3), for conversion and programming.

The PSA consists of an aluminium box of the same dimensions as its flight article and contains a PCB with the necessary power converters, regulators, and connectors. A block diagram of the PSA is illustrated in Figure 2:

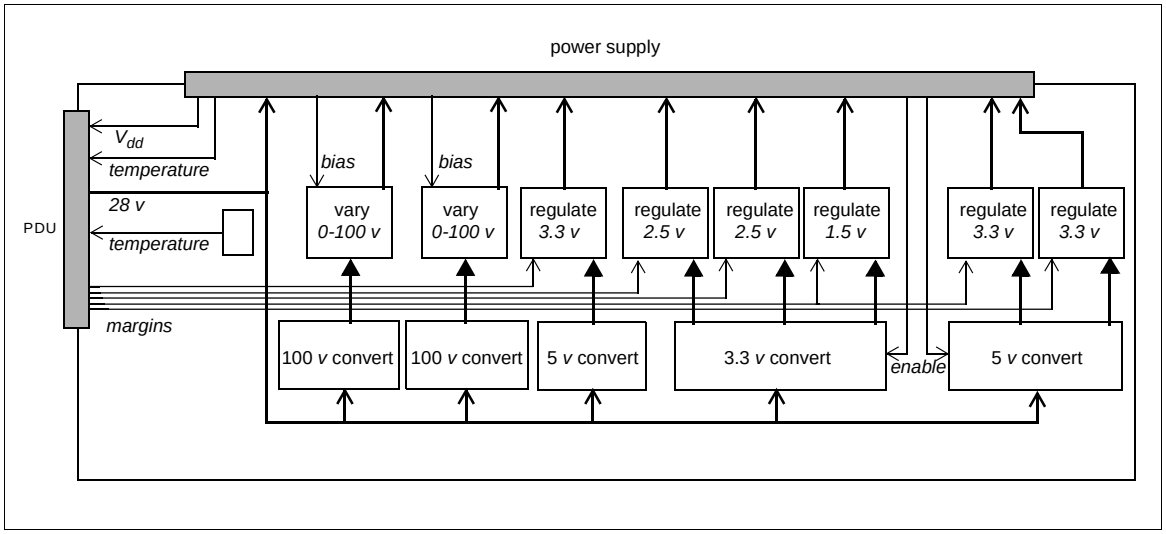

Figure 2 Power supply assembly

1.3 LAT power supply

to be described.

1.4 Transition board

The transition board is used in a one-node test-stand (for example, one tower, or one AEM) to emulate the functionality of both the PDU and GASU of the LAT. The logic and connectors for this board are all contained on a single-width, 6U VME module. This board has the following principal functions:

- Provides the system clock. This clock may be either internal or external. If internal, the clock runs at the standard LAT rate of 20 MHZ.
- Contains the functionality of the “mini-GLT” (see [2]). This include provision for an external trigger.
- Provides the same connector transition for the command fabric as would the Fanin / Fanout Unit contained on the LAT. That is, it “emulates” the *command* fabric.
- Provides the same connector transition for the event fabric as would the Event Builder Unit contained on the LAT. That is, it “emulates” the *event* fabric.

- Allows environmental monitoring of those quantities on the TEM / AEM which would in the flight article be monitored by the PDU. This includes module and power supply temperatures, as well as its supply voltage.
- Allows programmatic control over a module's power supply margins. This is an engineering *only* functionality and will not be provided in the flight article.

A block diagram of this board is illustrated in Figure 3:

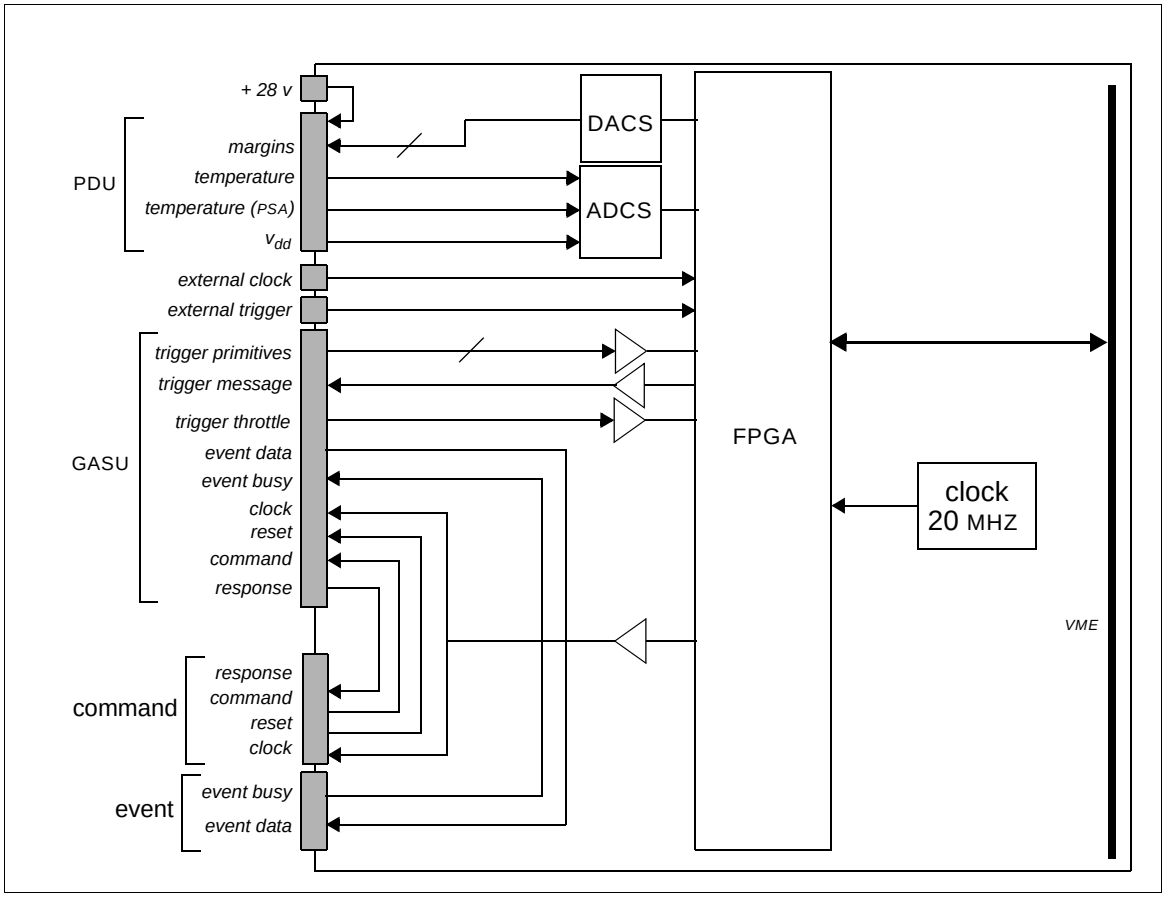

Figure 3 Transition board

1.4.1 Register model

1.4.1.1 Event Number and Tag

The message encoded and transmitted by the mini-GLT and received by a source is called a "Trigger Message". For each message sent, the mini-GLT tags the message with a sequence number. Once set, the mini-GLT will "increment" this sequence number. This register

determines both the initial and current value of the sequence number and is illustrated in Figure 4:

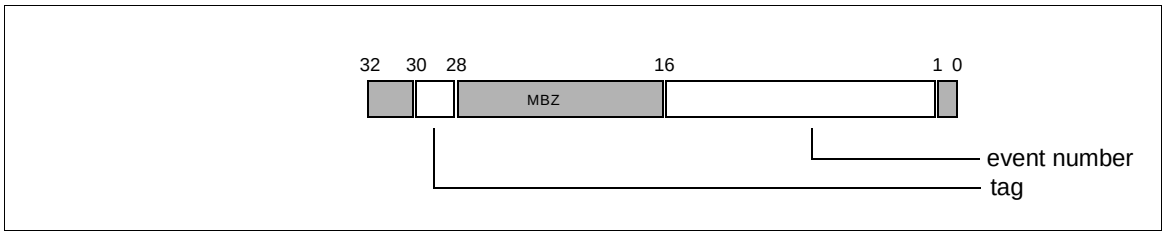

Figure 4 The sequence register

tag: The two *least* significant bits of the 17-bit event sequence number. The remaining 15-bits of the sequence number are contained in the ***event number*** field.

event number: The 15 most significant bits of the 17-bit event sequence number. The low-order two bits of the sequence number are contained in the ***tag*** field.

1.4.1.2 Trigger Message

The message encoded and transmitted by the mini-GLT and received by a source is called a "Trigger Message". The mini-GLT allows the user program control over the contents of a message when sent. This control is expressed with the register illustrated in Figure 5:

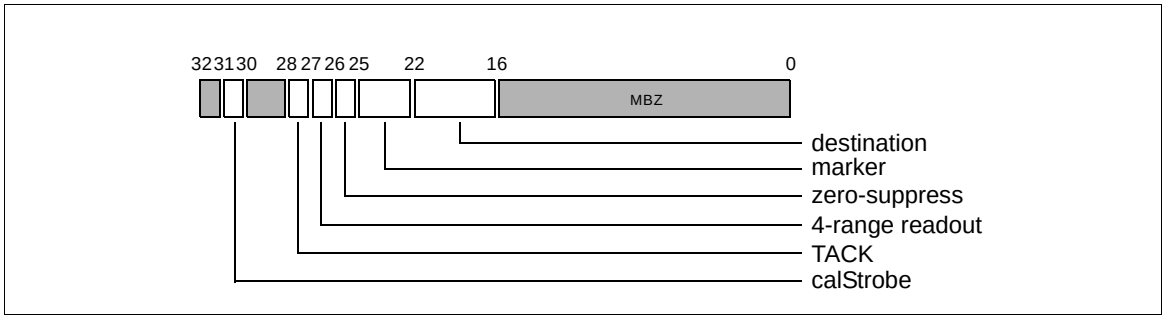

Figure 5 The trigger message register

calStrobe: Specifies what type of command should *first* be issued by a module to its Front-End Electronics. If this field is true (*set*), the first command emitted is a `calStrobe`. If the field is false (*clear*), the first command emitted is a TACK (see also the ***TACK*** field).

TACK: Specifies whether a *second* command should be issued by the TEM to its Front-End Electronics. If this field is true (*set*), a second command is emitted (following the first command specified in the ***calStrobe*** field). This second command is always a TACK. If the field is false (*clear*), a second command is *not* emitted.

4-range readout: If this field is *set*, the calorimeter Front-End Electronics will emit all four ranges of its event data. If *clear*, the calorimeter will auto-range and send the one appropriate range for its event data.

zero suppress: If this field is *set*, a TEM or AEM will zero suppress event data emitted by the Calorimeter or ACD Front-End electronics. If this field is *clear*, the TEM or AEM will *not* zero suppress any event data emitted by the Calorimeter or ACD.

marker: Used by flight software in order to insert markers at well-known times into the event stream.

destination: Specifies (if an event is to be emitted) the destination of the event data.

1.4.1.3 Trigger Source Mask

The mini-GLT on the transition board receives five different types of trigger requests. Each one of these trigger request *sources* can be masked off from trigger consideration using the register illustrated in Figure 6. The mini-GLT will mask the value of this register against transitions on the trigger request lines and then OR the result. If the result is *true* and the throttle line is *false*, a trigger message will be generated. This is a *mask* register. Only if a field is *set*, will the corresponding line be considered.

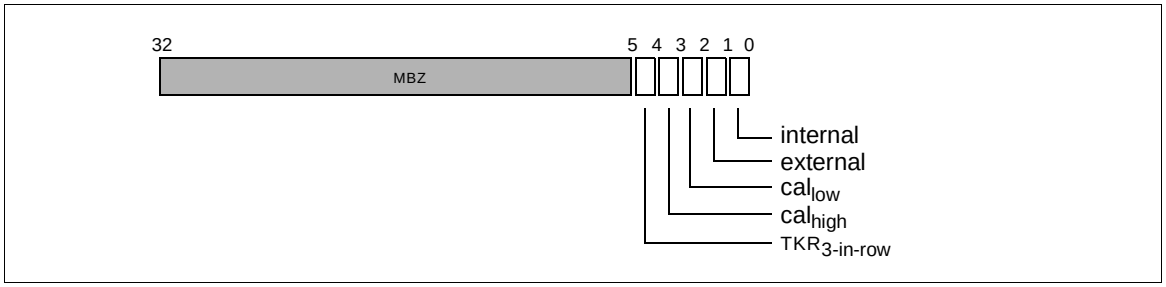

Figure 6 Trigger source mask

1.4.1.4 Generate trigger

Writing to this register will generate a one-shot signal on the *internal* trigger request line. If this line is *not* masked (see Figure 6) and the trigger is *not* throttled, a trigger message will be transmitted. The value written to this register is ignored. Reading this register will return unpredictable results.

1.4.1.5 Test features

The transition board has the capability to defeat certain standard features, which in the normal course of operation would always be enabled. This functionality is present only to allow *testing* of those features. One should think long and hard before modifying the default value of this register.

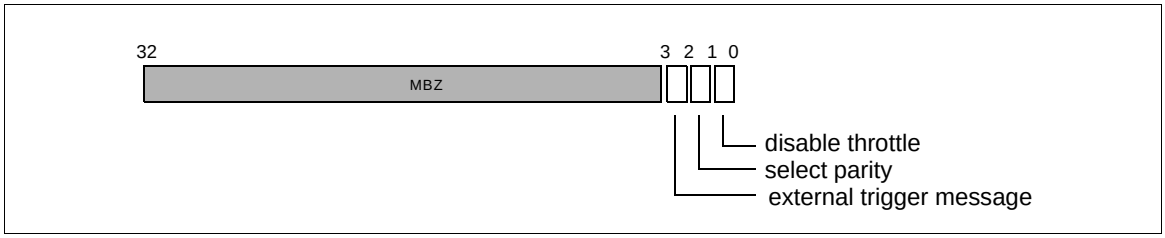

Figure 7 Test features

disable throttle: If *set*, the mini-GLT ignores the state of the throttle line sent by the TEM or AEM.

select parity: Determines whether the parity generated by the mini-GLT for a trigger message is *odd* or *even*. If the field is *clear, odd* parity is generated. If the field is *set*, *even* parity is generated.

external trigger message: Determines the type of trigger message sent in response to an external trigger request (see Figure 6). If the field is *clear*, the CALSTROBE and TACK fields of the trigger message will be clear. If this field is *set*, the value of these fields will determined by the values found in the trigger message register (see Figure 5).

1.4.1.6 Margin DACs

There are five registers used to change the margins of the different power supplies of the PSA (see Section 1.2). The correspondence between register number and power supply is enumerated in Table 1. The structure of each of these registers is identical and is illustrated in Figure 8. In reality each register is “fronting” for an individual DAC. The DAC is a commercial part, the MAXIM 5121 (see [4]). The low-order 16 bits of this register reflect the value of the 5121’s so-called “input register” and has the structure documented in Table 1 of [4]. Note, that after writing this register, it takes a certain amount of “settling time” before the newly written value appears in this register. The ***valid*** field of this register may be used to determine when, after writing this register, the value has settled. While the transition board is loading a new value, the value of this field is *clear*. Once, the board has completed loading, the value of this field will be *set*.

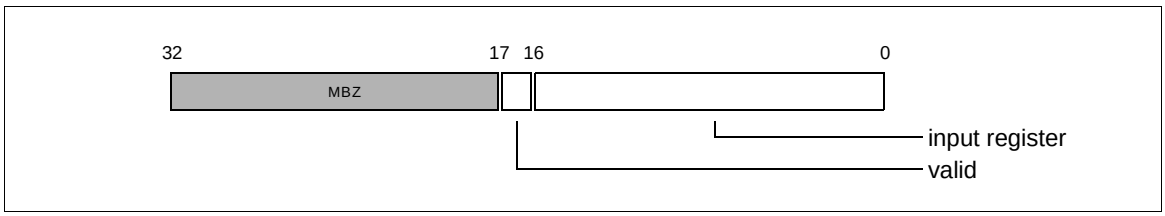

Figure 8 Margin DAC for PSA power supplies

Table 1 Power supply margin registers

Power Supply(s)	register number
TEM/AEM 3.3 volts	to be defined
CAL/ACD 3.3 volts (digital)	to be defined
TKR 2.5 volts (digital)	to be defined
TKR 1.5 volts (analog)	to be defined
CAL/TKR 3.3 and 2.5 volts (analog)	to be defined
Total	**5**

1.4.1.7 Monitoring ADCs

The transition board has the capability to monitor various analog quantities brought from the TEM / AEM and PSA on the PDU cable (see Section 1.2). The correspondence between register number and monitored quantity is enumerated in Table 2. The structure of each of these registers is identical and is illustrated in Figure 9. In reality each register is “fronting” for an individual ADC. The ADC is a commercial part, the MAXIM 145 (see [5]). The low-order 12 bits of this register reflect the converted value. To begin conversion, the user *writes* the register (the value written is ignored). This will force the ***valid*** field to be *cleared*. At a fixed time later, conversion is complete and the ***valid*** field will be *set*. If the register is written while a conversion is in progress, the write is ignored.

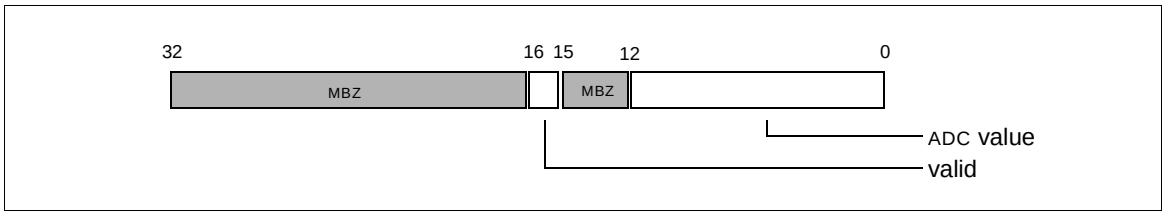

Figure 9 Monitoring ADC register

Table 2 Monitor registers

quantity monitored	register number
TEM/AEM VDD (A)	to be defined
TEM/AEM Temperature (A)	to be defined
PSA Temperature (A)	to be defined
TEM/AEM VDD (B)	to be defined
TEM/AEM Temperature (B)	to be defined
PSA Temperature (B)	to be defined
Total	**6**

1.5 LCB

See [3], with particular emphasis on Appendix B.

1.6 Cables and connectors

Table 3 PDU cable (3M 25 pin D-sub high density, MN # 7485-69-1)

I/O signal name	wires	total pins[a]
28V (power)	4	4 *x* 2 = 8
Temperture (module)	2	2 *x* 2 = 4
Temperture (power supply)	2	2 *x* 2 = 4
VDD (module)	2	2 *x* 2 = 4
power supply margins	5	5 *x* 1[b]= 5
Total		**25**

a. Unless noted, all signals are redundant, therefore wire count is doubled for each signal.

b. As these signals are not used for flight, redundancy is not required

Table 4 GASU cable (51pin micro-D)

I/O signal name	wires	LVDS?	redundant?	total wires
EVENT_DATA	1	yes	yes	1 *x* 2 *x* 2 = 4
EVENT_BUSY	1	yes	yes	1 *x* 2 *x* 2 = 4
TRIGGER_CAL_LOW	1	yes	yes	1 *x* 2 *x* 2 = 4
TRIGGER_CAL_HIGH	1	yes	yes	1 *x* 2 *x* 2 = 4
TRIGGER_TRACKER	1	yes	yes	1 *x* 2 *x* 2 = 4
TRIGGER_THROTTLE	1	yes	yes	1 *x* 2 *x* 2 = 4
TRIGGER_MESSAGE	1	yes	yes	1 *x* 2 *x* 2 = 4
CLOCK	1	yes	yes	1 *x* 2 *x* 2 = 4
RESET	1	yes	yes	1 *x* 2 *x* 2 = 4
RESPONSE	1	yes	yes	1 *x* 2 *x* 2 = 4
COMMAND	1	yes	yes	1 *x* 2 *x* 2 = 4
Total				**44**

Table 5 Command cable (25 pin micro-D)

I/O signal name	wires	total wires[a]
CLOCK	1	1 *x* 2 *x* 2 = 4
RESET	1	1 *x* 2 *x* 2 = 4
RESPONSE	1	1 *x* 2 *x* 2 = 4
COMMAND	1	1 *x* 2 *x* 2 = 4
Total		**16**

a. All signals are LVDS and are doubled for redundancy

Table 6 Event cable (25 pin micro-D)

I/O signal name	wires	total wires[a]
DATA_A	8	8 *x* 2 = 16
BUSY_A	1	1 *x* 2 = 2
DATA_B	1[b]	1 *x* 2 = 2
BUSY_B	1	1 *x* 2 = 2
Total		**22**

a. All signals are LVDS

b. For the engineering LCB, the redundant data path will use only *one* of its eight wires

1.7 Summary

1.7.1 What do you throw away?

- The two comm-boards
- Any “home-brew” power-supply solution
- The rats-nest of cabling you currently love and enjoy

1.7.2 What do you keep?

- The same programming model and consequently your own software investment. Some new functionality is provided, which, if used (your choice), could require additional software development on your part.
- Your VME crate
- Your embedded processor (*Motorola* MVME 2306)
- Everything *downstream* of the architecture described here

1.7.3 What do you gain?

- A real, long-term solution to your power supply requirements. Note: this includes flight version control of your High Voltage.

- Cleaner, more understandable cabling / module plant. Hopefully this will allow more straightforward installation of a test-stand, as well as easing the maintenance burden.
- Higher fidelity emulation of the (LAT) environment in which your detector and electronics will eventually reside. This includes not only additional operational control and monitoring over the tower or ACD, but also a realistic electronics noise environment.
- Better performance. The LCB's event throughput will be at least a factor of 10 better then the current comm-board. Command / response performance will also improve.