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	Subsystem/Office Anticoincidence Detector Subsystem	
Document Title **ACD Functional Test Plans (Comprehensive Performance Test)**		

Gamma-ray Large Area Space Telescope (GLAST)

Large Area Telescope (LAT)

ACD Functional Test Plans (Comprehensive Performance Test)

DRAFT

CHANGE HISTORY LOG

Revision	Effective Date	Description of Changes

Prepared by: _____ Date: _____

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1. Purpose

The purpose of the Comprehensive Performance Test (CPT) is to define the most complete functional testing needed to verify the performance of the GLAST LAT ACD. Other test plans, including Aliveness, Limited Functional, and Full Functional Tests, are subsets of this plan. For each test plan there is a parallel detailed test procedure.

2. Acronyms and Definitions

ACD	The LAT Anti-Coincidence Detector Subsystem
ADC	Analog-to-Digital Converter
AEM	ACD Electronics Module
ASIC	Application Specific Integrated Circuits
BEA	Base Electronics Assembly
CAL	The LAT Calorimeter Subsystem
CPT	Comprehensive Performance Test
DAQ	Data Acquisition
EGSE	Electrical Ground Support Equipment
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
FM	Flight Module
FMEA	Failure Mode Effect Analysis
FREE	Front End Electronics
GAFE	GLAST ACD Front End – Analog ASIC
GARC	GLAST ACD Readout Controller – Digital ASIC
GEVS	General Environmental Verification Specification
GLAST	Gamma-ray Large Area Space Telescope
HVBS	High Voltage Bias Supply
ICD	Interface Control Document
IDT	Instrument Development Team
I&T	Integration and Test
IRD	Interface Requirements Document
JSC	Johnson Space Center
LAT	Large Area Telescope
MGSE	Mechanical Ground Support Equipment
MLI	Multi-Layer Insulation

MPLS	Multi-purpose Lift Sling
PCB	Printed Circuit Board
PDR	Preliminary Design Review
PMT	Photomultiplier Tube
PVM	Performance Verification Matrix
QA	Quality Assurance
SCL	Spacecraft Command Language
SEL	Single Event Latch-up
SEU	Single Event Upset
SLAC	Stanford Linear Accelerator Center
TACK	Trigger Acknowledge
TDA	Tile Detector Assembly
T&DF	Trigger and Data Flow Subsystem (LAT)
TBD	To Be Determined
TBR	To Be Resolved
TSA	Tile Shell Assembly
TSS	Thermal Synthesizer System
TKR	The LAT Tracker Subsystem
VME	Versa Module Eurocard
WBS	Work Breakdown Structure
WOA	Work Order Authorization

Comprehensive Performance Test (CPT) – a series of functional tests that exercises all functions of the ACD system and includes an absolute measurement of all the ACD tile efficiencies.

Full Functional Test (FFT) - a series of functional tests that exercises all functions of the ACD system except an absolute measurement of all the ACD tile efficiencies.

Limited Functional Test (LFT) - a series of functional tests that exercises all major functions of the ACD system.

Aliveness Test (FFT) - a functional test that turns on the ACD in a nominal state and verifies basic operation of all channels.

3. Applicable Documents

Documents relevant to the ACD Functional Test Plans include the following.

1. LAT-SS-00016, LAT ACD Subsystem Requirements – Level III Specification
2. LAT-SS-00352, LAT ACD Electronics Requirements – Level IV Specification
3. LAT-SS-00437, LAT ACD Mechanical Requirements – Level IV Specification
4. LAT-MD-00039-01, LAT Performance Assurance Implementation Plan (PAIP)
5. LAT-MD-00099-002, LAT EEE Parts Program Control Plan
6. LAT-SS-00107-1, LAT Mechanical Parts Plan
7. LAT-MD-00078-01, LAT System Safety Program Plan (SSPP)
8. ACD-QA-8001, ACD Quality Plan
9. LAT-TD-00720-D1 ACD Phototube Helium Sensitivity
10. LAT-DS-00740-1 Temperature Characteristics of ACD Photomultiplier Tubes
11. Response to RFQ 5-09742, Hamamatsu Photomultiplier Tube Proposal
12. LAT-MD-00404-01, LAT Contamination Control Plan
13. LAT ACD Subsystem Verification Table/Plan

4. ACD Functional Testing

Testing described in the Comprehensive Performance Test (CPT) includes operational tests that will be performed after the assembly of the ACD. It assumes control of the ACD by an EGSE system with a high-level command system, details of which are TBD, and readout of ACD data through the EGSE data stream, with specific displays to be defined as needed.

Because the CPT is a fairly exhaustive (i.e. time-consuming) test, it will be performed on a limited basis. Subsections of the CPT will be used for subassembly testing, aliveness testing, limited functional testing, and full (but not comprehensive) functional testing.

The CPT calls out specific tests that verify ACD Level IV requirements, as indicated in the ACD Subsystem Verification Table/Plan, and referenced by Level IV requirement number.

Each test plan has a parallel test procedure that gives step-by-step instructions for the testing. Because each of the 194 channels is unique, much of the testing must be automated.

5. ACD Comprehensive Performance Test Plan

Step	Function	Commands	Displays	Analysis (reference to Level IV requirements verification in parentheses)
Turn-On/Low Voltage Checkout				
1	Power on primary AEM electronics	Turn on primary AEM power	AEM Currents/voltages	Compare with stored reference values
2	Power on FREE cards	Turn on low-voltage power Send read command for all registers 194 x 11 GAFE registers, 12 x 42 GARC registers	ACD Currents/voltages 24 FREE V 2 FREE I Temperatures Shell BEA PMT (4) FREE (12)	Compare with stored reference values (28 V, 3.3 V) Verify default state as in ICD. Verify on/off commands (5.14.3) Record power in low-voltage state Verify temperatures (5.9.10)
3	Configure nominal settings	Set 194 x 6 GAFE registers. Set 12 x 39 GARC registers. Read back all. NOT using zero-suppress mode.	Command register See Appendix C for sample display page for these.	Compare with stored reference configuration Verify commanding (5.14.4, 5.14.5, 5.14.8) Verify digital housekeeping (5.9.9)
4	Determine pedestals	Send TACKs to each channel (194)	PHA histogram	Determine location and width of pedestal for each channel
5	Confirm test charge injection capability	Test Charge injection – GAFE CONFIG, TCI_DAC. 194 GAFEs x 2 levels	Rates (AEM) PHA histogram	Verify test pulse injection (5.9.8) – VETO and both PHA ranges
6	Raise/lower VETO thresholds	Change thresholds, VETO_DAC Adjust charge injection, TCI_DAC 194 GAFEs	Command register Rates PHA histogram	Rate v. commanded input Compare with stored reference values Verify test pulse injection level (5.9.8) Verify adjustable VETO threshold (5.3, 5.14.4)

Step	Function	Commands	Displays	Analysis (reference to Level IV requirements verification in parentheses)
7	Raise/lower HLD threshold	Change thresholds, HLD_DAC Adjust charge injection. TCI_DAC 194 GAFEs	Command register Rate PHA histogram	Rate v. commanded input Compare with stored reference values Verify adjustable HLD threshold (5.6, 5.14.5)
8	Compare VETO_AEM with VETO_Hitmap	Generate TACK from ACD using charge injection. 194 GAFEs	Command register Rates	Rates v. threshold Compare with stored reference values Verify functioning of TACK (5.7, 5.14.7) Compare rates (5.8.4, 5.9)
9	Verify low-range PHA	Generate TACK from ACD using charge injection. Adjust charge to different levels, CONFIG_REG, TCI_DAC 194 GAFEs	Command register PHA	Verify functioning of TACK (5.7, 5.14.7) Verify low-range PHA (5.9.3) Calibrate PHA
10	Verify high-range PHA	Generate TACK from ACD using charge injection Adjust charge to different levels CONFIG_REG, TCI_DAC 194 GAFEs	Command register PHA	Verify functioning of TACK (5.7, 5.14.7) Verify high-range PHA (5.9.3) Calibrate PHA
11	Verify zero-suppress	Generate TACK from ACD using charge injection Turn on zero-suppress. GARC mode. PHA Thresholds (194 GAFEs), 12 GARCs Adjust threshold. CONFIG_REG, TCI_DAC 194 GAFEs	Command register PHA	Verify functioning of TACK (5.14.7) Verify PHA not transmitted for low values in zero-suppress mode (5.9.3)

Step	Function	Commands	Displays	Analysis (reference to Level IV requirements verification in parentheses)
12	Integral non-linearity	Generate TACK from ACD using charge injection Adjust charge in steps. TCI_DAC 194 GAFEs x 64 steps	Command register PHA	Verify PHA integral non-linearity (5.9.5)
High Voltage Testing				
13	Check light-tightness	Turn on HVBSA, adjust to a low level, HVBS, GARC mode, then increase HVBS. 12 GARCs x TBD steps. Set VETO thresholds to nominal values 194 GAFEs	Rates HV monitor PHA	Compare rates with stored values.
14	Power on primary HVBS	Turn on HVBSA, adjust to nominal values for tubes. HVBS, GARC mode, Set VETO thresholds to nominal values VETO_DAC 194 GAFEs	Rates HV monitor PHA	Verify non-zero rates and PHA values (5.2). Compare rates with stored values.
15	Raise/lower HV	Change HV HVBS 12 GARCs	Rates Command register	Rates v. HV Compare with stored reference values Verify HV commanding (5.14.2)
16	Collect PHA spectra (short) Self-triggered gain test	Generate TACK from ACD 194 GAFEs	PHA spectra	Calculate pedestals Fit spectra with expected shape Compare with stored reference values Verify pulse digitization (5.9.3) See Appendix A.

Step	Function	Commands	Displays	Analysis (reference to Level IV requirements verification in parentheses)
17	Determine absolute thresholds	Generate TACK from ACD Adjust VETO thresholds VETO_DAC 194 GAFEs	PHA spectra	Compare with stored reference values Compute thresholds in MIPs (5.3)
18	Re-check pedestals	Send TACKs to each channel (194)	PHA histogram	Determine location and width of pedestal for each channel
19	Measure false VETO	Lower HV HVBS	Rates	Verify false VETO rates (5.4)
20	Test discriminator masking	Change discriminator mask PHA EN0 PHA EN1 12 GARCs 194 GAFEs 2 levels	Rates	Compare with stored reference values Verify discriminator masking (5.8.7)
21	Limit and state change checking	Enable limit checking and state change checking by EGSE	Messages for state changes, highlighted parameter values if out of limit	Compare currents, voltages, temperatures with a limit table. Compare register states with a nominal configuration table.
22	Gain calibration test Collect PHA spectra (long)	Generate TACK from ACD	Gated PHA spectra	Trigger on VETO signal from any tile, use this to gate PHAs for all other tiles in a selected pattern Calculate pedestals Fit spectra with expected shape Compare with stored reference values See Appendix B
23	SAA Mode test	SAA signal SAA	Rates, HV monitor	Compare with stored reference values Verify command works , mode change takes place, and notification done (5.14.9, 5.14.10) Measure power in this configuration.
24	Power measurement	N.A.	Currents, voltages	Measure total power when operating (5.16)
Repeat HV tests with secondary HV Bias supplies				

Step	Function	Commands	Displays	Analysis (reference to Level IV requirements verification in parentheses)
25	Check light-tightness	Turn on HVBSB, adjust to a low level, HVBS, GARC mode, then increase HVBS. 12 GARCs x TBD steps. Set VETO thresholds to nominal values 194 GAFEs	Rates HV monitor PHA	Compare rates with stored values.
26	Power on secondary HVBS	Turn on HVBSB, adjust to nominal values for tubes. HVBS, GARC mode, Set VETO thresholds to nominal values VETO_DAC 194 GAFEs	Rates HV monitor PHA	Verify non-zero rates and PHA values (5.2). Compare rates with stored values.
27	Raise/lower HV	Change HV HVBS 12 GARCs	Rates Command register	Rates v. HV Compare with stored reference values Verify HV commanding (5.14.2)
28	Collect PHA spectra (short) Self-triggered gain test	Generate TACK from ACD 194 GAFEs	PHA spectra	Calculate pedestals Fit spectra with expected shape Compare with stored reference values Verify pulse digitization (5.9.3) See Appendix A.
29	Determine absolute thresholds	Generate TACK from ACD Adjust VETO thresholds VETO_DAC 194 GAFEs	PHA spectra	Compare with stored reference values Compute thresholds in MIPs (5.3)
30	Measure false VETO	Lower HV HVBS	Rates	Verify false VETO rates (5.4)

Step	Function	Commands	Displays	Analysis (reference to Level IV requirements verification in parentheses)
31	Test discriminator masking	Change discriminator mask PHA EN0 PHA EN1 12 GARCs 194 GAFEs	Rates	Compare with stored reference values Verify discriminator masking (5.8.7)
32	Gain calibration test Collect PHA spectra (long)	Generate TACK from ACD	Gated PHA spectra	Trigger on VETO signal from any tile, use this to gate PHAs for all other tiles in a selected pattern Calculate pedestals Fit spectra with expected shape Compare with stored reference values See Appendix B
33	SAA Mode test	SAA signal SAA	Rates, HV monitor	Compare with stored reference values Verify command works , mode change takes place, and notification done (5.14.9, 5.14.10)
34	Power measurement	N.A.	Currents, voltages	Measure total power when operating (5.16) Compare with primary HVBS power.
Repeat some tests with secondary AEM				
35	Power on secondary AEM electronics	Turn on secondary AEM power	AEM Currents/voltages	Compare with stored reference values

Step	Function	Commands	Displays	Analysis (reference to Level IV requirements verification in parentheses)
36	Power on FREE cards	Turn on low-voltage power Send read command for all registers 194 x 11 GAFE registers, 12 x 42 GARC registers	ACD Currents/voltages 24 FREE V 2 FREE I Temperatures Shell BEA PMT (4) FREE (12)	Compare with stored reference values (28 V, 3.3 V) Verify default state as in ICD. Verify on/off commands (5.14.3) Verify temperatures (5.9.10)
37	Configure nominal settings	Set 194 x 6 GAFE registers. Set 12 x 39 GARC registers. Read back all.	Command register See Appendix C for sample display page for these.	Compare with stored reference configuration Verify commanding (5.14.4, 5.14.5, 5.14.8) Verify digital housekeeping (5.9.9)
38	Confirm test charge injection capability	Test Charge injection – GAFE CONFIG, TCI_DAC. 194 GAFEs x 2 levels	Rates (AEM) PHA histogram	Verify test pulse injection (5.9.8) – VETO and both PHA ranges
39	Check light-tightness	Turn on HVBSA, adjust to a low level, HVBS, GARC mode, then increase HVBS. 12 GARCs x TBD steps. Set VETO thresholds to nominal values 194 GAFEs	Rates HV monitor PHA	Compare rates with stored values.

Step	Function	Commands	Displays	Analysis (reference to Level IV requirements verification in parentheses)
40	Power on primary HVBS	Turn on HVBSA, adjust to nominal values for tubes. HVBS, GARC mode, Set VETO thresholds to nominal values VETO_DAC 194 GAFEs	Rates HV monitor PHA	Verify non-zero rates and PHA values (5.2). Compare rates with stored values.
41	Raise/lower HV	Change HV HVBS 12 GARCs	Rates Command register	Rates v. HV Compare with stored reference values Verify HV commanding (5.14.2)
42	Collect PHA spectra (short) Self-triggered gain test	Generate TACK from ACD 194 GAFEs	PHA spectra	Calculate pedestals Fit spectra with expected shape Compare with stored reference values Verify pulse digitization (5.9.3) See Appendix A.
Efficiency Testing				
43	Efficiency test – requires ACD in three different orientations. (very long runs)	Generate TACK from ACD	Gated PHA spectra	Trigger on VETO signal from any tile, use this to gate PHAs for all other tiles in a selected pattern Calculate pedestals Fit spectra with expected shape Compare with stored reference values that have absolute efficiency calibration. (5.2) See Appendix B
44	Determine latency	External gate from muon telescope to generate TACK Delay box	Rates, PHA spectra	Add and subtract delay until VETO signals and PHA signals are no longer seen (5.8.1)
45	High-rate protection	Configure AEM for limit checking on tile rates	Rates, HV	Use radioactive source to force tile rate above 10 KHz, watch for SAA command to reduce HV.

6. Redundancy (Cross-Strapping) Test Plan

Although the ACD is not fully redundant, there are parts of the system that have independent parallel components, namely the AEM and the HVBS (note that all FREE cards and all phototubes are used for normal operation). Tests should involve these independent subsystems under these guidelines:

- We wish to exercise the primary and secondary systems approximately equally, in order to gain confidence that we understand any possible performance differences and to assure that "infant mortality" of the systems is not an issue.

- One approach to achieving this goal: A functional test should not always start with the primary AEM and the primary HVBS, but cycle through the four combinations (Primary-Primary, Primary-Secondary, Secondary-Primary, Secondary-Secondary). Separate procedures may be needed.

- If both primary and secondary AEMs are being tested within one procedure, the alternate (whichever it is) does not need to repeat all the tests done on the first AEM. The VETO signals are distinct, as are the thermistors, but commands and serial data (?) go through the same circuitry on the GARC. For this reason, a sample of commands and data will be adequate to confirm performance.

7. Shorter Versions of Functional Testing

Aliveness test – steps 1, 2, 3, 13, 14, 16.

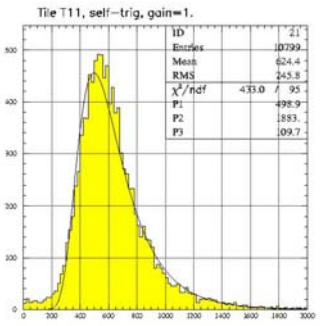
Abbreviated functional test – steps 1, 2, 3, 4, 5, 8, 9, 11, 13, 14, 16, 17, 21, 22

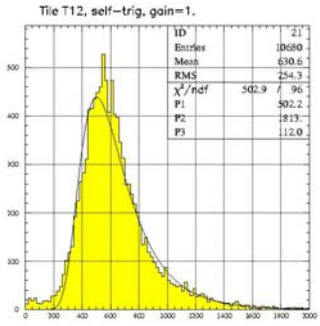
Full functional test – all steps except 43, 44 and 45.

Appendix A - Self-Triggered Mode Information (Steps 16 and 28 of CPT)

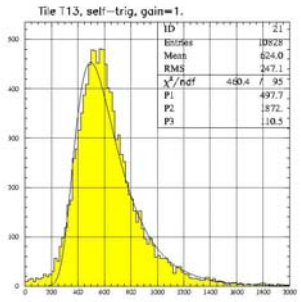
The Self-Triggered Mode of testing flight ACD. One way to do the gain calibration test is to look at all tile histograms in muon run self-triggering mode, meaning that all signals appeared in given tile will be used for the analysis. The advantage of this approach is that for ~ 1 hour of instrument running there will be from 3,000 to 15,000 events in the histogram (depending on the tile) which provides a very reliable and precise peak position determination. The disadvantage of this approach is that the histograms for some tiles, especially for the side tiles, will be very dependent on the muon flux angular distribution. This is because no external triggering will be used, so the angular range of particles causing the triggering will be 2π for every tile, which in the convolution with the incident flux angular dependence could cause the uncertainty if the latter one varies. Simulated histograms for self-triggering mode, are presented in fig. 1 and 2.

Fig. 1 – Top tiles in self-triggering mode

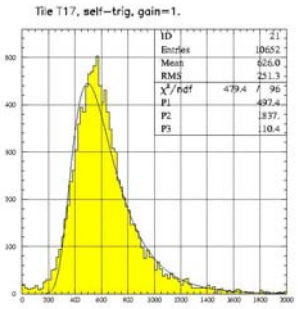




Tile T11 – middle tile in the edge row Tile T12 – next to the central tile

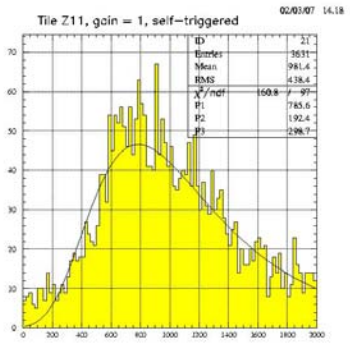


Tile T13 – top center tile

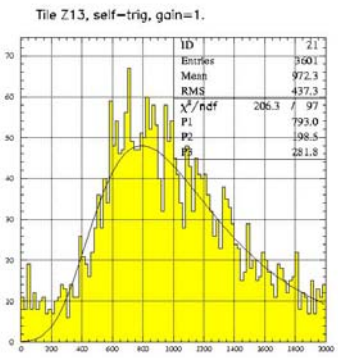


Tile T17 – diagonal from the central tile

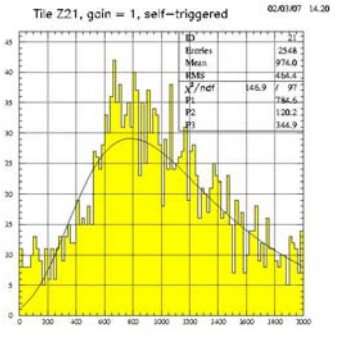
Fig. 2 – Side tiles



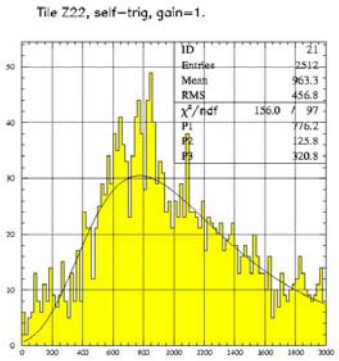
Tile Z11 – end tile in the top row



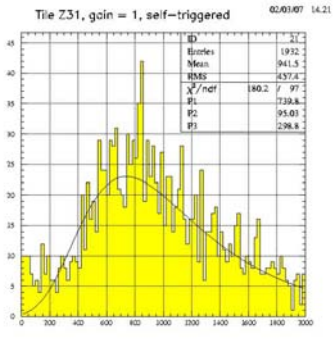
Tile Z13 – middle tile in the top row



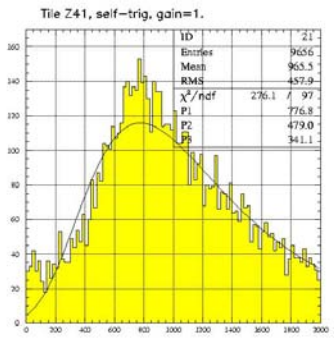
Tile Z21 – end tile in the second row



Tile Z22 – second tile from end in side second row



Tile Z31 – end tile in 3-rd row



Tile Z41 – Long tile bottom row

How sensitive is the self-triggering mode to the gain change? The gain change by 5% was simulated. Similar thing was experimentally tested and proven with muons on BFEM. The simulation run identical to that given above, but with the gain of 0.95 was performed. The MIP peak positions for these runs are given in the Table 3 along with the statistics in each corresponding histogram.

Tile	Statistics for 40 min	Peak position for gain = 1	Peak position for gain = 0.95	Ratio
T11	10,650	498.9	472.7	0.947
T12	10,680	502.2	476.4	0.949
T13	10,828	497.7	471.6	0.947
T17	10,651	497.4	471.6	0.948
Z11	3,631	785.6	748.9	0.953
Z13	3,601	793.0	756.7	0.954
Z21	2,547	784.6	748.8	0.954
Z22	2,512	776.2	729.7	0.940
Z31	1,930	739.8	711.2	0.961
Z32	1,944	765.5	735.8	0.961
Z41	9,658	776.8	738.0	0.950

Obtained results demonstrate that the approach is quite sensitive on the required level of sensitivity (5% of the gain relative change)

Appendix B – Information about Full ACD Gain Calibration Testing (Steps 22, 32, and 43 of CPT)

Test of the Flight ACD . The task is to find for each particular tile what tiles can be used to trigger it. The trajectories should be as normal to the tested tile surface as possible, with reasonable statistics to be collected from the cosmic muons. The tile numbering used in the simulations is shown in Fig. 3. The simulation run corresponded to approximately 40 minutes of

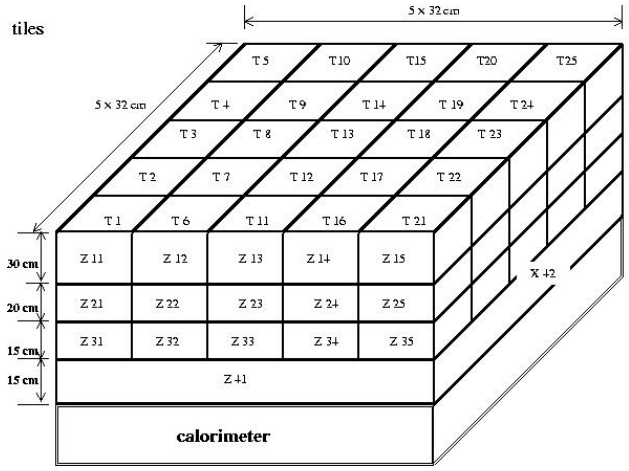
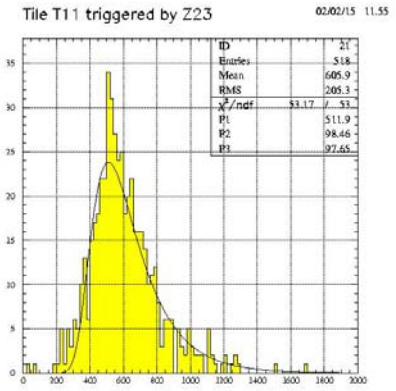


Fig. 3 – Tile numbering used for these simulations. The standard tile numbering convention will be used for actual data and testing.

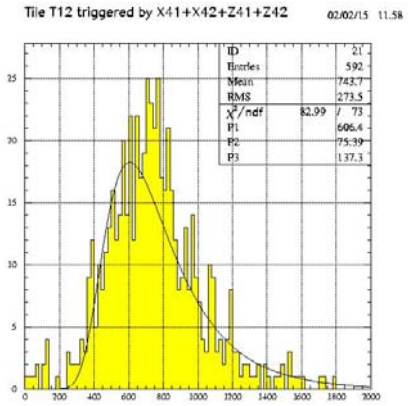
ACD running time, with 10-11 thousand triggers collected for each of top tiles. For each tile, the triggering tiles were carefully selected, and corresponding histograms are shown in figures below. For reliable fitting and MIP peak position determination, approximately 1,500 events are desirable in the histogram. Looking at the histograms, we see that the most difficult tiles to calibrate will be the upper side tiles (fig. 5), which will require 6-7 hours to get ~1,500 events. Limited calibration can be done within ~4 hours Steps 19 and 29).

Full calibration (Step 32) requires higher statistics with most particles normal to the tiles being tested. The approach is to change the orientation of the ACD: (1) top face horizontal; (2) one pair of sides horizontal; (3) opposite pair of sides horizontal.

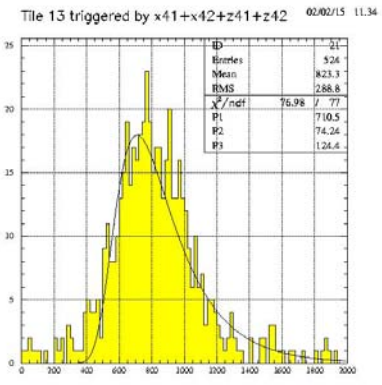
Fig.4 - Top tiles



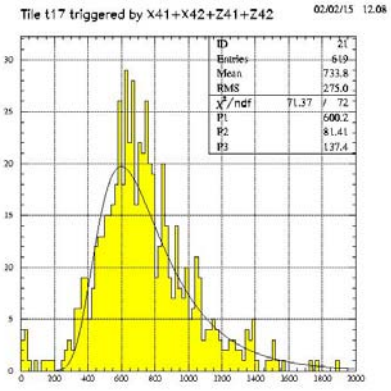
Tile T11 – middle of top edge



Tile T12 – next to the top central tile

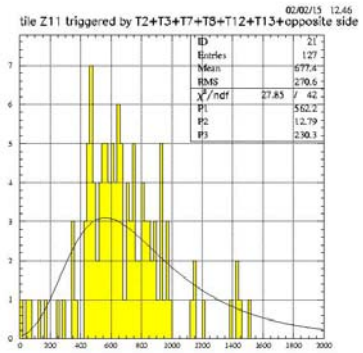


Tile T13 – top center tile

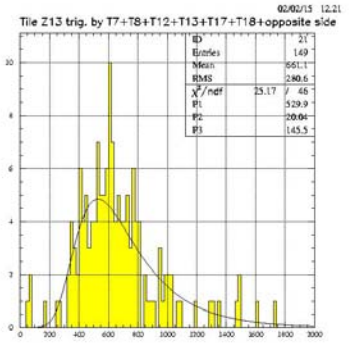


Tile T17 – diagonal from the top central tile

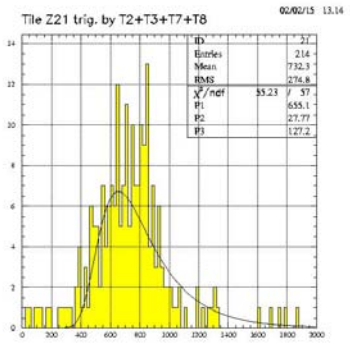
Fig. 5 - Side tiles



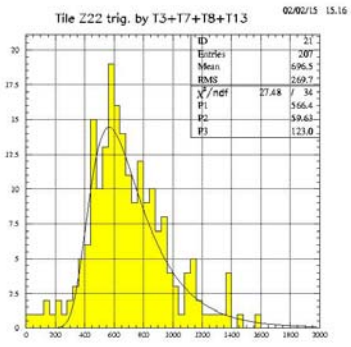
Tile Z11 – end tile in the side top row



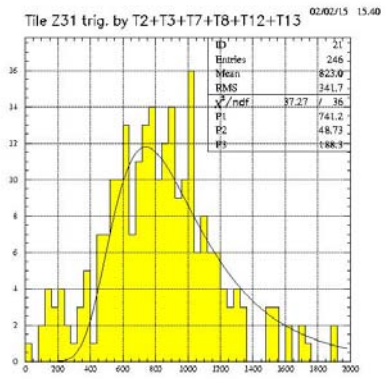
Tile Z13 – middle tile in the side top row



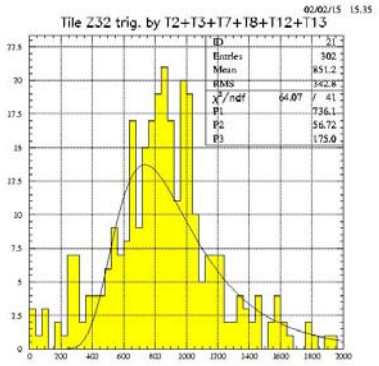
Tile Z21 – end tile in side second row



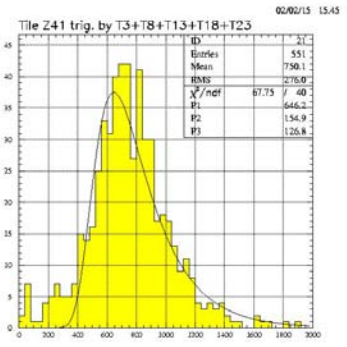
Tile Z22 – second tile from end in side second row



Tile 31 – end tile in side third row



Tile Z32 – second tile from end in side third row



Tile Z41 - Long tile, side bottom row

How many events do we need in the histogram for given peak position uncertainty? The common mathematical approach to this estimate is complicated by the high variability of the particle paths in the tile and desirable lowering the number of events needed. The simulations seem to the appropriate way to do this analysis. I did the following – using sea level muon flux in the simulations, the simulated pulse height distribution was fitted by Landau distribution to find the peak position. This was repeated for 10 sets of approximately 2,500, 1,000, and 500 events in the histogram and the mean value and standard deviation (σ) was determined for each of these sets of 10 runs. This was done for a tile on the top of ACD (where most of the muons hit the tile on or around normal incidence). The results are given in Table 2. The examples of the pulse height distribution for the top tile, 996 events and 511 events in the histogram are given in fig. 8 and fig.9 (column 3 and 4 in the table) respectively. The histogram for the side ("bad") tile and 374 events is shown in fig. 10 (5-th column in the table). It is seen that the precision of the peak position fitting is surprisingly high, even for such a small statistics as ~ 500 events are and for the "bad" tile (the side one) there are a large variation of the incident muon angles, and consequently the muon paths in the tile. We are looking for the change in the light yield on a level of 5% and more. For the efficiency test, we will want higher statistics with more particles moving normal to the tiles.

Table 2 Simulations of the peak position determination precision

Fitted MIP peak position	Top tile, ~2,500 events	Top tile, ~1,000 events	Top tile, ~500 events	Side tile, ~400 events, gain=1	Side tile, ~400 events, gain=0.95
	330.8	329.9	332.2	487.3	467.4
	333.0	326.8	338.2	495.2	467.2
	336.7	336.6	324.5	510.3	462.8
	340.9	338.4	331.5	481.3	489.9
	330.7	335.0	340.9	482.1	478.9
	334.9	330.9	348.4	491.9	539.5 ♣
	331.0	336.0	326.8	509.5	447.1
	336.8	339.1	343.0	510.9	482.1
	331.2	339.5	336.5	511.7	482.5
	336.2	334.8	350.8	521.1	476.4
Mean ±σ	334.2±3.4 (1%)	334.7±4.3 (1.3%)	337.3±8.7 (2.6%)	500.1±13.8 (2.8%)	478.7±24 (5%)

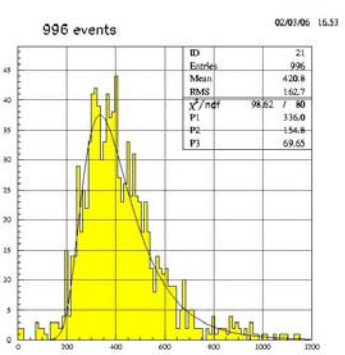


Fig. 8 Top tile, 996 events

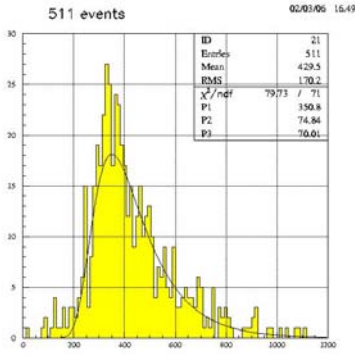


Fig.9 Top tile, 511 events

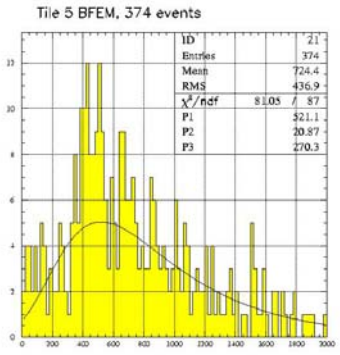


Fig. 10 side tile, 374 events

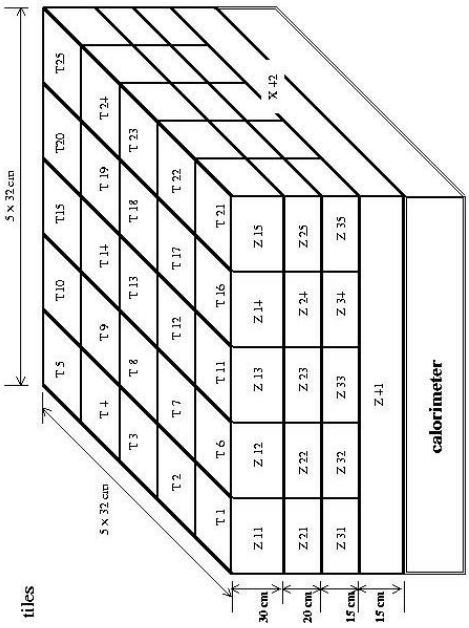
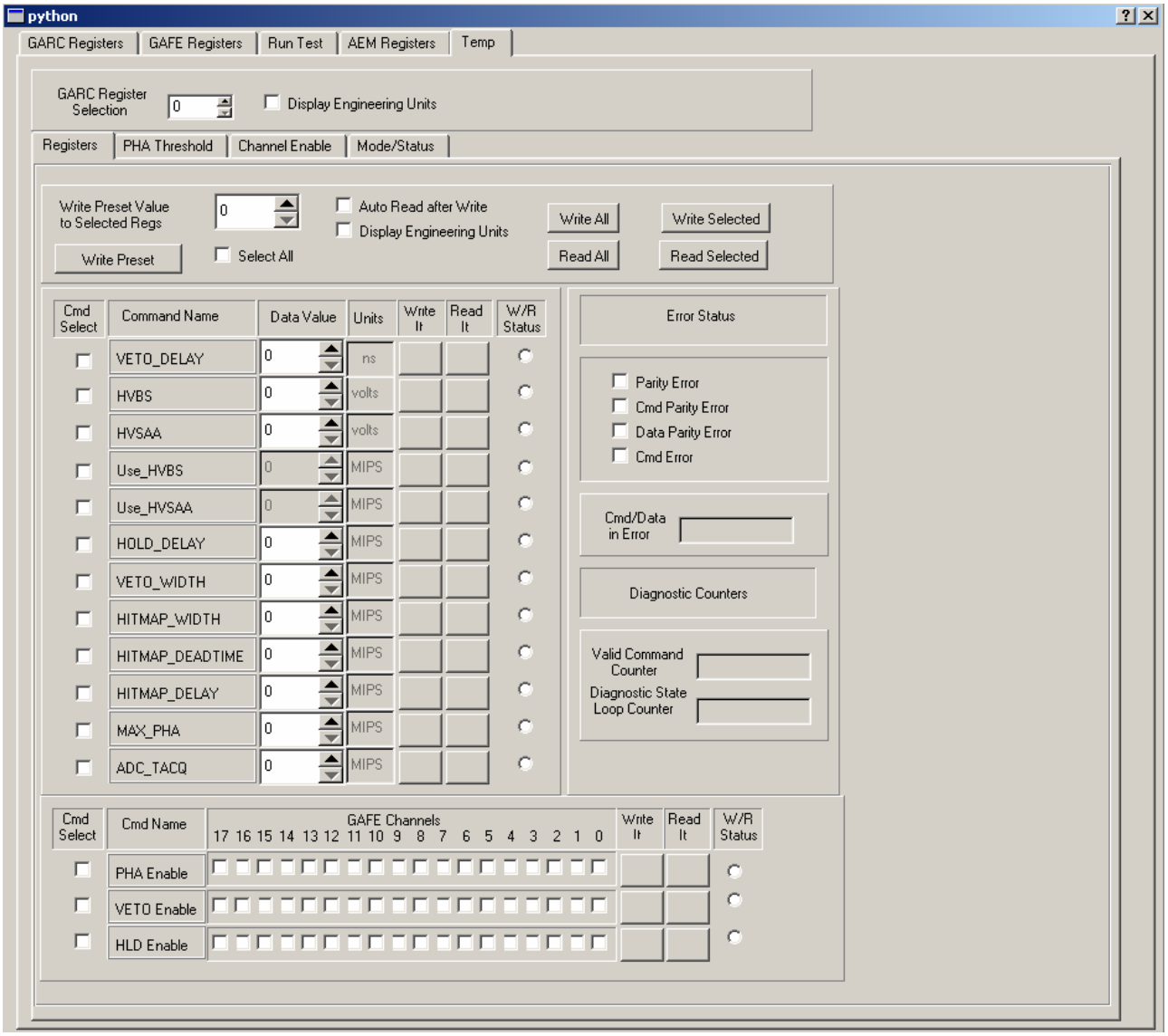


Fig. 11 For the full efficiency test, the ACD will need to be rotated as shown and into a similar configuration with the orthogonal sides horizontal.

Appendix C – Sample Display Page for Command Registers



Appendix D – Calibration Information to be Derived from Functional Testing

Table 1 – Calibration Parameters for Low-Energy Range

Tile/Ribbon	Tube	Rate (Hz)	Pedestal	Elec. Resp.	MIP Pos.	MIP FWHM	Thresh. command	Thresh. (derived)	HV command	HV readout	Effic. (derived)
000	0	350	125	1000	1200	300	440	450	1050	1050	.9998
	1										
001	0										
	1										
					.						
					.						
					.						
602	0	350	125	1000	1200	300	440	450	1050	1050	.9998
	1										
603	0										
	1										

Note: Electronic Response for the low-energy range is defined as the channel in which a 0.64 pC charge appears.

Table 2 – Calibration Parameters for High-Energy Range

Tile/Ribbon	Tube	Rate (Hz)	Pedestal	Elec. Resp.	CNO Pos.	CNO FWHM	Thresh. command	Thresh. (derived)	HV command	HV readout	
000	0	350	125	1000	1200	300	440	450	1050	1050	
	1										
001	0										
	1										

.
.
.

602	0	350	125	1000	1200	300	440	450	1050	1050	
	1										
603	0										
	1										

Note: Electronic Response for the high-energy range is defined as the channel in which a 31 pC charge appears.

Table 3 – Linearity Response for Low-Energy Range

Tile/ Ribbon	Tube	Step 0	Step 1	Step 2	Step 3	• • •	Step 61	Step 62	Step 63
000	0								
	1								
001	0								
				.					
				.					
				.					
603	0								
	1								

Table 4 – Linearity Response for High-Energy Range

Tile/ Ribbon	Tube	Step 0	Step 1	Step 2	Step 3	• • •	Step 61	Step 62	Step 63
000	0								
	1								
001	0								
				.					
				.					
				.					
603	0								
	1								