 GLAST LAT SUBSYSTEM SPECIFICATION	Document # **ACD-RQMT-000031 (was LAT-SS-00352-01)**	Date Effective Draft 12/20/02
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	Subsystem/Office ACD Subsystem	
Document Title **LAT ACD Subsystem Spec - Level IV Requirements/specifications**		

Gamma-ray Large Area Space Telescope

(GLAST)

Large Area Telescope (LAT)

Anticoincidence Detector (ACD)

Subsystem Level 4 Requirements/Specification

Rev –

12/20/02

CHANGE HISTORY LOG

Revision	Effective Date	Description of Changes	DCN #
1		• Initial Release	
2		• Replaced text reqs with only table, • added column of next higher level req, • corrected errors, updated some reqs, • added env and a few other reqs, • updated doc tree figure, • made changes due to trigger deglitch and delay	
3	12/19/02	• Initial CM Release • Using DOORS to create document • Many updates that fall into the following categories o Changes in requirements o Clarification of requirements o Fix typing errors	

ACD Approvals

Dave Thompson ACD Instrument Scientist	Date
Bob Hartman ACD Instrument Scientist	Date
Michael Amato ACD System Manager	Date
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Tom Johnson ACD Instrument Manager	Date
Ken Segal ACD Mechanical Lead	Date
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CONTENTS

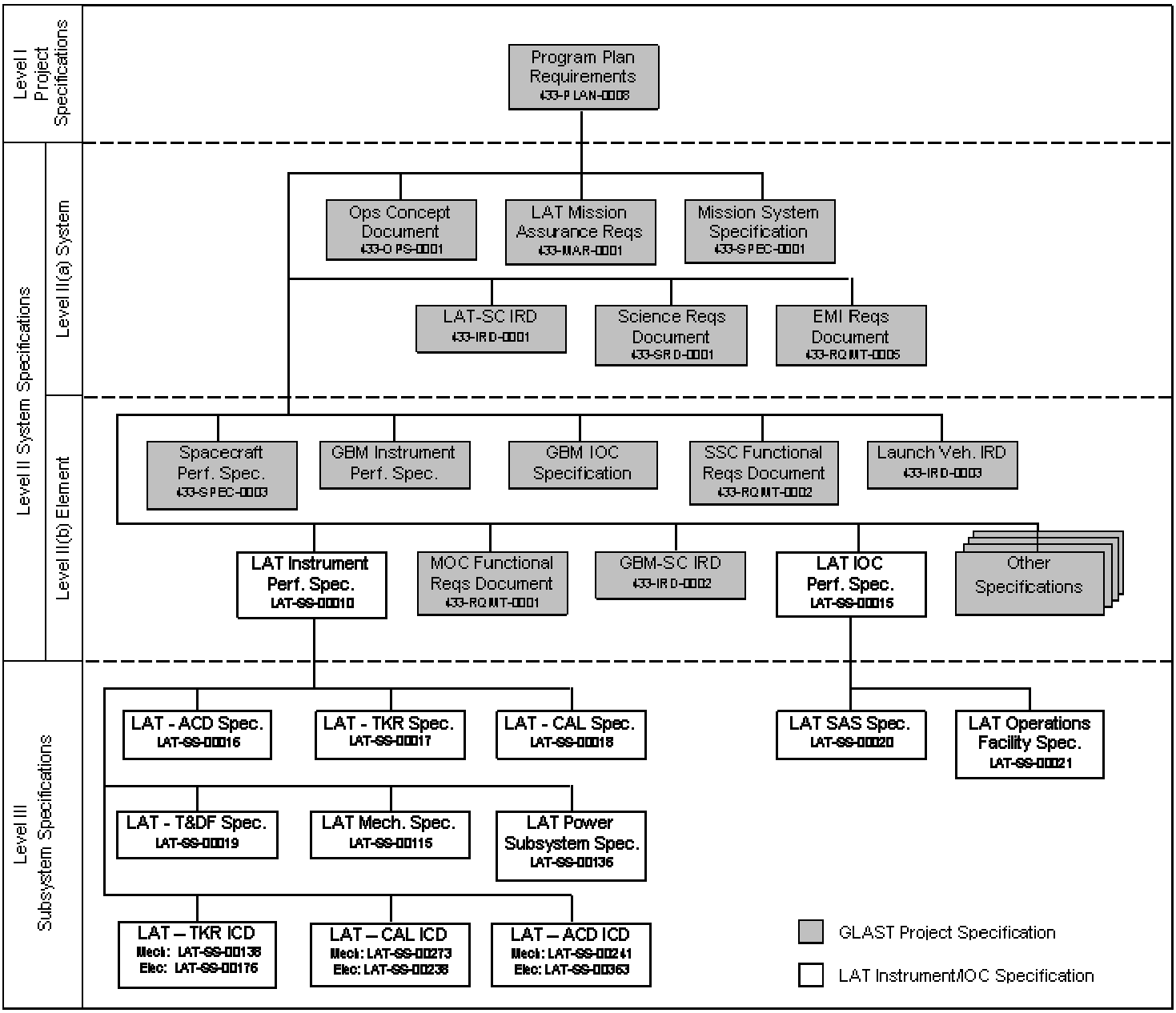
1. PURPOSE

This document defines level IV subsystem requirements for the GLAST Large Area Telescope (LAT) Anticoincidence Detector (ACD).

2. SCOPE

This specification captures the GLAST LAT requirements for the ACD. This encompasses the subsystem level requirements and the design requirements for the ACD.

This specification is identified in the specification tree of Figure 2-1.



3. DEFINITIONS

Acronyms

ACD - Anticoincidence Detector
FOV – Field of View
GLAST – Gamma-ray Large Area Space Telescope
IOC – Instrument Operations Center
IRD – Interface Requirements Document
LAT – Large Area Telescope
MIP – Minimum Ionizing Particle (see definition below)
MSS – Mission System Specification
PI – Principal Investigator
SAS – Science Analysis Software
SI/SC IRD – Science Instrument – Spacecraft Interface Requirements Document
SRD – Science Requirements Document
SSC – Science Support Center
TEM - Tower Electronics Module
TBD - To Be Determined
TBR – To Be Resolved

Definitions

μsec, μs – Microsecond, 10^{-6} second

Analysis – A quantitative evaluation of a complete system and /or subsystems by review/analysis of collected data.

Background Rejection – The ability of the instrument to distinguish gamma rays from charged particles.

Backsplash – Secondary particles and photons originating from very high-energy gamma-ray showers in the calorimeter giving unwanted ACD signals.

cm – centimeter

Cosmic Ray - Ionized atomic particles originating from space and ranging from a single proton up to an iron nucleus and beyond.

Dead Time – Time during which the instrument does not sense and/or record gamma ray events during normal operations.

Demonstration – To prove or show, usually without measurement of instrumentation, that the project/product complies with requirements by observation of results.

eV – Electron Volt

Field of View – Integral of effective area over solid angle divided by peak effective area.

GeV – Giga Electron Volts. 10^9 eV

Inspection – To examine visually or use simple physical measurement techniques to verify conformance to specified requirements.

MeV – Million Electron Volts, 10^6 eV

Minimum Ionizing Particle (MIP) – The mean signal from cosmic ray produced air shower muons at sea level normally incident on a scintillator tile. It corresponds to approximately 1.9 MeV per cm of scintillator.

nsec, ns – Nanosecond, 10^{-9} second

ph – photons

s, sec – seconds

Simulation – To examine through model analysis or modeling techniques to verify conformance to specified requirements

Testing – A measurement to prove or show, usually with precision measurements or instrumentation, that the project/product complies with requirements.

Validation – Process used to assure the requirement set is complete and consistent, and that each requirement is achievable.

Verification – Process used to ensure that the selected solutions meet specified requirements and properly integrate with interfacing products.

VETO - The signal from an individual ACD scintillator tile that indicates an energy deposit of at least ~0.3 MIP (~500 keV) in an ACD scintillator tile, or about 20% of that amount in one of the scintillating fiber ribbons. This threshold is set to be exceeded for a very high fraction of MIPs in the presence of all fluctuations in their energy deposit in the scintillator tiles. The VETO signals from individual tiles and ribbons are combined with information from the tracker and calorimeter to decide whether or not to reject events as background.

4. APPLICABLE DOCUMENTS

Documents that are relevant to the development of the ACD concept and its requirements include the following:

LAT-SS-00016, LAT ACD Subsystem Specification - Level III Requirements, June, 2001

LAT-GE-00009, “LAT Science Requirements Document–Level II Specification”, August 6, 2000.

LAT-SS-00010, "GLAST LAT Performance Specification", August 2000

LAT-SS-00047, "LAT Mechanical Performance Specification"

GSFC 433-MAR-0001, "Mission Assurance Requirements (MAR) for Gamma-Ray Large Area Telescope (GLAST) Large Area Telescope (LAT)", June 9, 2000.

"GLAST Large Area Telescope Flight Investigation: An Astro-Particle Physics Partnership Exploring the High-Energy Universe", proposal to NASA, P. Michelson, PI, November, 1999.

5. REQUIREMENTS

5.1 System Description

The LAT science instrument consists of an Anticoincidence Device (ACD), a silicon-strip detector tracker (TKR), a hodoscopic CsI calorimeter (CAL), and a Trigger and Dataflow system (T&DF). The principal purpose of the LAT is to measure the incidence direction, energy and time of cosmic gamma rays. The measurements are streamed to the spacecraft for data storage and subsequent transmittal to ground-based analysis centers. Signals produced by the ACD are used by the T&DF system to identify cosmic ray electrons and nuclei entering the instrument.

The ACD detects energetic cosmic ray electrons and nuclei for the purpose of removing these backgrounds. It is the principle means for detection of that background. This detector array covers the top and 4 sides of the TKR. It consists of an array of 89 plastic scintillator tiles (25 on the LAT top, 16 on each of the 4 sides, various sizes), plus 8 scintillating fiber "ribbons" that cover the gaps between the tiles. Each scintillator tile is read by 2 PMT's (baseline: Hamamatsu R4443; designated "A" and "B") via waveshifting fibers (and in some cases, clear optical fiber extensions).

The PMT's and the ACD electronics will be located around the base of the ACD, in the Base Electronics Assembly (BEA). The 50 waveshifting fiber bundles and associated clear fiber extensions from the ACD Top will be routed down 2 opposite sides of the ACD (24 and 26), so that those two sides of the BEA will be more heavily populated than the remaining two sides. Each assembly of one tile plus the two associated waveshifting fiber bundles and clear fiber extensions denoted as a Tile Detector Assembly (TDA).

On each of the two opposite LAT sides (±Y) that contain LAT radiators, the BEA will house two ACD electronics boards, one for "A" PMT's and one for "B" PMT's. On each of the remaining two LAT sides (non-radiator), the BEA will house four ACD electronics boards, two associated with "A" PMT's and two associated with "B" PMT's. Each ACD electronics board will be capable of servicing 18 PMT's, although they will vary with regard to numbers of unused electronics channels. All 12 of the ACD electronics boards are nominally identical.

Each ACD electronics board will receive power from redundant high voltage bias supply (HVBS), which is capable of providing the necessary high voltage for all 18 associated PMT's. All 18 PMT's associated with a specific board will receive the same high voltage.

Each ACD electronics board will contain 18 channels of analog, analog-to-digital, and digital processing electronics, as well as command reception and distribution logic and data collection and transmission logic.

Each ACD electronics board interfaces to the LAT via the ACD Electronics Module (AEM). The AEM receives all signals and data from the ACD and sends commands to the ACD. All digital communications between the ACD and the AEM will be via standard LVDS protocol.
Science signals from the TDA's and their associated PMT's are defined in terms of MIP's, the signal generated by a minimum-ionizing singly-charged particle traversing a tile in a direction normal to its surface. To provide a meaningful electronics specification, the definition of a MIP must be normalized to the electrical charge delivered by each of the two PMT's in response to a MIP. The following parameters are assumed for the MIP calculation:

10 photoelectrons per PMT per MIP

PMT gain of 400,000

The result is that **1 MIP** produces a PMT anode signal of **0.64 pC**.

REQUIRMENTS TABLE

Doors ID	LAT ACD Subsystem Level IV Requirements	In-links at depth 1	Link Comment
ACD4-25	5.2 Charged Particle Detection		
ACD4-26	The ACD shall produce both fast and logic (hitmap) VETO signals in response to PMT signals resulting from charged particles traversing the ACD tiles and ribbons.	ACD Level III Requirements LAT-SS-00016 ACD3-16	
ACD4-27	5.3 Adjustable Threshold on VETO Detection of Charged Particles		
ACD4-28	The threshold for detecting charged particles shall be adjustable from 0.064 to 1.28 pC (0.1 to 2 MIP), with a step size of $\leq$0.032 pC (0.05 MIP).	ACD Level III Requirements LAT-SS-00016 ACD3-18	
ACD4-29	5.4 False VETO due to Electrical Noise		
ACD4-30	The total ACD false VETO trigger rate due to noise shall be less than 10 kHz (~46Hz per channel) at 0.096 pC (0.15 MIP) threshold (assuming 1 us VETO pulses).	ACD Level III Requirements LAT-SS-00016 ACD3-28	
ACD4-31	5.5 High-Threshold Detection		

Doors ID	LAT ACD Subsystem Level IV Requirements	In-links at depth 1	Link Comment
ACD4-32	The ACD shall detect pulses due to highly-ionizing particles (carbon-nitrogen-oxygen or heavier nuclei), which produce signals from 31.2 - 200 MIP (20 pC to 128 pC) with a goal of 1000 MIP (640 pC). The ACD is required to detect, via the High-Level Discriminator (HLD), all signals above the High-Level threshold (nominally 25 MIP's); it is required to digitize (PHA) signals up to 200 MIP's (128 pC). The current design actually allows for digitization of signals up to 1000 MIP's (640 pC). Each ACD electronics board shall OR up to 18 HLD outputs (selected via command) to generate a single HLD_OR signal for transmission to the AEM.	ACD Level III Requirements LAT-SS-00016 ACD3-30	
ACD4-34	5.6 Adjustable High-Threshold		
ACD4-35	The High-Level Threshold shall be adjustable for PMT signals from 12.8 to 40.96 pC (20 to 64 MIP) in steps of 0.64 pC (1 MIP) ±20%.	ACD Level III Requirements LAT-SS-00016 ACD3-32	
ACD4-36	5.7 Level 1 Trigger Acknowledge (TACK)		
ACD4-37	The ACD electronics shall accept from the AEM a Level 1 Trigger Acknowledge signal and respond by digitizing and latching data.	ACD ICD LAT-SS-00363 ACDICD-46	
ACD4-38	5.8 Signals		
ACD4-39	5.8.1 Fast VETO (VETO_AEM) Signal Latency		

Doors ID	LAT ACD Subsystem Level IV Requirements	In-links at depth 1	Link Comment
ACD4-40	The fast VETO signal latency shall be 100<tlatent<600 nsec from the time of particle passage. The time jitter in the VETO pulses shall be <200 ns relative to particle passage. ('Deglitch' circuit raised min latency to 100 nsec from 50 nsec).	ACD Level III Requirements LAT-SS-00016 ACD3-34 ACD Level III Requirements LAT-SS-00016 ACD3-36	
ACD4-41	5.8.2 Fast VETO (VETO_AEM) Signal Width		
ACD4-42	The fast VETO output signal shall have a commandable width of 50 – 400 nsec, after 'de-glitching' on 2 successive clock pulses. The leading and trailing edges must be synchronous with clock pulses.	ACD Level III Requirements LAT-SS-00016 ACD3-430 ACD Level III Requirements LAT-SS-00016 ACD3-44 ACD Level III Requirements LAT-SS-00016 ACD3-46	
ACD4-43	5.8.3 Fast VETO (VETO_AEM) Retriggering		
ACD4-44	The Fast VETO discriminator shall be capable of retriggering less than 50 ns after the trailing edge of the VETO output signal.	ACD Level III Requirements LAT-SS-00016 ACD3-20	
ACD4-45	5.8.4 Logic VETO (VETO_Hitmap) Signal		

Doors ID	LAT ACD Subsystem Level IV Requirements	In-links at depth 1	Link Comment
ACD4-46	A map of VETO signals shall be generated for each TACK, indicating which ACD PMT's produced signals above their thresholds within ~200 ns of the time of the event causing the TACK. (Note: The ~200 ns window is required because of time jitter in the TACK signal).	ACD Level III Requirements LAT-SS-00016 ACD3-430 ACD Level III Requirements LAT-SS-00016 ACD3-38 ACD Level III Requirements LAT-SS-00016 ACD3-42	
ACD4-47	5.8.5 Logic VETO (VETO_Hitmap) Signal Latency		
ACD4-48	In response to a TACK, the map of VETO signals shall be latched by the time the ADC conversions are complete.	ACD Level III Requirements LAT-SS-00016 ACD3-40	
ACD4-49	5.8.6 High-Threshold Signal Latency		
ACD4-50	A highly-ionizing particle hitting the top or upper side row of tiles of the ACD shall produce a High-Threshold fast signal that will be delivered to the AEM with latency of no more than that the latency as defined for the fast VETO in specification 5.8.1. Command-selected signals out of the eighteen (18) High-Threshold fast signals generated on a single electronics board shall be OR'ed to produce a single signal for transmission to the AEM.	ACD Level III Requirements LAT-SS-00016 ACD3-48 ACD Level IV Requirements and Verification LAT-SS-00352 ACD4-40	

Doors ID	LAT ACD Subsystem Level IV Requirements	In-links at depth 1	Link Comment
ACD4-51	5.8.7 Discriminator Masking		
ACD4-52	Each ACD electronics board shall have the capability to disable any combination of the Fast VETO and HLD discriminator outputs. This is to mask unused HLD signals, unpopulated veto channels, and signals due to channel failure.	ACD Level IV Requirements and Verification LAT-SS-00352 ACD4-52 ACD Level III Requirements LAT-SS-00016 ACD3-30	
ACD4-53	5.8.8 ACD Trigger Primitives		
ACD4-54	This requirement deleted for ACD. The ACD will produce no trigger primitives internally. The VETO signals caused by the individual PMT's will be transmitted to the AEM, where they will be OR'ed together (for each tile or ribbon), and used by the AEM to generate trigger primitives.	ACD Level III Requirements LAT-SS-00016 ACD3-50	
ACD4-55	5.9 ACD Performance Monitoring		
ACD4-56	The AEM will scale and telemeter count rates for ACD VETO and HLD signals, as well as various trigger primitives. ACD voltages and currents will be monitored by the AEM.	ACD Level III Requirements LAT-SS-00016 ACD3-52	
ACD4-57	5.9.1 Low-Threshold Signal		
ACD4-58	Requirement deleted.		
ACD4-59	5.9.2 Low-Threshold Adjustability		
ACD4-60	Requirement deleted.		

Doors ID	LAT ACD Subsystem Level IV Requirements	In-links at depth 1	Link Comment
ACD4-61	5.9.3 Pulse Digitization (was Signal Content)		
ACD4-62	When a TACK signal is received, the ACD electronics shall digitize all PMT signal amplitudes with the following precision: --for a pulse below 6.4 pC (10 MIP), precision of <0.0128 pC (0.02 MIP) or 5%, whichever is larger; --for a pulse above 6.4 pC (10 MIP), precision of ≤0.64 pC (1 MIP) or 2%, whichever is larger. The largest signal amplitude to be digitized is at least 128 pC (200 MIP) goal of 640 pC (1000 MIP). The ACD shall transmit to the AEM only digitized signals above the command-adjustable threshold for the specific channel (zero-suppress threshold).	ACD Level III Requirements LAT-SS-00016 ACD3-58 ACD Level III Requirements LAT-SS-00016 ACD3-62	
ACD4-66	5.9.4 Pulse Height Measurement Latency		
ACD4-67	The PMT pulse amplitudes shall be digitized within 18.5 microseconds after a Level 1 trigger is received. (NOTE : Transmission to AEM not included in 18.5 microseconds, for example for the maximum data case, we put out 18 PHA words. This ends up taking ~ 29.5 or 30 usec of time for the PHA)	ACD Level III Requirements LAT-SS-00016 ACD3-64	
ACD4-68	5.9.5 Integral Non-Linearity		

Doors ID	LAT ACD Subsystem Level IV Requirements	In-links at depth 1	Link Comment
ACD4-69	The integral non-linearity should be $\leq$ 2% over the top 95% of the signal input range for the low-energe range (below 6.4 pC) for ease of analysis.	ACD Level III Requirements LAT-SS-00016 ACD3-52 ACD Level III Requirements LAT-SS-00016 ACD3-58	
ACD4-70	5.9.6 Differential Non-Linearity		
ACD4-71	Based on 1024 channels, the differential non-linearity shall be less than ±10% of the average channel width.	ACD Level III Requirements LAT-SS-00016 ACD3-52 ACD Level III Requirements LAT-SS-00016 ACD3-58	
ACD4-72	5.9.7 Temperature Stability		

Doors ID	LAT ACD Subsystem Level IV Requirements	In-links at depth 1	Link Comment
ACD4-73	The analog signal processing chain shall exhibit temperature stability of gain better than 500 ppm per degree C over the operating temperature range. For both the low range (0 to 6.4 pC ±20%, = 10 MIPs) and the high range (6.4 ±20% to 640 pC, 10 to 200 MIPs, the requirement is 200 MIPs but design goal is 1000 MIPs), the analog signal processing chain shall exhibit temperature stability of its baseline better than 0.05% of full scale per degree C.	ACD Level III Requirements LAT-SS-00016 ACD3-18 ACD Level III Requirements LAT-SS-00016 ACD3-20 ACD Level III Requirements LAT-SS-00016 ACD3-52 ACD Level III Requirements LAT-SS-00016 ACD3-58 ACD Level IV Requirements and Verification LAT-SS-00352 ACD4-73	
ACD4-74	5.9.8 Test Pulse Injection		
ACD4-75	For test purposes, the ACD electronics shall incorporate the capability to be artificially stimulated by a test charge, via commands. The test charge injection range shall be 0 - 200 MIP with a goal of 0 - 1000 MIP.	ACD Level III Requirements LAT-SS-00016 ACD3-52	
ACD4-76	5.9.9 Digital Housekeeping		

Doors ID	LAT ACD Subsystem Level IV Requirements	In-links at depth 1	Link Comment
ACD4-77	The state of all ACD command registers shall be available for readout via AEM commands. The AEM will scale all ACD VETO and HLD rates and transmit the results in low rate telemetry.	ACD Level III Requirements LAT-SS-00016 ACD3-66	
ACD4-78	5.9.10 Temperature Monitoring		
ACD4-79	ACD shall provide temperature transducer signals for survival, safe, and operational modes. Signals are specifically defined in ACD ICD. ACD does not provide the actual temperature monitoring.	ACD Level IV Requirements and Verification LAT-SS-00352 ACD4-73 ACD Level III Requirements LAT-SS-00016 ACD3-66	
ACD4-80	5.10 High Voltage Bias Supply		
ACD4-81	5.10.1 HVBS Output Voltage Range		
ACD4-82	The HVBS shall operate from +400 V to +1250 V.	ACD Level III Requirements LAT-SS-00016 ACD3-97 ACD Level III Requirements LAT-SS-00016 ACD3-110	
ACD4-83	5.10.2 HVBS Output Current		

Doors ID	LAT ACD Subsystem Level IV Requirements	In-links at depth 1	Link Comment
ACD4-84	The HVBS shall provide sufficient current to drive all PMTs (max 18) on each FREE circuit card at the maximum voltage (+1250V).	ACD Level III Requirements LAT-SS-00016 ACD3-16	Also driven by the PMT Operational Requirements.
ACD4-85	5.10.3 HVBS Limiting Output Current		
ACD4-86	The HVBS output current shall be limited to protect the ACD from one PMT short. At maximum output voltage, each HVBS shall be capable of supplying a total output current of 60 μA. The nominal output current will be 36 μA.	ACD Level III Requirements LAT-SS-00016 ACD3-68 ACD Level III Requirements LAT-SS-00016 ACD3-91	
ACD4-87	5.10.4 HVBS Output Voltage Adjustment		
ACD4-88	The HVBS output voltage shall be programmable with an analog input. The limiting output current of each HVBS shall be ~80 μA.	ACD Level III Requirements LAT-SS-00016 ACD3-18 ACD Level III Requirements LAT-SS-00016 ACD3-32 ACD Level III Requirements LAT-SS-00016 ACD3-52	
ACD4-89	5.10.5 HVBS Input Power		

Doors ID	LAT ACD Subsystem Level IV Requirements	In-links at depth 1	Link Comment
ACD4-90	Each HVBS shall operate from a supply voltage of 28V ± 1V, with possible input ripple of 10 mV (frequency range 50 Hz to 50 MHz). The noise shall be less than 100 mV RMS from DC to 1.0 MHz.	ACD ICD LAT-SS-00363 ACDICD-45	
ACD4-91	5.10.6 HVBS Line and Load Regulation		
ACD4-92	The HVBS output voltage shall be regulated to ±0.5% for all combinations of input voltage and load current. (This produces ~5% change in PMT gain).	ACD Level III Requirements LAT-SS-00016 ACD3-18 ACD Level III Requirements LAT-SS-00016 ACD3-20	
ACD4-93	5.10.7 HVBS Output Ripple		
ACD4-94	The HVBS output voltage ripple shall be compatible with the ACD ASIC design. The HVBS output voltage ripple shall not exceed ±2 mV p-p over the frequency range 100 Hz to 50 MHz	ACD Level III Requirements LAT-SS-00016 ACD3-16	Also driven by a design compatibility between the PMTs and Analog ASIC.
ACD4-95	5.10.8 HVBS Power Consumption		
ACD4-96	The HVBS power dissipation at maximum output voltage and limiting current shall be <300 mW.	ACD Level III Requirements LAT-SS-00016 ACD3-91	
ACD4-97	5.10.9 HVBS Ramp Up/Down Time		

Doors ID	LAT ACD Subsystem Level IV Requirements	In-links at depth 1	Link Comment
ACD4-98	For either application or removal of input power, the time for the HVBS output voltage to reach its final level (for turn-on, within regulation tolerance) shall be between 5 and 30 seconds. Note: The 5 second requirement is driven by the PMT, the 30 seconds is driven by the maximum tolerable time for HVBS to stabilize when entering/exiting the SAA.	ACD Level III Requirements LAT-SS-00016 ACD3-97 ACD Level III Requirements LAT-SS-00016 ACD3-68	Also driven by the PMT Operational Requirements.
ACD4-99	5.10.10 HVBS Temperature Stability		
ACD4-100	The HVBS output voltage temperature stability shall be no worse than 500 ppm/C.	ACD Level III Requirements LAT-SS-00016 ACD3-20	
ACD4-101	5.10.11 HVBS Output Voltage Monitoring		
ACD4-102	The HVBS shall provide a linear output voltage monitor (for transmission to the AEM) in the range 0.0 to 2.5 V.	ACD ICD LAT-SS-00363 ACDICD-41 ACD Level III Requirements LAT-SS-00016 ACD3-66	
ACD4-103	5.10.12 HVBS Ground Isolation		
ACD4-104	The DC impedance between input and output grounds shall be 100 ohms ±20%.	ACD ICD LAT-SS-00363 ACDICD-61	
ACD4-105	5.10.13 HVBS Oscillator Frequency		

Doors ID	LAT ACD Subsystem Level IV Requirements	In-links at depth 1	Link Comment
ACD4-106	The HVBS shall utilize an oscillator frequency ≥100 kHz (to minimize EMI issues).	ACD Level III Requirements LAT-SS-00016 ACD3-97	
ACD4-107	5.10.14 HVBS EMI and Susceptibility		
ACD4-108	The HVBS shall neither generate nor be susceptible to electromagnetic interference exceeding the EMI/EMC test requirement, GSFC-433-RQMT-0005.	ACD Level III Requirements LAT-SS-00016 ACD3-97	
ACD4-109	5.11 PMT		
ACD4-110	5.11.1 PMT Bias Chain Total Resistance		
ACD4-111	The total resistance of a PMT bias chain shall be such as to result in a nominal current (at the maximum HVBS voltage) of 2 microamps (~100 times the PMT average anode current.)	ACD Level III Requirements LAT-SS-00016 ACD3-20 ACD Level III Requirements LAT-SS-00016 ACD3-16	Also driven by the PMT Operational Requirements.
ACD4-112	5.11.2 PMT Bias Chain Filter Resistance		

Doors ID	LAT ACD Subsystem Level IV Requirements	In-links at depth 1	Link Comment
ACD4-113	At least four percent of the total resistance of the bias chain shall be in a filter resistor(s) at the high voltage input. This PMT bias chain filter resistance protects against a PMT short with a current limiting resistor and filters out HVBS ripple.	ACD Level III Requirements LAT-SS-00016 ACD3-68 ACD Level III Requirements LAT-SS-00016 ACD3-28	
ACD4-114	5.11.3 PMT Bias Chain Resistor Distribution		
ACD4-115	The number and values of the remaining resistors in the bias chain shall be selected to be compatible with the selected PMT, Hamamatsu R4443.	ACD Level III Requirements LAT-SS-00016 ACD3-16	Also driven by the PMT Operational Requirements.
ACD4-116	5.11.4 PMT Anode Signal Coupling		
ACD4-117	The PMT anode signal shall be coupled into the associated analog electronics via two capacitors of 680 pF in series. A charge leakage bleed-off resistor of at least 1-mega ohms shall be incorporated on the low-voltage side of the capacitor pair.	ACD Level III Requirements LAT-SS-00016 ACD3-16	Also driven by a design compatibility between the PMTs and Analog ASIC and good design practice.
ACD4-118	5.11.5 PMT Bias Chain Load Resistor		
ACD4-119	A load resistor of $\geq$ 10 KΩ shall be incorporated into the bias network.	ACD Level III Requirements LAT-SS-00016 ACD3-16	Also driven by the PMT Operational Requirements.
ACD4-120	5.11.6 PMT Bias Chain Dynode Decoupling		

Doors ID	LAT ACD Subsystem Level IV Requirements	In-links at depth 1	Link Comment
ACD4-121	The resistors biasing the last three-dynode stages shall be bypassed by capacitors to prevent a drop in gain for very large pulses or the maximum expected high rate of pulses (<1% gain change for 3kHz rate).	ACD Level III Requirements LAT-SS-00016 ACD3-16	
ACD4-122	5.12 Radiation Tolerance		
ACD4-123	The ACD electronics shall remain within specifications after a total ionizing radiation dose of 4.5 kRad(Si).	ACD Level III Requirements LAT-SS-00016 ACD3-97	Also driven by the GLAST Mission Spec (433-SPEC-0001)
ACD4-124	5.12.1 Single Event Upset Tolerance		
ACD4-125	A single event upset (SEU) shall not cause the ACD electronics to transition to an unsafe state.	ACD Level III Requirements LAT-SS-00016 ACD3-108 ACD Level III Requirements LAT-SS-00016 ACD3-68	Also driven by the GLAST Mission Spec (433-SPEC-0001)
ACD4-126	5.12.2 Latchup Tolerance		

Doors ID	LAT ACD Subsystem Level IV Requirements	In-links at depth 1	Link Comment
ACD4-127	Parts that show any SEE's at an LET lower than 37 MeV*cm^2/mg shall not degrade the mission performance.	ACD Level III Requirements LAT-SS-00016 ACD3-108 ACD Level III Requirements LAT-SS-00016 ACD3-68 ACD Level III Requirements LAT-SS-00016 ACD3-97	Also driven by the GLAST Mission Spec (433-SPEC-0001)
ACD4-128	5.13 Reliability		
ACD4-863	The ACD reliability allotment from LAT is currently .96 over 5 years.	ACD Level III Requirements LAT-SS-00016 ACD3-68	
ACD4-129	5.13.1 ACD Electronics Reliability		
ACD4-130	No single failure in the ACD electronics shall result in complete loss of signal from more than one ACD detector (tile or ribbon). The overall calculated reliability of the ACD electronics assembly shall be at least 0.98 in one year.	ACD Level III Requirements LAT-SS-00016 ACD3-68	
ACD4-131	5.13.2 ACD Tile Detector Assembly and Scintillator Ribbon Reliability		

Doors ID	LAT ACD Subsystem Level IV Requirements	In-links at depth 1	Link Comment
ACD4-132	The probability of the loss of both VETO signals from a specific scintillator tile shall be less than 1% in 5 years). The probability of the loss of VETO signals from a scintillator ribbon shall be less than 5% in 5 years. The overall calculated reliability of ACD scintillating tiles and scintillator ribbons shall be at least 0.99 in one year.	ACD Level III Requirements LAT-SS-00016 ACD3-70 ACD Level III Requirements LAT-SS-00016 ACD3-68 ACD Level III Requirements LAT-SS-00016 ACD3-74	
ACD4-133	5.13.3 Requirement moved to 5.12.2.		
ACD4-134	5.13.4 Requirement moved to 5.12.1.		
ACD4-135	5.13.5 ACD Micrometeoroid Shield/Thermal Blanket Reliability		
ACD4-136	The overall calculated reliability of an ACD micrometeoroid shield/thermal blanket shall be at least 0.99 in one year.	ACD Level III Requirements LAT-SS-00016 ACD3-68	
ACD4-137	5.13.6 Requirement combined with 5.13.2		
ACD4-138	5.14 Commands		
ACD4-139	5.14.1 Detector On/Off Commands		

Doors ID	LAT ACD Subsystem Level IV Requirements	In-links at depth 1	Link Comment
ACD4-140	The AEM will implement commands to allow each group of 18 PMT's to be powered on and off together.	ACD ICD LAT-SS-00363 ACDICD-54 ACD Level III Requirements LAT-SS-00016 ACD3-77	
ACD4-141	5.14.2 Detector Gain Commands		
ACD4-142	The ACD shall implement adjustability of the high voltage applied to the group of 18 PMT's associated with a single board.	ACD Level III Requirements LAT-SS-00016 ACD3-79 ACD Level III Requirements LAT-SS-00016 ACD3-32 ACD Level III Requirements LAT-SS-00016 ACD3-18	
ACD4-143	5.14.3 Electronics On/Off Commands		

Doors ID	LAT ACD Subsystem Level IV Requirements	In-links at depth 1	Link Comment
ACD4-144	The AEM will implement commands to allow each ACD electronics board to be separately powered on and off.	ACD ICD LAT-SS-00363 ACDICD-45 ACD Level III Requirements LAT-SS-00016 ACD3-68 ACD Level III Requirements LAT-SS-00016 ACD3-81	
ACD4-145	5.14.4 VETO Threshold Commands		
ACD4-146	The ACD shall implement adjustability of the VETO threshold for each PMT.	ACD Level III Requirements LAT-SS-00016 ACD3-83 ACD Level III Requirements LAT-SS-00016 ACD3-32 ACD Level III Requirements LAT-SS-00016 ACD3-18 ACD Level IV Requirements and Verification LAT-SS-00352 ACD4-28	

Doors ID	LAT ACD Subsystem Level IV Requirements	In-links at depth 1	Link Comment
ACD4-147	5.14.5 High-Threshold Commands		
ACD4-148	The ACD shall implement adjustability of the High-Level Discriminator Threshold for each PMT.	ACD Level III Requirements LAT-SS-00016 ACD3-18 ACD Level III Requirements LAT-SS-00016 ACD3-32 ACD Level III Requirements LAT-SS-00016 ACD3-85 ACD Level IV Requirements and Verification LAT-SS-00352 ACD4-35	
ACD4-149	5.14.6 ACD Monitoring Commands		
ACD4-150	The ACD shall implement adjustability of the monitoring functions of the ACD electronics, including the zero suppression for each PMT.	ACD Level III Requirements LAT-SS-00016 ACD3-87 ACD Level III Requirements LAT-SS-00016 ACD3-52	
ACD4-151	5.14.7 TACK Format		

Doors ID	LAT ACD Subsystem Level IV Requirements	In-links at depth 1	Link Comment
ACD4-152	TACK format shall be in compliance with ICD definition of TACK.	ACD ICD LAT-SS-00363 ACDICD-47 ACD Level III Requirements LAT-SS-00016 ACD3-58	
ACD4-153	5.14.8 Command Format		
ACD4-154	Command formats shall be in compliance with ICD format definitions.	ACD ICD LAT-SS-00363 ACDICD-46	
ACD4-155	5.14.9 SAA Mode commands		
ACD4-156	The ACD photomultiplier HVBSs shall switch into a low-gain mode to protect the phototubes in very high intensity particle conditions (> 10 kHz in an individual tile) such as the South Atlantic Anomaly. (Accomplished by HVBS command from AEM to GARC)	ACD Level III Requirements LAT-SS-00016 ACD3-89 ACD Level III Requirements LAT-SS-00016 ACD3-110	
ACD4-157	5.14.10 Notification of Mode Change		
ACD4-158	The ACD shall identify times when it switches into low-gain mode for high counting rate conditions.	ACD Level III Requirements LAT-SS-00016 ACD3-112	
ACD4-159	5.15 Output Data Formats		
ACD4-160	ACD Output data formats shall be in compliance with ICD format definitions.	ACD ICD LAT-SS-00363 ACDICD-58	

Doors ID	LAT ACD Subsystem Level IV Requirements	In-links at depth 1	Link Comment
ACD4-161	5.16 Power Consumption		
ACD4-162	The ACD total electronics power consumption shall not exceed 31 W conditioned.	ACD Level III Requirements LAT-SS-00016 ACD3-91	
ACD4-163	5.17 Total ACD Mass		
ACD4-164	The total mass of the ACD shall not exceed 280 kg (allocation of 270 kg with 10 kg reserve). (The mass was increased from 235 Kg pending signature approval of CR# XR1200-01)	ACD Level III Requirements LAT-SS-00016 ACD3-93	
ACD4-165	5.18 Environmental Requirements		
ACD4-166	The ACD shall meet all structural, thermal, EM and radiation environment requirements.	ACD Level III Requirements LAT-SS-00016 ACD3-97 ACD Level III Requirements LAT-SS-00016 ACD3-104	
ACD4-167	5.18.1 Ground – Handling and transportation Vibration and Shock		
ACD4-168	Deleted in LAT level IIb 12/10/01, see ACD Transportation and Procedure (ACD-TBD-XX)	ACD Level III Requirements LAT-SS-00016 ACD3-97	
ACD4-169	5.18.2 Orbit - Flight temperature ranges		

Doors ID	LAT ACD Subsystem Level IV Requirements	In-links at depth 1	Link Comment
ACD4-856	ACD shall be able to handle orbit survival and operational temperature ranges specified in the ACD ICD (LAT-SS-363)	ACD ICD LAT-SS-00363 ACDICD-65 ACD Level III Requirements LAT-SS-00016 ACD3-97	
ACD4-185	5.18.3 Launch - Static Load		
ACD4-186	ACD shall be capable of normal operation after exposure to launch loads as given in SI/SC IRD (sec 3)	ACD Level III Requirements LAT-SS-00016 ACD3-97	
ACD4-187	5.18.4 Launch - Random Vibrations		
ACD4-188	ACD shall be capable of normal operation after exposure to ASD levels referred to in the SC IRD which are given in GEVS Table D-6	ACD Level III Requirements LAT-SS-00016 ACD3-97	
ACD4-189	5.18.5 Launch - Acoustic Loads		
ACD4-190	Capable of normal operation after exposure to acoustic loads given in SI/SC IRD which refers to spec 433-SPEC-0003, the acoustic equivalant design loads are derived in ACD SPEC-3006 (this used to refer to GEVS Table D-3 T but has been changed). (Note : information on acoustic abatement at the GLAST launch pad and preliminary acoustic loads analyses for ACD have reduced acoustic loads)	ACD Level III Requirements LAT-SS-00016 ACD3-97	
ACD4-191	5.18.6 Launch – Shock		

Doors ID	LAT ACD Subsystem Level IV Requirements	In-links at depth 1	Link Comment
ACD4-192	Capable of normal operation after exposure to external shock levels given in GEVS Table D-8 or D-9, as applicable, attenuated to SI/SC interface values.	ACD Level III Requirements LAT-SS-00016 ACD3-95	
ACD4-193	5.18.7 Launch – temperature		
ACD4-194	Tolerate 0 to 30 °C in launch configuration (Note - Considering asking for lower temp (~0 to 15C) to help Tile Gap issue)	ACD Level III Requirements LAT-SS-00016 ACD3-97	
ACD4-195	5.18.8 Launch – Pressure		
ACD4-196	Flux Environment		
ACD4-197	Tolerate Earth IR loads of 265 W/m^2 (hot case), and 208 W/m^2 (cold case), plus Earth Albedo factor of 0.40 (hot case), and 0.25 (cold case) . See LAT Thermal Design Parameters Study LAT-TD-00224.	ACD ICD LAT-SS-00363 ACDICD-65	Also driven by Thermal Design Parameters Study LAT-TD-00224.
ACD4-198	Environment		
ACD4-199	Solar Flux - 1419 W/m^2 (hot case), and 1286 W/m^2 (cold case), sustained exposure on +X side. See LAT Thermal Design Parameters Study LAT-TD-00224.	ACD ICD LAT-SS-00363 ACDICD-65	Also driven by Thermal Design Parameters Study LAT-TD-00224.
ACD4-200	5.18.9 On-orbit – Thermal		

Doors ID	LAT ACD Subsystem Level IV Requirements	In-links at depth 1	Link Comment
ACD4-857	Handle orbit interface, survival and operational thermal values specifed in ICD.	ACD Level III Requirements LAT-SS-00016 ACD3-106 ACD Level III Requirements LAT-SS-00016 ACD3-97 ACD ICD LAT-SS-00363 ACDICD-65	
ACD4-202	5.18.10 On-Orbit Charged Particle Radiation		
ACD4-203	Deleted from LAT IIb		
ACD4-204	5.18.11 On-Orbit - Meteoroid and Debris Flux		
ACD4-205	Instrument must withstand meteoroid and debris flux estimates given in GLAST MSS Section 'Micrometeoroid and Debirs Flux' for impact probabilities of 0.001 and above	ACD Level III Requirements LAT-SS-00016 ACD3-104	
ACD4-206	5.19 Performance Life		
ACD4-207	The ACD shall maintain the specified performance for a minimum of five years in orbit.	ACD Level III Requirements LAT-SS-00016 ACD3-108	
ACD4-208	5.20 Rate Requirement for Operation within Specification		

Doors ID	LAT ACD Subsystem Level IV Requirements	In-links at depth 1	Link Comment
ACD4-209	Each ACD PMT and its associated electronics shall be capable of operating within the specifications above at MIP rates up to 3 kHz. (The 3kHz per tile is just above the high count rate.)	ACD Level III Requirements LAT-SS-00016 ACD3-114	
ACD4-210	5.21 Testability		
ACD4-211	The ACD electronics shall incorporate additional capabilities as needed to enable thorough and efficient testing, throughout the GLAST mission, of the functions required of the ACD.	ACD Level III Requirements LAT-SS-00016 ACD3-72 ACD Level III Requirements LAT-SS-00016 ACD3-68	
ACD4-212	5.22 Center of Mass		
ACD4-213	The ACD center of mass shall be X=Y<5 mm and Z<393 mm as listed in the ACD-LAT ICD (LAT-SS-00363)	ACD Level III Requirements LAT-SS-00016 ACD3-95 ACD ICD LAT-SS-00363 ACDICD-11	
ACD4-214	5.23 Volume		
ACD4-215	As shown in the ACD IDD (Interface Definition Drawings) (LAT-DS-00309, 00040 & 00038), the ACD volume shall be:	ACD Level III Requirements LAT-SS-00016 ACD3-99	Also driven by (LAT-DS-00309) LAT IDD !
ACD4-216	Inside LAT Grid: 1574 x 1574 x -204.7 mm		
ACD4-217	Inside LAT Tracker: 1515.5 x 1515.5 x 650 mm		

Doors ID	LAT ACD Subsystem Level IV Requirements	In-links at depth 1	Link Comment
ACD4-218	Outside: 1806 x 1806 x 1050 mm (these dimensions have been agreed upon by all of the necessary individuals, however, they will be finalized upon the signature approval of the LAT ACD Interface Definition Drawings. The previous outside volume is 1796 x 1796 x 1015 mm.		
ACD4-219	5.24 Instrument Coverage		
ACD4-220	The ACD TDA's shall cover the top and sides of the LAT trackers down to 0.5 mm below the top of the CsI in the Calorimeter. See ACD IDD (Interface Definition Drawings) (LAT-DS-00309, 00040 & 00038).	ACD Level III Requirements LAT-SS-00016 ACD3-22	Also driven by (LAT-DS-00309) LAT IDD
ACD4-221	5.25 LAT to ACD Gap.		
ACD4-222	The minimum ACD distance from the LAT Trackers shall be as defined in LAT-DS-00038 or ACD IDD (Interface Definition Drawings) (LAT-DS-00309, 00040 & 00038).	ACD Level III Requirements LAT-SS-00016 ACD3-22	
ACD4-223	5.26 Material interaction of gamma radiation (Gamma radiation due to ACD material interactions)		
ACD4-224	The ACD shall cause interaction of less than 6% of the incident gamma radiation.	ACD Level III Requirements LAT-SS-00016 ACD3-102	
ACD4-225	5.27 Thermal Blanket/ Micrometeoroid Shield Areal Mass Density		

Doors ID	LAT ACD Subsystem Level IV Requirements	In-links at depth 1	Link Comment
ACD4-226	The thermal blanket/micrometeoroid shield shall have mass per unit area of ~ <0.32 g/cm^2 which should minimize secondary gamma-ray production by undetected cosmic ray interactions.	ACD Level III Requirements LAT-SS-00016 ACD3-102 ACD Level IV Requirements and Verification LAT-SS-00352 ACD4-224	
ACD4-227	5.28 Gaps between scintillating tiles		
ACD4-228	The gaps between scintillating tiles shall be small enough over the operating temperature range to meet the ACD efficiency requirement. See tile gap analysis trade study.	ACD Level III Requirements LAT-SS-00016 ACD3-20	
ACD4-229	5.29 Light Throughput		
ACD4-230	The amount of light transmitted from the scintillating tiles to the PMT shall be sufficient to produce a signal of 18 P.E. for one MIP.	ACD Level III Requirements LAT-SS-00016 ACD3-20	

6.0 VERIFICATION STRATEGY

The verification strategy will test, analyze (may include modeling/simulation), inspect, or demonstrate all requirements of section 5 to ensure that the instrument meets the requirements of this specification.

Testability and verification commentary

The ACD electronics shall incorporate additional capabilities as needed to enable thorough and efficient testing, throughout the GLAST mission, of the functions required of the ACD.