LAT PROJECT DOCUMENT CHANGE NOTICE (DCN)

DCN No. LAT-XR-842-03

SHEET 1 **OF** 1

ORIGINATOR: Rich Bielawski	**PHONE:** 408-245-0726	**DATE:** 4/21/03
CHANGE TITLE: ACD-LAT Interface Control Document (ICD)-Mechanical, Thermal, and Electrical		**ORG.:**

DOCUMENT NUMBER	TITLE	NEW REV.
LAT-SS-00363	ACD-LAT Interface Control Document (ICD)-Mechanical, Thermal	05
	And Electrical	

CHANGE DESCRIPTION (FROM/TO):

(1) General: Fixed typographical and grammatical errors
(2) Sec 2: Deleted extraneous text
(3) Sec 5: Corrected drawing title of LAT-DS-00309, ACD-LAT Interface Definition Drawing
(4) Sec 5: Added LAT-TD-00035, LAT Coordinate and Numbering Systems
(5) Sec 6.1: Corrected document title of LAT-TD-00035, LAT Coordinate and Numbering Systems
(6) Sec 6.2.1: Added "All bolts, washers and other hardware used on the flight article shall be from the NASA/GSFC approved parts list."
(7) Sec 6.3.1: Added to section title "Reference Only"
(8) Sec 6.3.2: Updated CG requirement
(9) Sec 6.4.2: Replaced "must" with "shall"
(10) Sec 6.5: Refers to the LAT Environmental Specification, LAT-SS-00778 for ACD structural and environmental requirements
(11) Sec 8: Updated text
(12) Sec 8: Updated Figure 1, AEM to ACD Electrical Interface
(13) Sec 8.1.2: Changed text to refer to connector backshell series instead of specific connector backshell model number
(14) Sec 8.1.5: Added Figure 3, ACD BEA Connector Locations
(15) Sec 8.1.5: Replaced TBD's with "ACD" in Table 1, Electronics Interface Connector Reference Designator
(16) Sec 8.2: Section reorganized; Added text for high level description of instrumentation connectors

REASON FOR CHANGE:

ACTION TAKEN: ☒ **Change(s) included in new release** ☐ **DCN attached to document(s), changes to be included in next revision**
☐ **Other (specify):**

DISPOSITION OF HARDWARE (IDENTIFY SERIAL NUMBERS):	**DCN DISTRIBUTION:**
☒ **No hardware affected (record change only)**	
☐ **List S/Ns which comply already:**	
☐ **List S/Ns to be reworked or scrapped:**	
☐ **List S/Ns to be built with this change:**	
☐ **List S/Ns to be retested per this change:**	
☐	

SAFETY, COST, SCHEDULE, REQUIREMENTS IMPACT? ☐ **YES** ☒ **NO**
If yes, CCB approval is required. Enter change request number:

APPROVALS	DATE	OTHER APPROVALS (specify):	DATE
ORIGINATOR: Rich Bielawski (signature on file)	4/21/03	ACD- D. Thompson (signature on file)	4/24/03
ORG. MANAGER: Dick Horn (signature on file)	4/21/03	P&SA- D. Marsh (signature on file)	4/21/03
Chief Mechanical- M. Nordby (signature on file)	4/24/03	I&T- E. Bloom (signature on file)	4/28/03
Chief Electrical- G. Haller (signature on file)	4/24/03	Mechanical- M. Campell (signature on file)	4/21/03
Chief Design- L. Klaisner (signature on file)	4/21/03		
DCC RELEASE: Natalie Cramar (signature on file)	4/21/03	Doc. Control Level: ☒ Subsystem ☐ LAT IPO ☐ GLAST Project	

Continuation:

(17) Sec 8.2.1.1:Updated connector part number from JTP02RE-16-35P to JTP02RE-14-35P
(18) Sec 8.2.1.1:Updated connector shell size from 16 to 14
(19) Sec 8.2.1.1:Updated number of pins from 55 to 37
(20) Sec 8.2.1.1:Updated text on instrumentation connector location
(21) Sec 8.2.1.2: Updated connector part number from JT06RT-16-35S to JT06RT-14-35S
(22) Sec 8.2.1.1:Updated connector shell size from 16 to 14
(23) Sec 8.2.1.1:Updated number of pins from 55 to 37
(24) Sec 8.2.1.1: Changed text to refer to connector backshell series instead of specific connector backshell model number
(25) Sec 8.2.1.3:Updated section title
(26) Sec 8.2.1.3:Replaced "thermistors" with "temperature sensors"
(27) Sec 8.2.1.4:Updated text
(28) Sec 8.2.1.4:Updated Table 3, Safe Mode Temperature Connector Reference Designators
(29) Sec 8.2.2: Updated text, added thermistor details
(30) Sec 8.2.2: Updated Table 4, Temp1 Signals and Pinout
(31) Sec 8.2.3: Added new section, ACD to ACD Temp Sensor Bracket. Section includes connector description and location, harness description, naming convention for connector designator, thermistor and PRT details, signal names and pinout
(32) Sec 8.6: Refers to the LAT Environmental Specification, LAT-SS-00778 for ACD EMI/EMC requirements
(33) Sec 11.1: Refers to the LAT Environmental Specification, LAT-SS-00778 for ACD thermal requirements
(34) Sec 11.2: Refers to the LAT Environmental Specification, LAT-SS-00778 for LAT thermal requirements as it pertains to the ACD
(35) Sec 11.5: Refers to the ACD-LAT IDD, LAT-DS-00309 for the bolted joint details
(36) Sec 13.2: Refers to the LAT Survey and Alignment Test Plan, LAT-MD-01586 and the ACD-LAT IDD, LAT-DS-00309 for survey, alignment, datum structure, and fiducial location details
(37) Sec 13.3: Refers to the LAT Instrumentation Plan, LAT-TD-00890 and the ACD Integration and Test Plan, LAT-TD-00430 for flight and test instrumentation used during test.
(38) Sec 13.4.1:Added helium monitoring equipment
(39) Sec 13.4.2:Moved to this section, "LAT will provide enough information for ACD to manufacture a Grid simulator for testing purposes."
(40) Sec 14.2: Updated helium monitoring requirement

Reason for Change:

(1) Fix known errors.
(2) Clarify text.
(3) Incorrect drawing title.
(4) Missing reference document.
(5) Incorrect document title.
(6) Clarify requirement.
(7) Mass section is reference only.
(8) CG requirement was out of date.
(9) Keep document language consistent.
(10) LAT Environmental Specification is the source for structural and environmental requirements.
(11) - (32) Updated to reflect current design.
(33), (34) LAT Environmental Specification is the source thermal requirements.
(35) ACD-LAT IDD is the source for bolt details.
(36) LAT Survey and Alignment Test Plan is the source for surveying and alignment requirements.
(37) LAT Instrumentation Plan and the ACD Integration & Test Plan are the source documents for instrumentation used during test.
(38) Requirement was not published in any other documents.
(39) Requirement is most appropriate in the I&T section.
(40) Clarify helium monitoring requirement.

	Document # **LAT-SS-00363-05**	Date Effective 4/18/03
	Prepared by(s) M. Amato, G. Shiblie G. Haller, M. Nordby, G. Unger, D Shepard, K. Segal, R. Bielawski	Supersedes Previous
GLAST LAT SUBSYSTEM SPECIFICATION	Subsystem/Office ACD Subsystem, Electrical and Mechanical systems	
Document Title **ACD-LAT Interface Control Document (ICD) – Mechanical, Thermal and Electrical**		

Gamma-ray Large Area Space Telescope (GLAST)

Large Area Telescope (LAT)

ACD-LAT Interface Control Document (ICD) – Mechanical, Thermal and Electrical

CHANGE HISTORY LOG

Revision	Effective Date	Description of Changes
1	12/28/01	Initial Draft
2	4/4/02	Initial Release – Authorized
3	4/29/02	Draft of combined version of Mech and Elect ICD
4	12/5/02	Extensive updates since dPDR DCN LAT-XR-00842-02
5		Updated for CDR, see DCN LAT-XR-00842-03 for details.

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1. Purpose

The ACD-LAT ICD delineates interfaces so that subsystem components can be designed and fabricated based on clear, understood values for their interfaces to the rest of the LAT. This ICD will also serve as a requirements list against which interface tests are developed, and against which the ACD subsystem must be verified prior to integration on the LAT. This document establishes and describes the electrical interface between the ACD Front-end Electronics (i.e. Front-end event electronics (FREE) circuit card) and the ACD Electronics Module (AEM). Also, this document establishes and describes the mechanical and thermal interfaces between the Anticoincidence Detector (ACD) subsystem and the LAT

2. Scope

The scope of this ICD document includes two areas. One is the electrical interface between the ACD Front-end Electronics and the ACD Electronics Module. The interconnections as well as the commanding and dataflow are described. The second area includes all mechanical and thermal interfaces between the LAT and the ACD.

3. Acronyms

ACD – Anticoincidence Detector

ADC – Analog to Digital Converter

AEM – ACD Electronics Module

AGN – Active Galactic Nuclei

BEA – Base Electronics Assembly

BOL – Beginning of Life

CAL – Calorimeter

CFC - Carbon Fiber Composite

CG – Center of Gravity

CNO – Carbon-Nitrogen-Oxide

CTE - Coefficient of Thermal Expansion

DC – Direct Current

DFS – Data-Flow System

EMI – Electromagnetic Interference

EOL – End of Life

FREE – Front-End Electronics

GAFE – GLAST Analog Front End

GARC – GLAST Analog Readout Controller

GLAST – Gamma-ray Large Area Space Telescope

GLT – Global Trigger

GRB – Gamma-Ray Burst

GSE - Ground Support Equipment

GSFC – Goddard Space Flight Center

HLD – High Level Discriminator

HVBS – High Voltage Bias Supply

ICD – Interface Control Document

IRD – Interface Requirements Document

LAT – Large Area Telescope

LLD – Low Level Discriminator

LVDS – Low Voltage Differential Signal

M-GSE - Mechanical Ground Support Equipment

MIP – Minimum Ionizing Particle

MLI – Multi-Layer Insulation

MPLS – Multi-Purpose Lifting Sling

MSB – Most Significant Bit

N – Newtons

PMT – Photo-Multiplier Tube

RMS – Root Mean Square

SRD – Science Requirements Document

TACK – Trigger Acknowledge

TBR – To Be Resolved

TBD - To Be Determined

T&DF – Trigger and Dataflow System

TEM - Tower Electronics Module

TKR – Tracker

TRG – Trigger

TSA – Tile Shell Assembly

4. Definitions

μsec, μs – Microsecond, 10^{-6} second

Analysis – A quantitative evaluation of a complete system and /or subsystems by review/analysis of collected data.

Background Rejection – The ability of the instrument to distinguish gamma rays from charged particles.

cm – centimeter

Cosmic Ray Œ Ionized atomic particles originating from space and ranging from a single proton up to an iron nucleus and beyond.

Demonstration – To prove or show, usually without measurement of instrumentation, that the project/product complies with requirements by observation of results.

Event – an event results in that the instrument is triggered and the data associated to that event is read out.

Inspection – To examine visually or use simple physical measurement techniques to verify conformance to specified requirements.

Nominal MIP – 1 MIP produces a PMT anode signal of 0.64pC

MeV – Million Electron Volts, 10^6 eV

MHz – Megahertz, 10^6 hertz

s, sec – seconds

Simulation – To examine through model analysis or modeling techniques to verify conformance to specified requirements

TACK - Trigger Acknowledge signal distributed from the trigger system to the detector sub-systems. The sub-systems save the event data in an event buffer when receiving this signal.

Testing – A measurement to prove or show, usually with precision measurements or instrumentation, that the project/product complies with requirements.

Trigger – generates a decision whether to readout the instrument and distributes a Trigger Acknowledge to acquire event data considering data received from the detector sub-systems.

V - Volts

Validation – Process used to assure the requirement set is complete and consistent, and that each requirement is achievable.

Verification – Process used to ensure that the selected solutions meet specified requirements and properly integrate with interfacing products.

5. Applicable Documents

1. ANSI Y 14.5M Standard
2. Directive 561-PG-8700.2.1, Flight FPGA Design Guidelines
3. Directive 564-PG-8700.2.1, Microelectronics and Signal Processing Branch
4. GEVS-SE General Environmental Verification Specification for STS & ELV Payloads, Subsystems, and Components
5. GSFC-433-RQMT GLAST EMI/EMC Requirements Document
6. LAT-DS-00038 LAT Mechanical Systems Mechanical Integration LAT Instrument Layout
7. LAT-DS-00309 ACD-LAT Interface Definition Dwg
8. LAT-DS-01151 ACD Outline Drawing
9. LAT-TD-00890 LAT Instrumentation Plan
10. LAT-SS-00010 LAT level IIb specifications
11. LAT-SS-00016 ACD level III requirements/specifications
12. LAT-TD-00035 LAT Coordinate and Numbering Systems
13. LAT-SS-00289 Conceptual Design of the LAT ACD Electronics Module
14. LAT-SS-00291 Electrical Grounding and Shielding Plan
15. LAT-SS-00352 ACD level IV requirements/specifications
16. LAT-SS-00458 LAT Electronics Subsystem Preliminary Design Report
17. LAT-SS-00778 LAT Environmental Specification
18. LVDS Owner's Manual (A General Design Guide for National's LVDS and Bus LVDS Products), 2nd Edition

6. Mechanical Interfaces

6.1. General Description

The ACD-Grid interface is the primary mechanical interface for the ACD. This provides the structural support and stability for the ACD, and provides a stable reference by which the ACD position is surveyed and maintained. This interface also provides the primary means for conductive heat transfer.

The reference coordinate system is shown in LAT Coordinate and Numbering System, LAT-TD-00035.

The System of Units used shall be metric.

The most up to date Grid drawing and the most up to date versions of other drawings referred to in this document reside on the LAT web site on Cyberdocs.

All drawings included in this document or referred to shall meet ANSI Y14.5M standards.

6.2. Flight Hardware

6.2.1. ACD Responsibilities

Development, fabrication, test, and delivery of the following components:

ACD flight unit with interfaces as described in this document.

MLI and micrometeoroid shield to cover the ACD, with thermal properties and coverage as defined in this document.

Bolts, washers, and any other hardware needed to attach the ACD to the Grid. All bolts, washers and other hardware used on the flight article shall be from the NASA/GSFC approved parts list.

Thermally conductive material, as needed to meet the interface requirements described in this document, to be used at the ACD-Grid interface joint.

6.2.2. LAT Responsibilities

Development, fabrication, and test of the following components:

Grid structure to support the ACD, with interfaces as specified in this document.

The ACD to LAT AEM flight cable harness.

Cableway and attachments for routing of the ACD to LAT AEM cable harness.

6.3. Mass Properties

6.3.1. Mass (Reference Only)

The ACD mass will be less than 280 Kg.

6.3.2. Center of Gravity

The maximum X/Y center of gravity offset from the geometric center of the ACD shall be +/- 10 mm. The Z-axis CG position shall be less than 340 mm where Z=0 is the top of the grid.

6.4. Structural Mounting and Load Transfer

6.4.1. ACD Requirements

The ACD is mounted to the Grid as shown in the LAT-ACD IDD drawing, LAT-DS-00309.

The ACD mount to the Grid shall conform to the dimensions and tolerances shown in LAT-ACD IDD drawing, LAT-DS-00309.

There is currently no specific requirement for surface preparation or coefficient of friction; friction will not be assumed to carry load.

The ACD structure at the Grid interface shall have a CTE of 21-25 x 10^{-6} m/m/degC (consistent with aluminum material)

6.4.2. LAT Requirements

The Grid mounting bosses for the ACD shall conform to the dimensions and tolerances shown in LAT-ACD IDD, LAT-DS-00309.

The Grid structure shall have a CTE of 21-25 x 10^{-6} m/m/degC (consistent with aluminum material)

The Grid shall be available for Grid to ACD pinning operation and fit check; this will be done during fit check before delivery.

6.5. Structural Interface Loads and Environmental Requirements

Structural interface loads and environmental test requirements are specified in the LAT Environmental Specification, LAT-SS-00778. Mechanical environmental tests are specified in the LAT Instrument Performance Verification Plan, LAT-MD-00408 and the ACD Integration and Test Plan, LAT-TD-00430

6.5.1. ACD Requirements

6.5.1.1 First Mode Frequency

The fixed base stiffness, fixed at the LAT-ACD interface points, shall produce a first mode frequency greater than 50 Hz.

6.5.1.2 Static-Equivalent Accelerations

Refer to LAT Environmental Specification, LAT-MD-00778, Section 8.1, Static-Equivalent Accelerations.

6.5.1.3 ACD-Grid Interface Loads

Refer to LAT Environmental Specification, LAT-MD-00778, Section 8.2, Interface Limit Loads.

6.5.1.4 Sinusoidal Vibration

Refer to LAT Environmental Specification, LAT-MD-00778, Section 9.1, Sinusoidal Vibration.

6.5.1.5 Random Vibration

Refer to LAT Environmental Specification, LAT-MD-00778, Section 9.2, Random Vibration.

6.5.1.6 Acoustic Spectrum

Refer to LAT Environmental Specification, LAT-MD-00778, Section 9.3, Acoustic.

6.5.1.7 Shock Environment

Refer to LAT Environmental Specification, LAT-MD-00778, Section 10, Shock Environment.

ACD interfaces with LAT shall be able to withstand the maximum expected interface reactions without any violation of the ACD structural requirements. This will be demonstrated by test and/or analysis.

6.5.2. LAT Requirements

The Grid shall be capable of tolerating the reaction forces due to ACD acceleration and vibration loading. LAT interfaces with ACD shall be able to withstand the maximum expected interface reactions without any violation of the LAT structural requirements. This will be demonstrated by test and/or analysis.

7. Dimensions

Stay-clear dimensions are not-to-exceed dimensions. The nominal dimensions plus any needed tolerances is included within this stay-clear. These dimensions are defined, and are measured with respect to a unique datum reference system.

7.1. Nominal Stay-Clear Dimensions

The ACD subsystem components shall stay within the stay-clear volume described in LAT-ACD IDD drawing, LAT-DS-00309. ACD stay-clears and dimensions shall be quoted and measured with respect to the datum reference system defined in the LAT-ACD IDD drawing, LAT-DS-00309. Stay-clear dimensions are to be measured at 21 +/- 3 degrees C.

7.2. Stay-Clear for Dynamic and Thermal Motions

Maximum excursions beyond the static stay-clears are:

Allowed Lateral Dynamic Motions

1 mm inward motion of the TSA CFC shell.
2 mm outward motion of the TSA CFC shell on the outside of the ACD.
10 mm outward motion of the MLI shielding.
Thermal contraction/dilation of the interfaces to the Grid, consistent with the thermal expansion coefficient of aluminum.

Allowed Vertical Dynamic Motions

4 mm downward motion of the TSA CFC shell.

8. Electrical Interfaces

The ACD electrically interfaces to the AEMs, Power Distribution Unit (PDU) and Spacecraft, see Figure 1. The ACD electronics interfaces to the AEM through 24 connectors (twelve to AEM (A) and twelve to AEM (B)) that are mounted on the BEA. This interface passes through the LAT DAQ EMI Shield. These twenty-four (24) bulkhead connectors penetrate the DAQ EMI shield and route to the AEMs. These connectors carry all of the ACD digital I/O signals and power to ACD; and some of the analog sensors. All of the temperatures sensors that are distributed on the ACD, outside of the BEA, electrically interface either the PDU or the Spacecraft. Temperature sensor signals routed to the PDU pass through the DAQ EMI Shield. Temperature sensor signals routed to the spacecraft pass through an ACD Temp Sensor Bracket located outside of the DAQ EMI shield.

The harness connecting the ACD front-end to the LAT EMI shield connectors is described in this document. The LAT DAQ subsystem is responsible for all cables between the Base Electronics Assembly and the LAT DAQ EMI shield and ACD Temp Sensor Bracket.

All signal characteristics are specified and measured on connectors at the BEA interface.

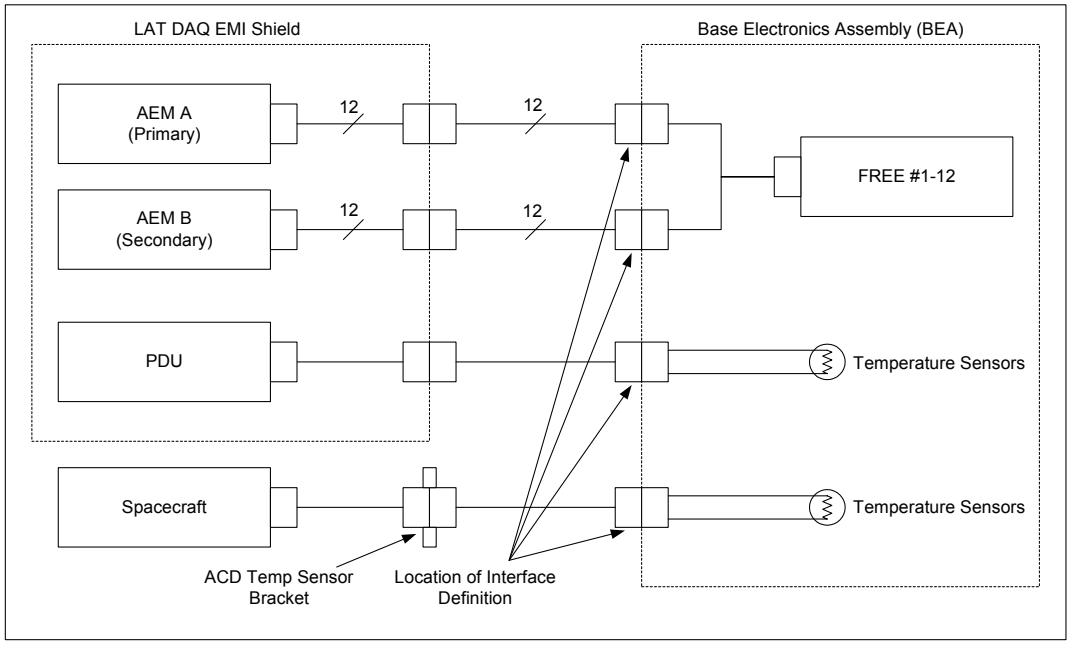

Figure 1 AEM to ACD Electrical Interface

8.1. Cable and Connectors Between ACD and LAT

8.1.1. ACD Base Electronics Assembly Bulkhead Connector, (Receptacle)

The connector part number is JTP02RE-20-35P(453) which is a MIL-DTL-38999 Series II bayonet coupling low profile metal shell connector with size 22 (high-density) contacts. The shell size is 20, and number of pins is 79. The arrangement of pins is shown below. Figure 2 shows the connector.

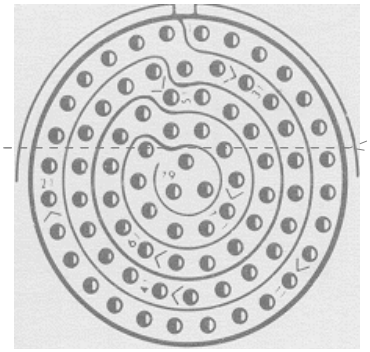

Figure 2 G35 Pin Arrangement

This connector is listed on the NASA Parts Selection List (NPSL) and data may also be found at the following website, http://nepp.nasa.gov/npsl/Connectors/m38999/38999_s3.htm. The ACD bulkhead connectors have male pins.

Twelve (12) of the 24 total connectors interface to AEM A connectors, and the other 12 connectors interface to AEM B connectors. There are 60 conductors for each cable and interface and the signal are identified in Table 2, Signals List.

8.1.2. Connector at ACD BEA Side, (Plug)

This connector is a plug that mates to the bulkhead connector listed in 8.1.1. The connector part number is JT06RT-20-35S(453) which is a MIL-DTL-38999 Series II bayonet coupling metal shell connector with size 22 (high-density) contacts. The shell size is 20, and number of pins is 79. The arrangement of pins is shown in Figure 2. This connector shall have an M85049/76 series right-angled backshell selected from the NPSL for cable strain relief.

This connector is listed on the NASA Parts Selection List (NPSL) and may be found at http://nepp.nasa.gov/npsl/Connectors/m38999/38999_s3.htm. This connector has sockets.

8.1.3. Connector at ACD Electronics Module Side (for info only)

The connector on the AEM is a right angle 100 pin micro-D metal shell connector manufactured by Cristek Interconnects, Inc. The part number is MCR-1-100-1B1.

8.1.4. Harness between ACD BEA and ACD Electronics Module

The harness from the ACD BEA to the LAT EMI shield is approximately 0.75 m long (Ref) and consists of 24 AWG wires for all signals and power. The power lines in the harness will have a harness shield, separate from the harness shield on the signal wires. These shields shall be grounded at both ends. The overall harness shall also have a harness shield, which shall be grounded at both ends. The method used to ground these shields shall provide optimum grounding contact with the backshell and connector and should avoid using a drain wire for grounding the shield.

The harness from the LAT EMI shield to the AEM has the same design, and is up to 1 m (Ref) long.

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8.1.5. Naming Convention for Connector Designators

The following Table 1 lists the designation for each connector at the BEA interface. The connectors mounted on the BEA shall be clearly marked with these designations. The mating connectors at the end of the DAQ cables shall be clearly labeled with these designations.

Deleted: Table 1

The exact ACD BEA connector locations for each connector shall be documented in the ACD Outline Drawing, LAT-DS-01151. For the purposes of the ICD, the location of the connectors will be defined by the X or Y coordinate and the general location of the connector as defined in Figure 3. The location of each individual connector is defined in Table 1 and Table 3.

Deleted: Table 1

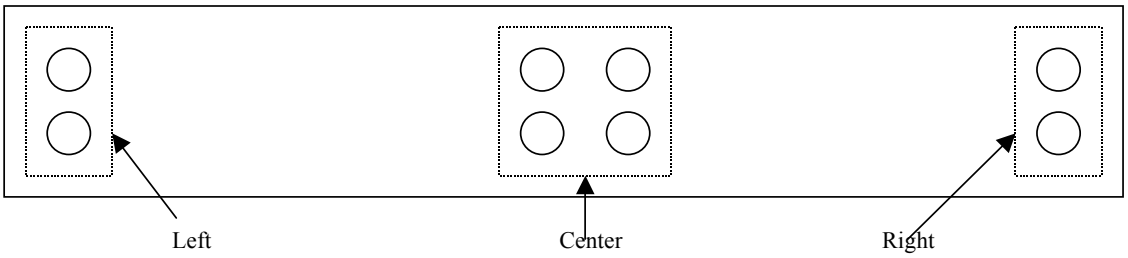


Figure 3 ACD BEA Connector Locations (Outside looking into BEA)

Table 1 Electronics Interface Connector Reference Designator

FREE Designator	ACD Connector Location	Connecting AEM	BEA Connector Designator	LAT Connector Designator	LAT Cable Number
1LA	-X, Center	Prime(A)	ACD-1LAJ1	ACD-P1	ACD-W1
1LA	-X, Center	Redundant(B)	ACD-1LAJ2	ACD-P2	ACD-W2
1RB	-X, Center	Prime(A)	ACD-1RBJ3	ACD-P3	ACD-W3
1RB	-X, Center	Redundant(B)	ACD-1RBJ4	ACD-P4	ACD-W4
2LA	–Y, Center	Prime(A)	ACD-2LAJ7	ACD-P7	ACD-W7
2LA	–Y, Center	Redundant(B)	ACD-2LAJ8	ACD-P8	ACD-W8
2LB	–Y, Left	Prime(A)	ACD-2LBJ5	ACD-P5	ACD-W5
2LB	–Y, Left	Redundant(B)	ACD-2LBJ6	ACD-P6	ACD-W6
2RA	–Y, Right	Prime(A)	ACD-2RAJ11	ACD-P11	ACD-W11
2RA	–Y, Right	Redundant(B)	ACD-2RAJ12	ACD-P12	ACD-W12
2RB	–Y, Center	Prime(A)	ACD-2RBJ9	ACD-P9	ACD-W9
2RB	–Y, Center	Redundant(B)	ACD-2RBJ10	ACD-P10	ACD-W10
3LA	+X, Center	Prime(A)	ACD-3LAJ13	ACD-P13	ACD-W13
3LA	+X, Center	Redundant(B)	ACD-3LAJ14	ACD-P14	ACD-W14
3RB	+X, Center	Prime(A)	ACD-3RBJ15	ACD-P15	ACD-W15
3RB	+X, Center	Redundant(B)	ACD-3RBJ16	ACD-P16	ACD-W16
4LA	+Y, Center	Prime(A)	ACD-4LAJ19	ACD-P19	ACD-W19
4LA	+Y, Center	Redundant(B)	ACD-4LAJ20	ACD-P20	ACD-W20
4LB	+Y, Left	Prime(A)	ACD-4LBJ17	ACD-P17	ACD-W17
4LB	+Y, Left	Redundant(B)	ACD-4LBJ18	ACD-P18	ACD-W18
4RA	+Y, Right	Prime(A)	ACD-4RAJ23	ACD-P23	ACD-W23
4RA	+Y, Right	Redundant(B)	ACD-4RAJ24	ACD-P24	ACD-W24
4RB	+Y, Center	Prime(A)	ACD-4RBJ21	ACD-P21	ACD-W21
4RB	+Y, Center	Redundant(B)	ACD-4RBJ22	ACD-P22	ACD-W22

8.1.6. Signal Names

8.1.6.1 Signal Naming

The signal name format is: ACD_nnnnnn_##xy where
nnnnnn is the signal name
is an optional 2 digit number
x is A or B indicating the A or B interface
y is P or M indicating positive or negative for differential signals

All digital signals except ACD_CLK are transmitted and received low true and so indicated by using "N" as the first character of the signal name. This convention is used to take advantage of the fact that the LVDS receivers default to the high state if the inputs open or are disconnected.

8.1.6.2 Signal List

A list of each of the signal wires between the ACD and the AEM (A interface only) is detailed below in Table 3.

Table 2 Signal List

Signal Name	Signal Description	Signal Bundle No.	Pin No.	Input (I) Output (O) Analog(A) Power (P)	Wire Type and Gauge
ACD_CLK_AP	Clock+ to ACD	1	79	I	24 AWG, TP
ACD_CLK_AM	Clock- to ACD		78		
ACD_NSCMD_AP	Command+ to ACD	2	77	I	24 AWG, TP
ACD_NSCMD_AM	Command- to ACD		76		
ACD_NRST_AP	Reset+ to ACD	3	75	I	24 AWG, TP
ACD_NRST_AM	Reset- to ACD		74		
ACD_NSDATA_AP	Data+ to AEM	4	73	O	24 AWG, TP
ACD_NSDATA_AM	Data- to AEM		72		
ACD_NVETO_00AP	Veto Ch 0 + to AEM	5	71	O	24 AWG, TP
ACD_NVETO_00M	Veto Ch 0 - to AEM		70		
ACD_NVETO_01AP	Veto Ch 1 + to AEM	6	69	O	24 AWG, TP
ACD_NVETO_01AM	Veto Ch 1 - to AEM		68		
ACD_NVETO_02AP	Veto Ch 2 + to AEM	7	67	O	24 AWG, TP
ACD_NVETO_02AM	Veto Ch 2 - to AEM		66		

Table 2 Signal List

Signal Name	Signal Description	Signal Bundle No.	Pin No.	Input (I) Output (O) Analog(A) Power (P)	Wire Type and Gauge
ACD_NVETO_03AP	Veto Ch 3 + to AEM	8	65	O	24 AWG, TP
ACD_NVETO_03AM	Veto Ch 3 - to AEM		64		
ACD_NVETO_04AP	Veto Ch 4 + to AEM	9	63	O	24 AWG, TP
ACD_NVETO_04AM	Veto Ch 4 - to AEM		62		
ACD_NVETO_05AP	Veto Ch 5 + to AEM	10	61	O	24 AWG, TP
ACD_NVETO_05AM	Veto Ch 5 - to AEM		60		
ACD_NVETO_06AP	Veto Ch 6 + to AEM	11	59	O	24 AWG, TP
ACD_NVETO_06AM	Veto Ch 6 - to AEM		58		
ACD_NVETO_07AP	Veto Ch 7 + to AEM	12	57	O	24 AWG, TP
ACD_NVETO_07AM	Veto Ch 7 - to AEM		56		
ACD_NVETO_08AP	Veto Ch 8 + to AEM	13	55	O	24 AWG, TP
ACD_NVETO_08AM	Veto Ch 8 - to AEM		54		
ACD_NVETO_09AP	Veto Ch 9 + to AEM	14	53	O	24 AWG, TP
ACD_NVETO_09AM	Veto Ch 9 - to AEM		52		
ACD_NVETO_10AP	Veto Ch 10 + to AEM	15	51	O	24 AWG, TP
ACD_NVETO_10AM	Veto Ch 10 - to AEM		50		
ACD_NVETO_11AP	Veto Ch 11 + to AEM	16	49	O	24 AWG, TP
ACD_NVETO_11AM	Veto Ch 11 - to AEM		48		
ACD_NVETO_12AP	Veto Ch 12 + to AEM	17	47	O	24 AWG, TP
ACD_NVETO_12AM	Veto Ch 12 - to AEM		46		
ACD_NVETO_13AP	Veto Ch 13 + to AEM	18	45	O	24 AWG, TP
ACD_NVETO_13AM	Veto Ch 13 - to AEM		44		
ACD_NVETO_14AP	Veto Ch 14 + to AEM	19	43	O	24 AWG, TP
ACD_NVETO_14AM	Veto Ch 14 - to AEM		42		
ACD_NVETO_15AP	Veto Ch 15 + to AEM	20	41	O	24 AWG, TP

Table 2 Signal List

Signal Name	Signal Description	Signal Bundle No.	Pin No.	Input (I) Output (O) Analog(A) Power (P)	Wire Type and Gauge
ACD_NVETO_15AM	Veto Ch 15 - to AEM		40		
ACD_NVETO_16AP	Veto Ch 16 + to AEM	21	17	O	24 AWG, TP
ACD_NVETO_16AM	Veto Ch 16 - to AEM		18		
ACD_NVETO_17AP	Veto Ch 17 + to AEM	22	19	O	24 AWG, TP
ACD_NVETO_17AM	Veto Ch 17 - to AEM		20		
ACD_NCNO_AP	CNO + to AEM	23	21	O	24 AWG, TP
ACD_NCNO_AM	CNO - to AEM		22		
ACD_HV1_AP	HVBS 1 Monitor + to AEM	24	23	A	24 AWG, TP
ACD_HV1_AM	HVBS 1 Monitor - to AEM		24		
ACD_TEMP_AP	Temp Monitor + to AEM	25	25	A	24 AWG, TP
ACD_TEMP_AM	Temp Monitor - to AEM		26		
ACD_HV2_AP	HVBS 2 Monitor + to AEM	26	27		
ACD_HV2_AM	HVBS 2 Monitor – to AEM		28		
ACD_VDD_0A	+3.3V Power to ACD	27	1	P	24 AWG, Twisted Wires
ACD_GND_0A	+3.3V Power Return		30		
ACD_VDD_1A	+3.3V Power to ACD		3	P	
ACD_GND_1A	+3.3V Power Return		31		
ACD_VDD_2A	+3.3V Power to ACD		4	P	
ACD_GND_2A	+3.3V Power Return		32		
ACD_28V_0A	+28V Power to ACD HVBS	28	5	P	24 AWG, Twisted Wires
ACD_28V_RTN_0A	+28V Return		33		
ACD_28V_1A	+28V Power to ACD HVBS		7	P	
ACD_28V_RTN_1A	+28V Return		34		
Not Used	Pins 2, 6, 8-16, 29, 35-39 not used	29	rest	-	-

8.1.7. Digital Inputs and Outputs

LVDS is used for all digital signals. The signal current is 3.5 mA, and the termination resistor is 100 ohms.

8.1.8. Signal Description

ACD_CLK: 20 MHz ± 1% continuous, 45-55% duty cycle clock from the ACD Electronics Module (AEM).

ACD_NSCMD: The command signal from AEM. The ACD_NSCMD signal transitions on the trailing edge of ACD_CLK and is shifted into the ACD on the leading edge of ACD_CLK. A single start bit, (logic 1), signals the beginning of a command.

ACD_NRST: Reset from AEM. ACD_NRST is synchronous to ACD_CLK. ACD_NRST at logic one resets state machines and initializes registers and modes in ACD. The ACD_NRST is at least five ACD_CLK cycles.

ACD_NSDATA: Data from ACD. The ACD_NSDATA signal transitions on the leading edge of ACD_CLK. The beginning of a data packet indicated by a single start bit.

ACD_NCNO, ACD_NVETOs: Veto discriminator output signals from ACD. The ACD_NCNO interface signal is the OR of the selected (via command) HLD discriminators.

ACD_HV: Analog monitor of the high voltage power supply voltage output. 0 - 2.5 volts indicates 0 - full-scale volts at the supply output. Pseudo differential analog, with signal on ACD_HVP and ground on ACD_HVN, 10K ± 5% source impedance all lines.

ACD_TEMP: ACD board temperature monitor, 30K thermistor, GSFC S-311-P-18 series (YSI 44900 series).

ACD_VDD(0-2): +3.3V supplied by the AEM to the ACD FREE circuit cards.

ACD_28V(0-1): +28V supplied by the AEM to the ACD HVBSs.

8.2. ACD Flight Instrumentation Connectors

The ACD shall provide two thermal instrumentation connectors, each containing temperature sensors. One connector contains only safe mode temperature sensors and interfaces to the PDU. The second connector contains only survival temperature sensors and interfaces to the Spacecraft.

8.2.1. ACD to PDU Interface

8.2.1.1 ACD (Safe Mode) Instrumentation Connectors, Receptacle

The ACD (Safe Mode) instrumentation connector part number is JTP02RE-14-35P(453) which is a MIL-DTL-38999 Series II bayonet coupling low profile metal shell connector with size 22 (high density) contacts. The shell size is 14, and number of pins is 37. The arrangement of pins is shown in Figure 4.

This connector shall be located on the –X side of the ACD. See the ACD-LAT IDD LAT-DS-00309 and ACD Outline Drawing LAT-DS-01151 for exact location of this connector.

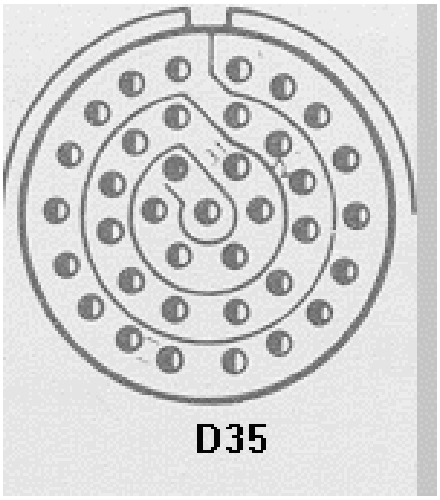


Figure 4. D35 Pin Arrangement

8.2.1.2 Connector at ACD BEA Side, Plug

This connector is a plug that mates to the bulkhead connector listed in 8.2.1.1. The connector part number is JT06RT-14-35S(453) which is a MIL-DTL-38999 Series II bayonet coupling metal shell connector with size 22 (high density) contacts. The shell size is 14, and number of pins is 37. The arrangement of pins is shown in Figure 4. This connector shall have an M85049/76 series right-angled backshell selected from the NPSL for cable strain relief.

8.2.1.3 Harness between ACD BEA and LAT PDU

The harness from the ACD BEA to the LAT EMI shield is approximately 0.75 m long (Ref) and consists of 24 AWG twisted shielded pairs for all temperature sensors. The overall harness shall also have a harness shield, which shall be grounded at both ends.

8.2.1.4 Naming Convention for Connector Designators

The following Table 3 lists the designation for the safe mode instrumentation connector at the BEA interface. The connector mounted on the BEA shall be clearly marked with this designation. The mating connectors at the end of the PDU cable shall be clearly labeled with this designation.

Table 3 Safe Mode Temperature Sensor Connector Reference Designators

Connector Designator	ACD Connector Location	LAT Connection	LAT Connector Designator	LAT Cable Number
TEMP1	-X, Left	PDU	ACD-P25	ACD-W25

8.2.2. Signal Names

The following table lists the signal names for each temperature sensor and the connector pin outs. ACD shall use 30K thermistors, GSFC 311-P-18-09S7R6 (YSI 44909).

Table 4 TEMP1 Signals and Pin out

Sensor Name	Sensor Description	Sensor Type	Pin No.	Wire Type and Guage
XM_PMT_1L_P	-X PMT Rail, Left, Primary	Thermistor	1 2	24 AWG, TSP
XM_PMT_1L_S	-X PMT Rail, Left, Secondary	Thermistor	3 4	24 AWG, TSP
YM_PMT_2L_P	-Y PMT Rail, Right, Primary	Thermistor	5 6	24 AWG, TSP
YM_PMT_2L_S	-Y PMT Rail, Right, Secondary	Thermistor	7 8	24 AWG, TSP
XP_PMT_3L_P	+X PMT Rail, Left, Primary	Thermistor	9 10	24 AWG, TSP
XP_PMT_3L_S	+X PMT Rail, Left, Secondary	Thermistor	11 12	24 AWG, TSP
YP_PMT_4L_P	+Y PMT Rail, Right, Primary	Thermistor	13 14	24 AWG, TSP
YP_PMT_4L_S	+Y PMT Rail, Right, Secondary	Thermistor	15 16	24 AWG, TSP
XP_O_SHELL_P	+X, Outside Composite Shell, Primary	Thermistor	17 18	24 AWG, TSP
XP_O_SHELL_S	+X, Outside Composite Shell, Secondary	Thermistor	19 20	24 AWG, TSP
XM_O_SHELL_P	-X Outside Composite Shell, Primary	Thermistor	21 22	24 AWG, TSP

Sensor Name	Sensor Description	Sensor Type	Pin No.	Wire Type and Guage
XM_O_SHELL_S	-X Outside Composite Shell, Secondary	Thermistor	23 24	24 AWG, TSP
YP_GRID_IF_P	+Y, BEA/Grid Interface, Primary	Thermistor	25 26	24 AWG, TSP
YP_GRID_IF_S	+Y, BEA/Grid Interface, Secondary	Thermistor	27 28	24 AWG, TSP
YM_GRID_IF_P	-Y, BEA/Grid Interface, Primary	Thermistor	29 30	24 AWG, TSP
YM_GRID_IF_S	-Y, BEA/Grid Interface, Secondary	Thermistor	31 32	24 AWG, TSP
Spare		Thermistor	33 34	24 AWG, TSP
Spare		Thermistor	35 36	24 AWG, TSP
Not Used	Pin 37			

8.2.3. ACD to ACD Temp Sensor Bracket Interface

8.2.3.1 ACD (Survival) Instrumentation Connectors, Receptacle

The ACD (Survival) instrumentation connector part number is JTP02RE-18-35P(453) which is a MIL-DTL-38999 Series II bayonet coupling low profile metal shell connector with size 22 (high density) contacts. The shell size is18, and number of pins is 66. The arrangement of pins is shown in Figure 5.

This connector shall be located on the +X side of the ACD. See the ACD-LAT IDD LAT-DS-00309 and ACD Outline Drawing LAT-DS-01151 for exact location of this connector.

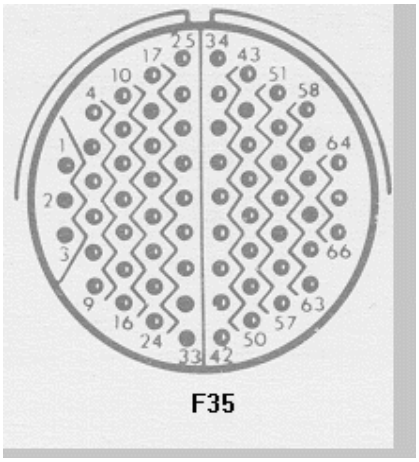


Figure 5. F35 Pin Arrangement

8.2.3.2 Connector at ACD BEA Side, Plug

This connector is a plug that mates to the bulkhead connector listed in 8.2.3.1. The connector part number is JTP06RT-18-35S(453) which is a MIL-DTL-38999 Series II bayonet coupling metal shell connector with size 22 (high density) contacts. The shell size is 18, and number of pins is 66. The arrangement of pins is shown in Figure 5. This connector shall have an M85049/76 series right-angled backshell selected from the NPSL for cable strain relief.

8.2.3.3 Harness between ACD BEA and ACD Temp Sensor Bracket

The harness from the ACD BEA to the ACD Temp Sensor Bracket is approximately 1 m long (Ref) and consists of 24 AWG twisted shielded pairs for all temperature sensors. The overall harness shall also have a harness shield, which shall be grounded at both ends.

8.2.3.4 Naming Convention for Connector Designators

The following Table 5 lists the designation for the survival mode instrumentation connector at the BEA interface. The connector mounted on the BEA shall be clearly marked with this designation. The mating connector at the end of the ACD Temp Sensor Bracket cable shall be clearly labeled with this designation.

Table 5 Survival Mode Temperature Sensor Connector Reference Designator

Connector Designator	ACD Connector Location	LAT Connection	LAT Connector Designator	LAT Cable Number
TEMP2	+X, Left	Spacecraft	ACD-P26	ACD-W26

8.2.3.5 Signal Names

This table lists the signal names for each temperature sensor and the connector pin outs. The ACD shall use two types of temperature sensors: 30K thermistors, PN: 311-P-18-09S7R6 (YSI 44909) and Rosemont PRTs, PN: 118MF2000A. Table 6 will document the sensor type for each signal.

Table 6 TEMP2 Signals and Pin out

Sensor Name	Sensor Description	Sensor Type	Pin No.	Wire Type and Guage
XP_TILE_P	+X Tile, Primary	PRT	1 2	24 AWG, TSP
XP_TILE_S	+X Tile, Secondary	PRT	4 5	24 AWG, TSP
XM_TILE_P	-X Tile, Primary	PRT	6 7	24 AWG, TSP
XM_TILE_S	-X Tile, Secondary	PRT	8 9	24 AWG, TSP
YP_TILE_P	+Y Tile, Primary	PRT	10 11	24 AWG, TSP
YP_TILE_S	+Y Tile, Secondary	PRT	12 13	24 AWG, TSP
YM_TILE_P	-Y Tile, Primary	PRT	14 15	24 AWG, TSP
YM_TILE_S	-Y Tile, Secondary	PRT	17 18	24 AWG, TSP
ZP_TILE_P	+Z Tile, Primary	PRT	19 20	24 AWG, TSP
ZP_TILE_S	+Z Tile, Secondary	PRT	21 22	24 AWG, TSP
XP_IN_SHELL_P	+X Inside Composite Shell, Primary	Thermistor	23 24	24 AWG, TSP
XP_SHELL_S	+X Inside Composite Shell, Secondary	Thermistor	26 27	24 AWG, TSP

Sensor Name	Sensor Description	Sensor Type	Pin No.	Wire Type and Guage
XM_ IN_SHELL_P	-X Inside Composite Shell, Primary	Thermistor	28	24 AWG, TSP
			29	
XM_ IN_SHELL_S	-X Inside Composite Shell, Secondary	Thermistor	30	24 AWG, TSP
			31	
YP_ IN_SHELL_P	+Y Inside Composite Shell, Primary	Thermistor	32	24 AWG, TSP
			33	
YP_ IN_SHELL_S	+Y Inside Composite Shell, Secondary	Thermistor	34	24 AWG, TSP
			35	
YM_ IN_SHELL_P	-Y Inside Composite Shell, Primary	Thermistor	36	24 AWG, TSP
			37	
YM_ IN_SHELL_S	-Y Inside Composite Shell, Secondary	Thermistor	38	24 AWG, TSP
			39	
ZP_ IN_SHELL_P	+Z Inside Composite Shell, Primary	Thermistor	40	24 AWG, TSP
			41	
ZP_ IN_SHELL_S	+Z Inside Composite Shell, Secondary	Thermistor	43	24 AWG, TSP
			44	
XM_ PMT _1R_P	-X PMT Rail, Right, Primary	Thermistor	45	24 AWG, TSP
			46	
XM_ PMT _1R_S	-X PMT Rail, Right, Secondary	Thermistor	47	24 AWG, TSP
			48	
YM_ PMT _2R_P	-Y PMT Rail, Right, Primary	Thermistor	49	24 AWG, TSP
			50	
YM_ PMT _2R_S	-Y PMT Rail, Right, Secondary	Thermistor	52	24 AWG, TSP
			53	
XP_ PMT _3R_P	+X PMT Rail, Right, Primary	Thermistor	54	24 AWG, TSP
			55	

Sensor Name	Sensor Description	Sensor Type	Pin No.	Wire Type and Guage
XP_ PMT _3R_S	+X PMT Rail, Right, Secondary	Thermistor	56	24 AWG, TSP
			57	
YP_PMT_4R_P	+Y PMT Rail, Right, Primary	Thermistor	58	24 AWG, TSP
			59	
YP_PMT_4R_S	+Y PMT Rail, Right, Secondary	Thermistor	60	24 AWG, TSP
			61	
Spare			62	24 AWG, TSP
			63	
Spare			64	24 AWG, TSP
			65	
Not Used	Pins 3, 16, 25, 42, 51, 66			

8.3. Switching characteristics timing diagram – Events and VETOs.

Any particle that generates an electrical signal above the VETO's threshold shall also force the GAFE's comparator to output a signal whose pulse duration is equal to the time the electrical signal is above the comparator's threshold. Two types of VETO signals shall be generated from the GAFE's comparator output, a VETO_AEM and a VETO_HITMAP.

8.3.1. VETO_AEM Signal Timing Characteristics

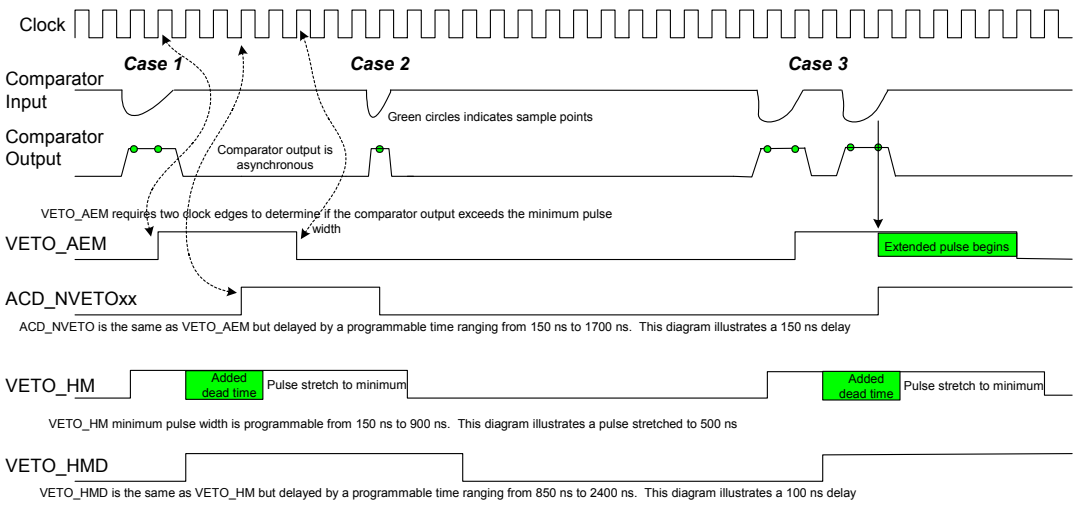
For generation of the VETO_AEM signals, the GARC shall contain digital delay lines, digital deglitch circuits and digital re-triggerable one shots. Each GAFE comparator output is first input to a digital delay line. A commandable delay tap (0 to 1550 nsec) is input to a deglitch circuit that looks for the delayed comparator signal to be present for at least two consecutive clock leading edges before a veto pulse is detected. Thus, the GARC will reject all input pulses of width less than 50 nsec, detect all input pulses of width greater than 100 nsec, and detect some and reject some pulses between 50 and 100 nsec in width. Once a pulse is detected, it fires a re-triggerable digital one-shot with width of 50 to 400 nsec (AEM commandable). The outputs of the one-shots are the ACD_NVETOxx signals. Note that for a minimum commanded delay of 0 nsec, the actual delay from discriminator input to ACD_NVETOxx output is 150 to 200 nsec (due to the synchronous circuitry) plus up to 20 nsec (due to I/O buffer and gate delays) in the GARC. For a maximum commanded delay of 1550 nsec, the actual delay from discriminator input to ACD_NVETOxx output is 1700 to 1750 nsec (due to the synchronous circuitry) plus up to 20 nsec (due to I/O buffer and gate delays) in the GARC.

8.3.2. VETO_HITMAP Signal Timing Characteristics

For generation of the VETO_HITMAP signals, the GARC uses the above delay lines with separate, commandable taps at 850 to 2400 ns. The delayed comparator pulse is stretched by 0 to 350 ns, commandable. The pulse is further stretched if necessary to meet a minimum pulse width of 150 to 900 ns, commandable. The final stretched pulse is sampled at trigger time, and read out in the event data as the hit map.

The following timing diagrams present what the VETO_AEM and VETO_HITMAP signals are for four different cases. The different cases are defined as follows:

Case 1: A charged particle event where the magnitude produces a comparator output that lasts at least 2 clock edges, but less than the VETO_AEM minimum pulse width.
Case 2: A charged particle event where the magnitude produces a comparator output that lasts less than 2 clock edges.
Case 3: Two charged particle events where each lasts at least 2 clock edges, but the second event occurs before the VETO_AEM pulse is complete.
Case 4: A charged particle event where the magnitude produces a comparator output greater than the VETO_AEM minimum pulse width.



The VETO_AEM signal is synchronized to the clock.

Figure 6 VETO Timing diagram (1)

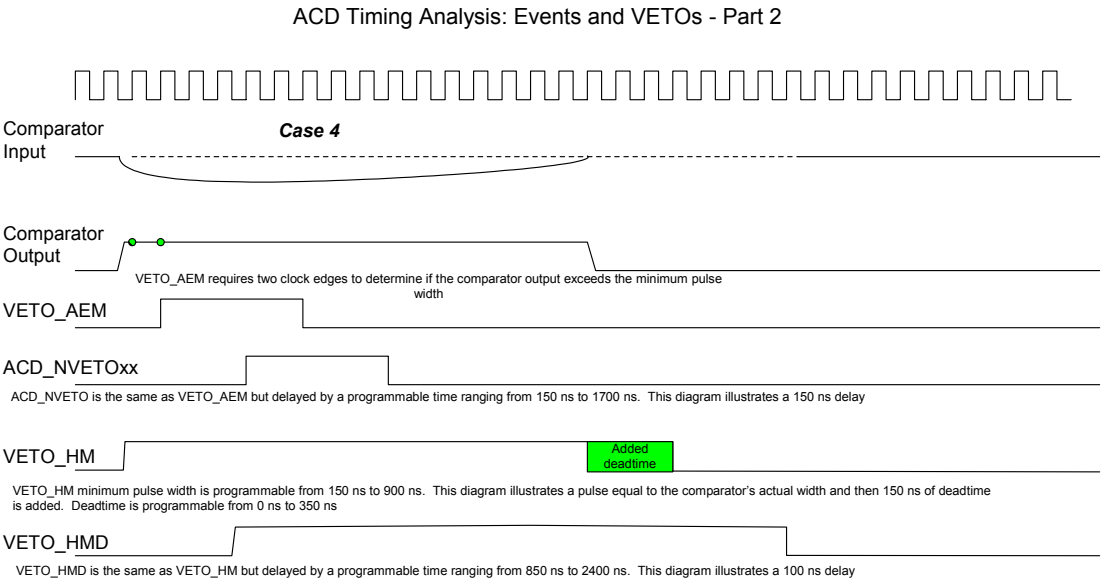


Figure 7 VETO Timing diagram (2)

8.4. Power

In each of the 24 cables, the ACD is supplied with +3.3 VDC nominal and +28 VDC nominal. All power uses redundant connector pins and wire in the cables (see Table 1). Power to the ACD is supplied on both A and B AEM connectors. A and B AEM power will be wired together at each FREE board. The AEM will handle the power switching, protection, sensing and conditioning. All power requirements are specified at the BEA interface and are listed in the following paragraphs. The requirements on the power at the AEM interface are specified in LAT-SS-0183 Level IV Power Specification Document.

Deleted: Table 1

The noise on the 3.3 volt VDD shall be less than 5mV from DC to 1.0 MHz. The maximum peak noise shall be less than 5mV. The voltage shall be regulated to voltages between 3.2 and 3.6 volts.

The ACD_28V, ACD_28RTN supplies power for the PMT HVBS. The voltage spans +28 ± 1 V. The noise shall be less than 10 mV RMS from DC to 1.0 MHz. The maximum peak noise shall be less than 10 mV. The worst-case total consumption of the 12 HVBSs shall be less than 5.0 W at 29V, maximum bus voltage. The nominal total consumption of the 12 HVBSs will be 2.4 W based on +28V bus voltage, 1 kV output and 30μA loading.

8.5. Grounding and Shielding

8.5.1. Grounding

The FREE circuit card is comprised of digital common, analog common, high voltage common and PMT common. All the commons are tied together on the FREE circuit card. See Figure 8. The FREE circuit card's common point shall be grounded to the AEM via the common mode choke on the power return lines. The FREE analog circuitry shall be shielded in a Faraday shield that is connected to the common and isolated from the chassis ground. The grounding design shall make provisions to connect the commons to chassis ground at a later date, in case performance measurements yield the need for such a connection. The concern is that if the amplifier common is not connected to the shield, capacitive coupling from the front-end board shield (which is connected to the structure), will couple noise.

8.5.2. Shielding

The cable between the FREE circuit card and the BEA shall have a shield connected to chassis ground only on the BEA because the cable is expected to be less than 12 inches long. The cable between the BEA and the LAT EMI DAQ shall have the shields connected to chassis ground at the BEA and at the DAQ EMI.

8.6. EMI/EMC

The EMI/EMC performance is specified in the LAT Environmental Specification, LAT-SS-00778.

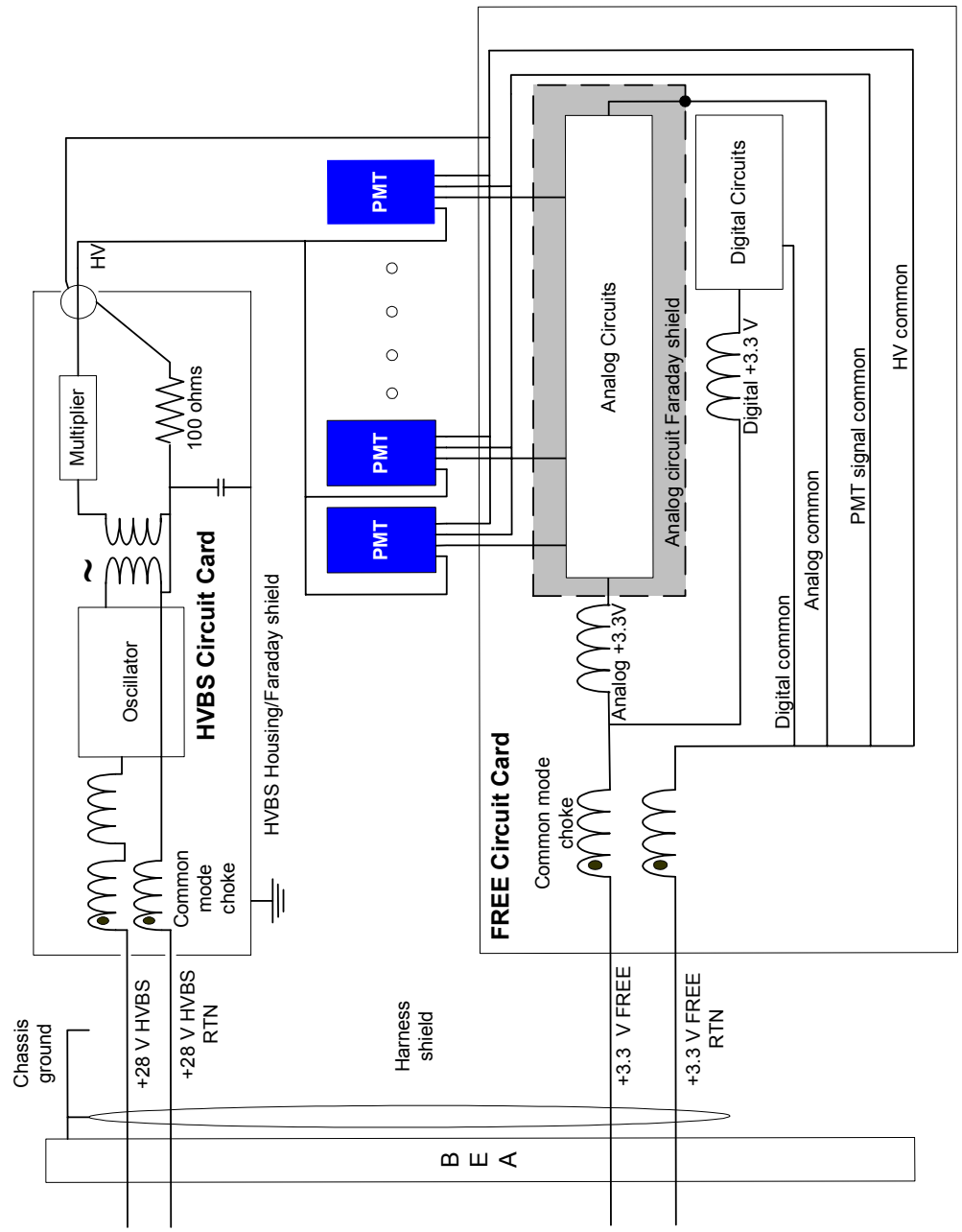


Figure 8 ACD Electronics Grounding

9. ACD Command and Data Format

All fields are MSB first (leftmost on drawings). Parity is odd. The data field is 16-bits. If a value of less than 16-bit is transferred from the AEM to the ACD, then the to-be-used bits are at the end of the field (leading zero's, the data is right justified). The same is true for data sent from the ACD to the AEM.

9.1. AEM to ACD Command Format

The AEM shall send either a trigger command or a configuration command to the ACD.

9.1.1. Trigger Command Format

Table 7 Trigger Command Format

Field	# Bits	Function
Start	1	1 for start
CMD Type Bits	2	10 to send only PHAs above threshold (TRIG_ZS) 01 to send all PHAs (TRIG_NOZS)
CMD Type Parity	1	Odd Parity over previous 2 bits (without Start bit)

9.1.2. Configuration Command Format

Table 8 Configuration Command Format

Field	# Bits	Function
Start	1	1 for start
CMD Type	2	00 for command
CMD Type Parity	1	Odd Parity over previous 2 bits (without Start bit)
GAFE/GARC Select	1	0 for GARC 1 for GAFE
GAFE/GARC Address	5	GAFE: Select which GAFE, 0x1F for all GAFE GARC: Select which function block
Read/Write	1	0 for write, 1 for read
Data/Dataless	1	0 for dataless, 1 for data, always 1 for ACD
Register/function number	4	Which register/function in the function block
CMD Parity	1	Odd parity bit over previous 15 bits
Data	16	Data Field
Data Parity	1	Odd parity bit over previous 16 bits

Note: invalid command codes are decoded as no-ops

9.1.3. Command Protocol

The logic on the cable is low-true, so that a disconnected LVDS cable (asserts high) won't result in start bits.

Three types of commands may be sent to the ACD; trigger commands, write configuration commands, and read configuration commands.

The GARC does not execute a command if a parity error is detected. If there is a command error, then the command is copied to command error register. If there is only a data-field error, then the data field is copied to command error register. If both fields are in error, then only the command field is copied. In addition, the command and/or Data ERR bit is set. Error bits are reset when readout.

9.1.4. Command Processing Times

Command processing time is defined as the time from the leading ACD_CLK edge during the NSCMD start bit to the GARC being ready to accept another command start bit. The GARC test signal LIVE is used to measure this processing time. (The LIVE signal is only accessible at a

monitoring pin inside the FREE). Readback data to the AEM is sent towards the end of the processing time.

Table 9 Command Processing Times

Command Type	Processing time in nanoseconds
All GARC Write Configuration except as noted	2000
All GARC Read Configuration except as noted	3550
Cal Pulse	2000
Reset	2000
Set HVBS DAC	5400
Read HVBS DAC	7100
GAFE Configuration Write	12250
GAFE Configuration Read	13900

9.1.5. Trigger Processing

There are three phases of trigger processing.

The Trigger detect and ADC conversion phase starts with the leading edge of ADC_CLK during the TACK start bit and ends with “data_busy” (an internal GARC signal). This takes a minimum of 10950 ns. This time is extended by the amount that Hold_Delay exceeds 2750 ns. This time is also extended by the ADC_TACQ time.

detect_convert_time = 10950 + max(0 , (Hold_Delay – 2750)) + ADC_TACQ (ns)

The Count PHA phase takes 50 ns per PHA channel up to 900 ns. Minimum time is zero ns if Max_PHA is set to zero. The GARC counts PHAs starting with channel 0 until Max_PHAs (above threshold if in ZS mode) are found or channel 17 is reached.

The data transmission phase is from the NSDATA start bit to the end of PHA transmission. There are 39 fixed bits in the event data plus 0 to 18 15-bit PHA Words.

9.2. GAFE Registers

Table 10 GAFE Registers

Reg Number	Name	Values	Default State
0	CONFIG_REG	Bit 0: GAFE3, GAFE4, GAFE 5, GAFE6: Unused	Low
		Bit 1: TCI Regular Gain Range Enable, 0=disable, 1=enable	Disable
		Bit 2: GAFE3,4,5,6: PHA Range Mode, 0=auto, 1=manual GAFE4: TCI High Range Test Charge enable, 0=disable, 1=enable	Auto on HiCal disable
		Bit 3: Range Select, 0=low, 1=high	LO
		Bit 4: Veto Discriminator Enable, 0=disable, 1=enable	Enable
		Bit 5: HLD Discriminator Enable, 0=disable, 1=enable	Enable
		Bit 6: GAFE3, GAFE 4: unused GAFE5, 6: TCI High Gain Range Enable, 0=disable, 1=enable	Disable
		Bit 7: GAFE3, GAFE 4, GAFE5: unused GAFE 6: TCI Low Gain Range Enable, 0=disable, 1=enable	Disable
		Bit 8: GAFE3, GAFE 4, GAFE5: unused GAFE6: Initial channel select, 0=high-gain, 1=low-gain	0
		Bits 15-9: Spare bits	0
1	VETO_DAC	GAFE3: 0 – 63: 3.2 to 0 nominal MIPs, steps of 0.05 MIPs GAFE4,5: 5.0 to –0.2 MIPs in steps of 0.08 MIP GAFE6: to follow	57➔0.35 .0.50[(2)]
2	VETO_VERNIER	GAFE3, GAFE6: unused GAFE4,5: 0 to –0.18 MIPs in steps of 0.003 MIP	55➔0.02

3	HLD_DAC	GAFE3: 0 – 63: 64 to 0 nominal MIPs, steps of ~1 MIP GAFE4, 5: 0 to 80 MIPs in steps of 1.2 MIP	38➔26 40
4	GAFE3-5: BIAS_DAC GAFE6:Auto-range DAC	GAFE3-5: 0 – 63 1.75 to 2.2 V, steps of 56mV GAFE6: to follow (sets lo-high auto-range switch point)	32➔1.75 V
5	TCI_DAC	0 – 63 Test charge inject level	0(4)
6	VERS_ADDR	Version Number, read only GAFE3-6	3
7	WRITE_CTR	Number of write commands since reset, read only	
8	REJECT_CTR	Number of command rejects since reset, read only	
9	LOOP_CTR	Number of commands since reset, read only	
10	CHIP_ADDR	GAFE Chip Address, read only	

Note 1: The GAFE Low Level Discriminator is not used by the FREE design. This signal was provided to zero-suppress PHA values. The PHA zero-suppress decision is instead done digitally in the GARC.

Note 2: The Default state format is: bits ➔ value

Note3: Reg 4, (BIAS_DAC) is a 6 bit register with a default of 32. Three ls bits are used by DAC.

9.3. GARC Registers

Table 11 GARC Registers

Function Block Address (5 bits)	Reg/Fct Number (4 bits)	Name	Description	Values	Initial State
0	1	Reset	Generates Reset for GARC registers and GAFE, write only	0	na
	2	Veto_Delay	Delay from Disc in to NVETO out	0-31 ➔ 150 - 1700, steps of 50 ns (see note 1)	5➔400 ns
	3	Calib	Set strobe high. Strobe is reset after trigger and PHA readout. write only	0	na
	8	HVBS	Specify normal HV Level	0-4095➔range from 0 to 1500 V (see note 2)	0
	9	SAA	Specify SAA HV Level	0-4095➔ range from 0 to 1500 V (see note 2)	0
	10	Use HV Normal	Write Sets HV DAC to Normal Level, read shift register in DAC	0	na
	11	Use HV SAA	Write Sets HV DAC to SAA Level, read shift register in DAC	0	na
	12	Hold Delay	Set Delay from Trigger (Leading edge of NSCMD) to Hold	0-127➔250-6600, steps of 50 ns	28➔1650 ns
	13	Veto Width	Pulse width of NVETO	0-7➔50-400, steps of 50 ns	2➔150 ns

Function Block Address (5 bits)	Reg/Fct Number (4 bits)	Name	Description	Values	Initial State
	14	Hitmap Width	Minimum pulse width of Hitmap Signals (GARC internal)	0-15➔150-900, steps of 50 ns	7➔500 ns
	15	Hitmap Deadtime	Time added to Hitmap signals	0-7➔0-350, steps of 50 ns	3➔150 ns
1	4	Look at Me	GARC will enable this interface, A or B, write only	60304	
	8	Hitmap Delay	Delay from Disc in to Hitmap signals	0-31➔850-2400, steps of 50 ns (see note 1)	16➔1650 ns
	9	PHA EN0 Reg	PHA readout enable, bits 15-0➔ channels 15-0 (ZS mode only)	Bit per channel	65535➔ All Enabled
	10	VETO EN0 Reg	VETO enable, channels 15-0	Bit per channel	65535➔ All Enabled
	12	PHA EN1 Reg	PHA readout enable, bits 1-0➔ channels 17 and 16 (ZS mode only)	Least significant two bits	3➔Both Enabled
	13	VETO EN1 Reg	VETO enable, channels 17 and 16	Least significant two bits	3➔Both Enabled
	15	Max PHA	Maximum number of PHA values to send	0-18	4
2	8	GARC Mode	Bit 0: Set parity for return data, 0=ODD (default), 1=EVEN Bit 1-3: HVBS A Enable, 000=Disabled (default), 111=Enabled Bits 4-6: HVBS B Enable, 000=Disabled (default), 111=Enabled Bit 7: Parity Select for GAFE Cmd, 0=ODD (default), 1=EVEN Bit 8: AEM A Veto outputs, 0=OFF, 1=ON (default) Bit 9: AEM B Veto outputs, 0=OFF, 1=ON (default) Bit 10:Control for the test pin mux (0 = HitMap_Test, 1 = live) Bit 11:Control for return data shift edge, 0=Neg Edge (default), 1=Pos Edge)		768
	9	GARC Status (read only)	Bit 0: Interface side, 0-A (default), 1-B Bit 1: HV Enable 1 (default OFF) Bit 2: HV Enable 2 (default OFF) Bit 3: Veto Enable A (default ON) Bit 4: Veto Enable B (default ON) Bit 5: ZS Status		24
	10	Command Reg	Command or data from last command error (read only)	16 bits	0
	11	GARC Diagnostic	Bit 15: parity_error Bit 14: cmd_parity_error Bit 13: data_parity_error Bit 12: cmd_error Bits 11-8: diag state loop counter Bits 7-0: valid command counter	16 bits, read only	
	12	Cmd Reject Counter	Number of Rejected Commands	8 bits, read only	0
	13	Free Board ID	Hardwired Board Serial Number	8 bits, read only	
	14	GARC Version	Version of GARC Chip	3 bits, read only	
3	8	PHA Threshold 0	PHA must exceed threshold unless send all PHAs type trigger Default of 1114 based on: baseline of 2 volts	0-4095	1114
	9	PHA Threshold 1		0-4095	1114
	10	PHA Threshold 2		0-4095	1114
	11	PHA Threshold 3		0-4095	1114
	12	PHA Threshold 4		0-4095	1114

Function Block Address (5 bits)	Reg/Fct Number (4 bits)	Name	Description	Values	Initial State
	13	PHA Threshold 5	full scale of 0.2 volts baseline 0 nominal MIPS full scale 10 nominal MIPS threshold 1 nominal MIPS Inversion of PHA values done in GARC	0-4095	1114
	14	PHA Threshold 6		0-4095	1114
4	8	PHA Threshold 7		0-4095	1114
	9	PHA Threshold 8		0-4095	1114
	10	PHA Threshold 9		0-4095	1114
	11	PHA Threshold 10		0-4095	1114
	12	PHA Threshold 11		0-4095	1114
	13	PHA Threshold 12		0-4095	1114
	14	PHA Threshold 13		0-4095	1114
5	8	PHA Threshold 14		0-4095	1114
	9	PHA Threshold 15		0-4095	1114
	10	PHA Threshold 16		0-4095	1114
	11	PHA Threshold 17		0-4095	1114
	12	ADC TACQ	ADC Acquisition Time, additional time from Hold to start of ADC clocks, see Trigger Timing	0-63 → 0-3150 ns	0

Note 1: Add 0 to 50 ns because of the asynchronous nature of the Discriminator input signal and add up to 20 ns for various propagation delays.

Note 2: The exact range and calibration curve will be provided at a later time, after the HVBS's are built.

9.4. GARC Interface Details

The GARC selects the A or B interface based on which side sent the last look_at_me command. A and B LVDS drivers for signals transmitted from the FREE to the AEM can be turned on (3.5 mA drive) and "off" (0.5 mA drive) via command. The design, characterization, testing, layout and verification of all LVDS interface circuitry are a LAT DAQ subsystem responsibility and are provided to GSFC.

9.4.1. Flip-Flop Cells, Global Clocking

The GARC and GAFE use cells from the Tanner library for all flip flop functions including DFF, DFF preset, and DFF reset. The asynchronous preset and reset are used to establish initial state and configuration values to the GARC and GAFE at power on and reset times. All flip-flop clocking is via the Tanner global clocking network with a loading setting of 4. The Tanner global reset feature is also used. Additional SEU tolerance for the high voltage enable flip-flops is achieved via triple redundancy.

9.4.2. Tanner I/O Pads

Standard Tanner I/O pads will be used by the GARC, including buffered CMOS input, buffered CMOS output, power input, ground input, and unbuffered (for the LVDS and other analog functions).

9.5. ACD to AEM Data Format

The ACD shall provide data to the AEM upon receiving either a trigger command or a read configuration command.

9.5.1. Configuration Readback Data

The ACD shall respond to the AEM's read configuration command with readback data. The data shall consist of thirty-two bits.

Table 12 Configuration Readback Data

Field	# Bits	Function
Start	1	1 for start
GAFE/GARC Select	1	Copy of write command field (0 for GARC, 1 for GAFE)
GAFE/GARC Address	5	Copy of write command field (Select which GAFE)
Read/Write	1	1 for read
Data/Dataless	1	Always 1
Register/function number	4	Copy of write command field (which register/function in the function block)
CMD Parity	1	Odd parity bit over previous 12 bits
Data	16	Data, MSB first
CMD/DATA ERROR	1	Error in parity detected
Parity	1	Odd parity bit over previous 17 bits

The CMD/Data error bit is set if command or data parity error are detected by the ACD. The states of the error bits are returned with each read command. The error bits are reset when read out.

9.5.2. Event Data

The ACD shall send event data to the AEM upon receiving a trigger command from the AEM.

Table 13 Event Data

Field	# Bits	Function
Start Bit	1	1 for start
Hit Map Bits	18	Bits 17-0 for channels 0-17, bit set if hit in channel
Zero Suppression Bits	18	Bits 17-0 for channels 0-17, bit set if PHA will be sent
CMD/Data ERROR	1	Error in command parity detected
Header Parity	1	Odd parity bit over previous 37 bits
PHA Words (quantity 0-18) Order: Channel 0 to channel 17	15	Bit 14: 1 if a PHA word is to follow Bit 13: 1 for high range, 0 for low range Bits 12-1: the PHA value, 0 to 4095 Bit 0: Odd parity over last 14 bits

The Hit Map bits indicate which channels had an active hit map signal at trigger time.

The ZS bits indicate which PHAs will be sent in the event data packet.

There are two trigger modes (Normal_Trigger and Send_All_Trigger):

Normal_Trigger: The PHA value of a channel is sent only if all the following is true:

- the channel value is above its set threshold (PHA-Threshold)
- the channel is enabled (PHA-EN)
- the number of channels sent preceding this one is less than MAX_PHA

Background: The Normal-Trigger mode is the standard mode used to read out only interesting (above PHA-Threshold) channels in order to minimize event data volume and system dead-time. If the number of values read out has a noticeable effect on the LAT system dead-time, the baseline mitigation approach is to reduce the number of values by increase of the threshold setting. Noise channels are expected to be disabled and thus do not contribute a PHA value. As a risk mitigation, in case of (unexpected) transient noise problems, MAX-PHA can be set to less than 18 to put a limit on the number of values read out. The baseline MAX-PHA setting is 18.

Send_All_Trigger: Always all 18 PHA values are sent independent of the setting of PHA-Threshold, PHA-EN, or MAX_PHA.

Background: In order to acquire baseline values for all channels during regular physics data taking, a low rate of "Send_ALL_Trigger" mode triggers are transmitted to the ACD system. For these triggers, it is expected that the read out of the 18 PHA values may result in LAT system dead-time. However, the LAT trigger system will keep the frequency of these "Send-All-Trigger" mode triggers low enough so that the ACD contribution to the integrated LAT system dead-time is negligible while still providing enough baseline PHA values to be able to monitor the ACD channels.

The "Zero-Suppress-Bit' field identifies the channels for which a PHA value is present in the PHA word field. This is true for either trigger mode. So for each Send_All_trigger all 18 bits are set in the Zero-Suppress bit field.

PHA_EN bits are used only for normal_trigger. PHAs are sent regardless of PHA_EN for Send_All_PHAs trigger.

The condition of no PHA words sent can be detected by 15 zero bits after the Header Parity. Otherwise, at least one of the 15 bits will be set.

10.ACD Tile Numbering Scheme

The numbering scheme serves several purposes. In software, the numbering scheme is used for storing the information about an event (both simulation and real data) and it is also used in the reconstruction and analysis. In hardware, the numbering scheme is used in the design, fabrication and test.

The numbering of the five faces of the ACD is defined in as follows. Face 0 is in front of the TKR, and is sometimes called the "top" or the "hat". The side faces are numbered (1,2,3,4) for the (-X, -Y, +X, +Y) faces, respectively. The ACD is shown Figure 8, unfolded for a two-dimensional representation.

A matrix numbering scheme is used for calculating nearest neighbors or other analyses. A four-digit matrix number uniquely specifies a tile and PMT. The least significant digit gives the column number, the next digit gives the row number, and the next digit gives the face number, as shown in Figure 8. The side rows are numbered from the front backward and the side columns are numbered along the respective (+X, +Y) axis. The most significant digit specifies the tile mapping to a PMT channel on a FREE card. The primary PMT channel is 0 and the secondary PMT channel is 1. Each tile has two PMTs (primary, secondary) that are mapped to two channels on different FREE cards.

A three-digit alphanumeric identifies each FREE Card. The least significant digit defines a primary "A" or secondary "B" board, the next digit defines the left "L" or right "R" side of the ACD face, and the next digit defines the face of the ACD where the boards are located. Figure 8 shows the PMT locations on the ACD.

The ACD also has eight fiber ribbons, each connected to two PMTs (primary, secondary). The four-digit number also uniquely specifies the fiber ribbon and PMT; however, the definition of this number is different from the tile numbering definition. The two least significant form a sequential number of fiber ribbons (00-03) along either the X-axis or Y-axis. The next digit defines the axis, X is 5 and Y is 6. The most significant digit specifies the fiber ribbon mapping to a PMT channel on a FREE card. The primary PMT channel is 0 and the secondary PMT channel is 1. Each fiber ribbon has two PMTs (primary, secondary) that are mapped to two channels on the FREE cards.

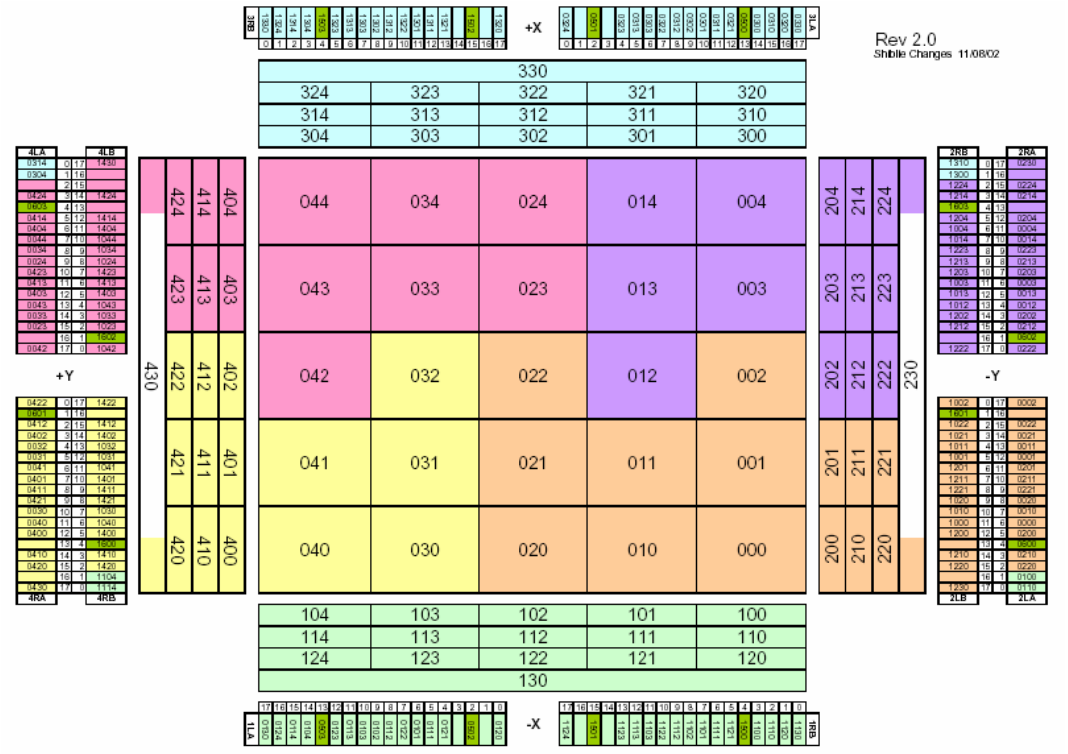


Figure 8. ACD Tile Numbering Scheme

11.Thermal Interface and Heat Transfer

The ACD has three thermal interfaces. First, the ACD-Grid interface is the primary means for conductive heat transfer. The second interface is the radiative thermal coupling to the outer space environment, through the MLI surrounding the ACD. The final interface is the radiative thermal interface between the inside surface of the ACD and the Tracker modules and Grid.

The LAT orbit altitude is a 450 Km, minimum, to 575 Km, maximum. The orbit inclination is 28.5 deg. The ACD shall use the on-orbit thermal environment heat flux values and SC thermal interface definitions as listed in the LAT-SC IRD, 433-IRD-0001.

11.1. ACD Temperature Requirements

The ACD shall meet the temperature requirements as listed in Table 14 and the LAT Environmental Specification, LAT-SS-00778.

Table 14. ACD-LAT Interface Temperature Ranges

State	Grid Int Tmin (degC)	Grid Int Tmax (degC)	Min TKR Temp (degC)	Max TKR Temp (degC)
Operating	-13	20	-10	25
Survival	-15	30	-20	30

No ACD hardware shall be tested above 45°C.

The cold case analysis for ACD efficiency uses an average tile temperature of -17°C.

11.2. LAT Interface Temperature Requirements

The LAT Grid and the LAT thermal control system shall maintain the ACD within the temperatures shown Table 14 and in the LAT Environmental Specification, LAT-SS-00778.

11.3. Temperature Rate of Change

Temperature transitioning of a component or its mounting interface may induce or subject a component to harmful stresses. Temperature transitioning is caused by the on-orbit environment, component startup and operation. In addition, temperature transition is induced during component and observatory thermal vacuum testing. Unless otherwise specified the component supplier shall assume that the maximum rate of change of any component or mounting interface when integrated to the observatory shall be no greater than 30°C/hr during integration and testing.

11.4. Power Dissipation

The maximum heat dissipated in the ACD during normal operating conditions shall be no greater than ~16 watts. The maximum orbit-average heat dissipated in the ACD during normal operating conditions shall be no greater than 11 watts.

The heat dissipation within the ACD shall be stable to within +/- 2 watts of the nominal during operations.

11.5. ACD-LAT Bolted Joint Interface

The bolted joint interface with the Grid shall be the primary mechanism for transferring heat into and out of the ACD. See the ACD-LAT IDD, LAT-DS-00309 for details.

The net heat transfer from the ACD to the LAT will be:

Qnet-hot = -5 W
Qnet-cold = -25 W

11.6. Multi-Layer Insulation

Thermal Multilayer Insulation (MLI) blankets shall be used to regulate radiant heat transfer between the observatory and its external environment. The following sections document ACD MLI blanket construction, electrical grounding, locations, and venting.

ACD MLI blankets shall be constructed of 6 to 18 inner layers of 1/4 mil thick mylar aluminized on both sides, each separated by a layer of dacron netting. The entire blanket assembly shall be sandwiched between a 3 mil thick Germanium Black Kapton (with scrim) sheet and a 1 mil thick VDA Kapton sheet.

The micrometeoroid shield and MLI blanket cover the ACD per drawing LAT-DS-00309, LAT-ACD IDD. The ACD MLI shall have an effective thru emittance, e* where 0.01 <e*<0.03. High emissivity(>0.78), low alpha(<0.55) on outer layer MLI blankets

The ACD MLI blanket shall be grounded at the Grid per drawing LAT-DS-01151, LAT-ACD Outline Drawing. The blanket shall be grounded at eight locations, two per side. The thermal blanket is currently assumed to end at the bottom of the ACD.

11.7. ACD Thermal Coatings

Thermal coatings shall be used to obtain thermo-optical properties that are required in the thermal design of the ACD. The use of any thermal coating must have prior approval from the electrical, materials, and thermal subsystems. The locations and thermal coatings to be used on the ACD are presented in Table 15.

Deleted: Table 14

Table 15 ACD Coatings

	Coating	MLI	MLI Out/In	High emissivity
ACD Shell	Non-coated M46J (inner and outer facesheets)	Covering all sides	Ge Black Kapton/VDA Kapton	> 0.8

ACD BFA	Black Anodize	Covering all sides	Ge Black Kapton/VDA Kapton	> 0.8

11.8. Tracker Surface Property Assumptions

The inside surface of the ACD and the tracker towers and grid are radiatively coupled. For the purpose of LAT and ACD thermal analysis, the following tracker tower and grid surface property assumptions can be made:

Tracker Tower - Black anodize or black paint with $0.8 < \text{emissivity} < 0.9$

Grid - Black Anodize with emissivity BOL = 0.82, EOL = 0.78

12.Electrical Packaging Interfaces

12.1. Cable and Connector Definitions

Cable and connector definitions are given in Section 8 of this document and the connector locations are shown on the ACD Outline Drawing, LAT-DS-01151.

12.2. Cable Routing and Support

Cable routing and cable support is detailed in the ACD Outline Drawing, LAT-DS-01151.

13.Integration and Test Interfaces

13.1. Integration Stay-Clears and Access Requirements

The ACD shall be integrated to the LAT vertically, from above.

The ACD shall be capable of being de-integrated from the Grid at any time. The de-integration of the ACD from the LAT will not require disassembly or invalidating verification of any other subsystem. Once the ACD is reintegrated, the only regression testing required is a limited electrical test to verify the ACD-LAT cable mates.

The MLI micrometeoroid shield shall either be integrated after the ACD, or its bottom skirt shall be able to be folded up onto the ACD during and after integration, to provide access to the LAT region under the ACD stay-clear. However, the MLI micrometeoroid shield currently ends at the bottom of the ACD BEA making this unnecessary in most instances.

The LAT will be supported at the Grid corners, with a frame that stays outside of the ACD useable envelope, as defined in the ACD-LAT IDD, LAT-DS-00309.

13.2. Provision for Surveying

Refer to the LAT I&T Survey and Alignment Plan, LAT-MD-01586 and the ACD-LAT IDD, LAT-DS-00309 for details of surveying, alignment, datum structure, and fiducial locations.

13.3. Instrumentation

Flight and test instrumentation (thermistors, thermocouples, accelerometers, strain gauges, etc.) used during test are defined in the LAT Instrumentation Plan, LAT-TD-00890 and the ACD Integration and Test Plan, LAT-TD-00430.

13.4. Integration GSE

ACD lifting and integration fixtures shall not violate the ACD's useable envelope as defined in the ACD-LAT IDD, LAT-DS-00309. ACD lift interface zones with allowable force and moment vectors are defined in the ACD-LAT IDD, LAT-DS-00309. During ACD integration, no GSE that would intrude in the ACD's usable envelope shall be mounted on top or on the sides of the Grid.

The Multi Purpose Lift Sling used for ACD integration at GSFC will be difficult to use during LAT integration due to height limitations. LAT I&T is responsible for the design, manufacture and proof test of the lift fixture for LAT-ACD integration at SLAC.

Note: Due to crane hook height limitations at the SLAC integration hall, it is not possible to use the Multi Purpose Lift Sling used for ACD integration at GSFC during LAT integration. For further clarification, details of the ACD sling used at GSFC are captured in the ACD Mechanical Ground Support Equipment document, ACD-REQ-7002.

13.4.1. ACD Provided GSE

Development, fabrication, test, and delivery of the following mechanical ground support equipment:

Lifting harnesses, shackles, and any other temporary hardware needed to support the ACD during integration on the LAT.

Handling Dolly to the support and move the ACD prior to integration to the LAT.

Any needed drill templates/pin templates.

Micrometeoroid shield/thermal blanket removal tools if needed.

ACD multi purpose test fixture.

Hydraset capable of manipulating ACD if needed.

Helium monitoring equipment with sufficient documentation and training for operation.

13.4.2. LAT Provided GSE

Development, fabrication, and test of the following components:

Crane for lifting the ACD with its lifting fixture. Capacity->290 Kg.

Lifting fixture for the ACD to be used at SLAC. Design factor of safety shall be >3 times against minimum material yield strength.

LAT will provide enough information for ACD to manufacture a Grid simulator for testing purposes.

14.Other Interfaces

14.1. Venting

During launch, air from the ACD shall be vented outward, away from the inside of the LAT. No ACD venting shall be allowed into the volume surrounding the TKR modules or down past the Grid perimeter.

14.2. Particulates and Other Contamination

The ACD shall contain all fracture-sensitive materials such that any particulates produced by a fracture are contained within the stay-clear volume of the ACD.

The ACD shall prevent any venting or shedding of particulates down, or out the bottom of its stay-clear, to avoid possible contamination of the spacecraft star tracker.

The ACD is sensitive to Helium and must be protected from concentrations greater than 5 parts per million, which is approximately the normal atmospheric concentration. Helium monitoring is required twice a week and whenever the ACD is moved to a new location. If the ACD is in a building with recirculated air and the building contains a source of helium then daily monitoring is required. All monitoring equipment shall be provided by the ACD subsystem.