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	Responsible Engineer(s) Michael Amato, George Shiblie, D. Sheppard	Supersedes None
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Gamma-ray Large Area Space Telescope

(GLAST)

Large Area Telescope (LAT)

Anticoincidence Detector (ACD)

Subsystem Verification Table/Plan

Draft 5

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Dave Thompson
ACD Instrument Scientist — Date

Bob Hartman
ACD Instrument Scientist — Date

Michael Amato
ACD System Manager — Date

George Shiblie
ACD Systems Engineer — Date

Tom Johnson
ACD Instrument Manager — Date

Ken Segal
ACD Mechanical Lead — Date

Glenn Unger ACD Electrical Lead	Date
Dave Sheppard ACD Electrical	Date
Jim La ACD I&T	Date

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1 PURPOSE

This document identifies and tracks the status of all of the tests needed to verify the level IV requirements for the GLAST Large Area Telescope (LAT) Anticoincidence Detector (ACD). This document also contains the test matrix that shows the tests that major ACD subsystems and components go through.

2 SCOPE

This specification captures the methods, status and procedures used to verify GLAST LAT requirements for the ACD. This encompasses the subsystem level requirements and the design requirements for the ACD. The document contains two major sections. The first section has the verification table. The second section has the test matrix.

3 SYSTEM DESCRIPTION AND DEFINITIONS

3.1 System Description

The LAT science instrument consists of an Anticoincidence Device (ACD), a silicon-strip detector tracker (TKR), a hodoscopic CsI calorimeter (CAL), and a Trigger and Dataflow system (T&DF). The principal purpose of the LAT is to measure the incidence direction, energy and time of cosmic gamma rays. The measurements are streamed to the spacecraft for data storage and subsequent transmittal to ground-based analysis centers. Signals produced by the ACD are used by the T&DF system to identify cosmic ray electrons and nuclei entering the instrument.

The ACD detects energetic cosmic ray electrons and nuclei for the purpose of removing these backgrounds. It is the principle means for detection of that background. This detector array covers the top and 4 sides of the TKR. It consists of an array of 89 plastic scintillator tiles (25 on the LAT top, 16 on each of the 4 sides, various sizes), plus 8 scintillating fiber "ribbons" that cover the gaps between the tiles. Each scintillator tile is read by 2 PMT's (baseline: Hamamatsu R4443; designated "A" and "B") via waveshifting fibers (and in some cases, clear optical fiber extensions).

The PMT's and the ACD electronics will be located around the base of the ACD, in the Base Electronics Assembly (BEA). The 50 waveshifting fiber bundles and associated clear fiber extensions from the ACD Top will be routed down 2 opposite sides of the ACD (24 and 26), so that those two sides of the BEA will be more heavily populated than the remaining two sides. Each assembly of one tile plus the two associated waveshifting fiber bundles and clear fiber extensions denoted as a Tile Detector Assembly (TDA).

On each of the two opposite LAT sides (±Y) that contain LAT radiators, the BEA will house two ACD electronics boards, one for "A" PMT's and one for "B" PMT's. On each of the remaining two LAT sides (non-radiator), the BEA will house four ACD electronics boards, two associated with "A" PMT's and two associated with "B" PMT's. Each ACD electronics board will be capable of servicing 18 PMT's, although they will vary with regard to numbers of unused electronics channels. All 12 of the ACD electronics boards are nominally identical.

Each ACD electronics board will receive power from redundant high voltage bias supply (HVBS), which is capable of providing the necessary high voltage for all 18 associated PMT's. All 18 PMT's associated with a specific board will receive the same high voltage.

Each ACD electronics board will contain 18 channels of analog, analog-to-digital, and digital processing electronics, as well as command reception and distribution logic and data collection and transmission logic.

Each ACD electronics board interfaces to the LAT via the ACD Electronics Module (AEM). The AEM receives all signals and data from the ACD and sends commands to the ACD. All digital communications between the ACD and the AEM will be via standard LVDS protocol.
Science signals from the TDA's and their associated PMT's are defined in terms of MIP's, the signal generated by a minimum-ionizing singly-charged particle traversing a tile in a direction normal to its surface. To provide a meaningful electronics specification, the definition of a MIP must be normalized to the electrical charge delivered by each of the two PMT's in response to a MIP. The following parameters are assumed for the MIP calculation:

10 photoelectrons per PMT per MIP

PMT gain of 400,000

The result is that **1 MIP** produces a PMT anode signal of **0.64 pC**.

3.2 Acronyms

ACD - Anticoincidence Detector
AEM – ACD Electronics Module
FOV – Field of View
FREE – FRont End Electronics
GLAST – Gamma-ray Large Area Space Telescope
HLD – High Level Discriminator
IOC – Instrument Operations Center
IDD – Interface Definition Drawing
IRD – Interface Requirements Document
LAT – Large Area Telescope
LET – Linear Energy Transfer
MIP – Minimum Ionizing Particle (see definition below)
MSS – Mission System Specification
PI – Principal Investigator
PMT – Photo Multiplier Tube
SEU – Single Event Upset
SAS – Science Analysis Software
SI/SC IRD – Science Instrument – Spacecraft Interface Requirements Document
SRD – Science Requirements Document
SSC – Science Support Center
TACK – Trigger ACKnowledge

TBD - To Be Determined
TBR – To Be Resolved
TCI – Test Charge Injection

3.3 Definitions

The following abbreviations and definitions apply within the context of this document:

Flt – Flight
Proto - Prototype
Qua - l Qualification
Vib - Vibration

μsec, μs – Microsecond, 10^{-6} second

Acceptance Tests: The validation process that demonstrates that hardware is acceptable for flight. It also serves as a quality control screen to detect deficiencies and, normally, to provide the basis for delivery of an item under terms of a contract.

Analysis – A quantitative evaluation of a complete system and /or subsystems by review/analysis of collected data.

Background Rejection – The ability of the instrument to distinguish gamma rays from charged particles.

Backsplash – Secondary particles and photons originating from very high-energy gamma-ray showers in the calorimeter giving unwanted ACD signals.

cm – centimeter

Contamination: The presence of materials of molecular or particulate nature that degrade the performance of hardware.

Cosmic Ray - Ionized atomic particles originating from space and ranging from a single proton up to an iron nucleus and beyond.

Dead Time – Time during which the instrument does not sense and/or record gamma ray events during normal operations.

Demonstration – To prove or show, usually without measurement of instrumentation, that the project/product complies with requirements by observation of results.

eV – Electron Volt

Electromagnetic Compatibility (EMC): The condition that prevails when various electronic devices are
performing their functions according to design in a common electromagnetic environment.

Electromagnetic Interference (EMI): Electromagnetic energy that interrupts, obstructs, or otherwise degrades or limits the effective performance of electrical equipment.

Field of View – Integral of effective area over solid angle divided by peak effective area.

Functional Tests: The operation of a unit in accordance with a defined operational procedure to determine whether performance is within the specified requirements.

GeV – Giga Electron Volts. 10^9 eV

Hardware: As used in this document, there are two major categories of hardware as follows:

a. **Prototype Hardware**: Hardware of a new design which is subjected to a design qualification test
program. It is not intended for flight.

b. **Flight Hardware**: Hardware to be used operationally in space. It includes the following subsets:

(1) **Protoflight Hardware**: Flight hardware of a new design; it is subject to a qualification test
program that combines elements of prototype and flight acceptance validation; that is, the
application of design qualification test levels and duration of flight acceptance tests.

(2) **Follow-On Hardware**: Flight hardware built in accordance with a design that has been qualified either as prototype or as protoflight hardware; follow-on hardware is subject to a flight acceptance test program.

(3) **Spare Hardware**: Hardware the design of which has been proven in a design qualification test program; it is subject to a flight acceptance test program and is used to replace flight hardware that is no longer acceptable for flight.

(4) **Re-flight Hardware**: Flight hardware that has been used operationally in space and is to be reused in the same way; the validation program to which it is subject depends on its past performance, current status, and the upcoming mission.

Inspection – To examine visually or use simple physical measurement techniques to verify conformance to specified requirements.

Level of Assembly: The following levels of assembly are used for describing test and analysis configurations

a. **Part**: A hardware element that is not normally subject to further subdivision or disassembly without destruction of design use. Examples include resistor, integrated circuit, relay, connector, bolt, and gaskets.
b. **Subassembly**: A subdivision of an assembly. Examples are wire harness and loaded printed circuit boards.
c. **Assembly**: A functional subdivision of a component consisting of parts or subassemblies that perform functions necessary for the operation of the component as a whole.
d. **Component or Unit**: A functional subdivision of a subsystem and generally a self-contained combination of items performing a function necessary for the subsystem's operation. Examples are TKR tower, CAL logs, ACD tiles, electronic boxes, e.g., GASU power supplies, SIU, etc. For the purposes of this document, "component" and "unit" are used interchangeably.
e. **Subsystem**: A functional subdivision of a payload consisting of two or more components. Examples are Structure, TKR, CAL, ACD, Electronics. Also included as subsystems of the payload are the science instruments or experiments.
f. **Instrument**: A spacecraft subsystem consisting of sensors and associated hardware for making measurements or observations in space. For the purposes of this document, the LAT and GBM are considered to be instruments.
g. **Observatory**: See Payload.
h. **Payload**: An integrated assemblage of modules, subsystems, etc., designed to perform a specified mission in space. For the purposes of this document, Payload, Observatory, and Spacecraft are used interchangeably.
i. **Spacecraft**: See Payload.

MeV – Million Electron Volts, 10^6 eV

Minimum Ionizing Particle (MIP) – The mean signal from cosmic ray produced air shower muons at sea level normally incident on a scintillator tile. It corresponds to approximately 1.9 MeV per cm of scintillator.

nsec, ns – Nanosecond, 10^{-9} second

ph – photons

Protoflight – see hardware

Qualification Test - Tests intended to demonstrate that the test item will function within performance specifications under simulated conditions more severe than those expected from ground handling, launch, and orbital operations. Their purpose is to uncover deficiencies in design and method of manufacture. They are not intended to exceed design safety margins or to introduce unrealistic modes of failure. The design qualification tests may be to either “prototype” or “protoflight” test levels.

Redundancy (of design): The use of more than one independent means of accomplishing a given function.

s, sec – seconds

Simulation – To examine through model analysis or modeling techniques to verify conformance to specified requirements

Testing – A measurement to prove or show, usually with precision measurements or instrumentation, that the project/product complies with requirements.

Thermal-Vacuum Test: A test conducted to demonstrate the capability of the test item to operate satisfactorily in vacuum at temperatures based on those expected for the mission. The test, including the gradient shifts induced by cycling between temperature extremes, can also uncover latent defects in design, parts, and workmanship.

Validation – Process used to assure the requirement set is complete and consistent, and that each requirement is achievable.

Verification – Process used to ensure that the selected solutions meet specified requirements and properly integrate with interfacing products.

VETO - The signal from an individual ACD scintillator tile that indicates an energy deposit of at least ~0.3 MIP (~500 keV) in an ACD scintillator tile, or about 20% of that amount in one of the scintillating fiber ribbons. This threshold is set to be exceeded for a very high fraction of MIPs in the presence of all fluctuations in their energy deposit in the scintillator tiles. The VETO signals from individual tiles and ribbons are combined with information from the tracker and calorimeter to decide whether or not to reject events as background.

3.4 APPLICABLE DOCUMENTS

Documents that are relevant to the development of the ACD concept and its requirements include the following:

LAT-SS-00016, LAT ACD Subsystem Specification - Level III Requirements,

LAT –SS-00352 “LAT ACD Subsystem Spec – Level IV Requirements/Specifications”

LAT-GE-00009, “LAT Science Requirements Document–Level II Specification”, August 6, 2000.

LAT-SS-00010, “GLAST LAT Performance Specification”, August 2000

LAT-SS-00047, “LAT Mechanical Performance Specification”

LAT-SS-00363, “ACD Mechanical, Thermal, and Front End Electronics to ACD Electronics Module Interface Control Document”

LAT-TD-00430, “LAT ACD Assembly, Integration, and Test Plan”

LAT-MD-00408, “LAT Instrument Performance Verification Plan”

GSFC 433-MAR-0001, “Mission Assurance Requirements (MAR) for Gamma-Ray Large Area Telescope (GLAST) Large Area Telescope (LAT)”, June 9, 2000.

“GLAST Large Area Telescope Flight Investigation: An Astro-Particle Physics Partnership Exploring the High-Energy Universe”, proposal to NASA, P. Michelson, PI, November, 1999.

4 Verification Approach and Systems Performance Assurance

The verification strategy will test, analyze (may include modeling/simulation), inspect, or demonstrate all requirements to ensure that the instrument meets the requirements of this specification.

4.1 The protoflight approach

ACD primarily uses a protoflight qualification approach. Generally this means there is no prototype ACD unit that is used for qualification but not intended for flight (i.e prototype approach). However, ACD does use some prototypes or engineering models for qualification of some subassemblies. Protoflight hardware is flight hardware of a new design; it is subject to a qualification test program that combines elements of prototype and flight acceptance validation; that is, the application of design qualification test levels and duration of flight acceptance tests.

ACD (and any LAT Protoflight units and components) will be subjected to individual qualification programs which may vary slightly from LAT-MD-00408, LAT Program Instrument Performance Verification Plan. In fact the previous statement comes directly from that document. This will result in the production of qualified flight hardware.

4.2 Required Documentation

The GLAST Program requires the following documents to delineate the processes and procedures for the verification and test of LAT hardware and software.

4.2.1 Requirements Documents

Each article of flight hardware or software developed for the LAT must have traceability to a requirements document that details the performance specifications of the article. Any tests which are performed for the GLAST program must reference a requirements document.

All components, units, subsystems and the LAT itself must be tested against a released performance specification. This specification must contain requirements for verification to determine acceptable performance.

4.2.2 Test Plans

All testing or analysis that provides verification of a requirement for the LAT program must be contained in a test plan. The test plan must provide the following information:

- Test plan objectives
- Performance requirements being met by test
- Verification method for each requirement
- Table of environmental test limits for each test
- Specifications to be tested
- Purpose and description of tests to be performed
- Facility requirements
- Data collection and test records
- Test configuration
- Limitations
- Analysis activities

4.2.3 Verification by Analysis

When a requirement is verified by analysis, the test plan must include the supporting information of the analytical verification. This material shall include the analysis objective, descriptions of mathematical models and any assumptions made. The expected output must also be identified for use in evaluation of results. The test plan will show traceability to Mission Assurance Requirements contained in 433-MAR-001 (through level 2, 3 and 4 requirements) for tests performed.

4.2.4 Test Procedures

Each article of flight hardware or software tested for the GLAST/LAT program will use released test procedures. These test procedures will be under configuration management and subject to review and acceptance by subsystem engineering, systems engineering and mission assurance.

Test procedures will include the following information as well as the necessary steps and operations to gather data in a repeatable fashion for a given test article. Test procedures for the LAT program will contain:

- Purpose
- Scope
- Applicable documents
- Test Support requirements
    - Environment
    - Equipment
    - Systems Assurance
    - Quality Assurance Provisions
    - Safety
    - Special Requirements
    - Certifications
- Test Performance Requirements

- Test Configuration & set-up
- Test Performance Procedure
- Test Data Records & Data Sheets

The Test Performance Requirements include test readiness conditions, support personnel requirements, test environmental conditions, and required test equipment..

5 Verification

5.1 Verification Table

The following table lists the verification method, procedure and status for every lowest level GLAST ACD requirement, which are almost exclusively level IV requirements. Refer to the ACD Configuration Management system for test procedures and other I&T documents.

Table 1. ACD Verification Table

ID	*LAT ACD Subsystem Level IV Requirements and Verification Table, LAT-SS-00352*	*Verification Method*	*Verification Procedure*	*Verification Rationalel/Comment*	*1st time or dvlpmnt procedure*
ACD4-25	5.2 Charged Particle Detection				
ACD4-26	The ACD shall produce both fast and logic (hitmap) VETO signals in response to PMT signals resulting from charged particles traversing the ACD tiles and ribbons.	Test	ACD Comprehensive Performance Test (CPT) (ACD-PLAN-000038)	Muons test	
ACD4-27	5.3 Adjustable Threshold on VETO Detection of Charged Particles				
ACD4-28	The threshold for detecting charged particles shall be adjustable from 0.064 to 1.28 pC (0.1 to 2 MIP), with a step size of $\leq$0.032 pC (0.05 MIP).	Test	ACD CPT (ACD-PLAN-000038) FREE Functional Test (ACD-TBD-XX)	The FREE Functional will characterize the adjustable threshold to the spec step size. The CPT will test this adjustabililty with the TCI circuit, however, it currently doesn't have the resolution to fully test this function.	
ACD4-29	5.4 False VETO due to Electrical Noise				
AC	The total ACD false VETO trigger rate	Analysis	ACD CPT	Set threshold to 0.15 MIP	

D4-30	due to noise shall be less than 10 kHz (~46Hz per channel) at 0.096 pC (0.15 MIP) threshold (assuming 1 us VETO pulses).	Test Simulation	(ACD-PLAN-000038)	and then reduce HVBS output until VETO count rate no longer decreases. The resulting VETO rate is the false trigger rate due to noise.	
AC D4-31	5.5 High-Threshold Detection				
AC D4-32	The ACD shall detect pulses due to highly-ionizing particles (carbon-nitrogen-oxygen or heavier nuclei), which produce signals from 31.2 - 200 MIP (20 pC to 128 pC) with a goal of 1000 MIP (640 pC). The ACD is required to detect, via the High-Level Discriminator (HLD), all signals above the High-Level threshold (nominally 25 MIP's); it is required to digitize (PHA) signals up to 200 MIP's (128 pC). The current design actually allows for digitization of signals up to 1000 MIP's (640 pC). Each ACD electronics board shall OR up to 18 HLD outputs (selected via command) to generate a single HLD_OR signal for transmission to the AEM.	Test Simulation	ACD CPT (ACD-PLAN-000038) up to ~64 MIP FREE Functional Specialty Test (ACD-TBD-XX) from 64 to 200 MIP, no req to fully test above 200 MIP. GAFE Simulations and analysis	200 to 1000 MIP will be tested in a basic way. The specialty test should not be tested on all FREE boards. This will change if SLAC implements full high-range TCI.	
AC D4-34	5.6 Adjustable High-Threshold				
AC D4-35	The High-Level Threshold shall be adjustable for PMT signals from 12.8 to 40.96 pC (20 to 64 MIP) in steps of 0.64 pC (1 MIP) ±20%.	Test	ACD CPT (ACD-PLAN-000038) FREE Functional Test (ACD-TBD-XX)	The FREE Functional will characterize the adjustable threshold to the spec step size. The CPT will test this adjustabililty with the TCI circuit, however, it might not have the full range to test this function. This will change if SLAC	

				implements full high-range TCI.	
AC D4-36	5.7 Level 1 Trigger Acknowledge (TACK)				
AC D4-37	The ACD electronics shall accept from the AEM a Level 1 Trigger Acknowledge signal and respond by digitizing and latching data.	Test	ACD CPT (ACD-PLAN-000038)		
AC D4-38	5.8 Signals				
AC D4-39	5.8.1 Fast VETO (VETO_AEM) Signal Latency				
AC D4-40	The fast VETO signal latency shall be 100<tlatent<600 nsec from the time of particle passage. The time jitter in the VETO pulses shall be <200 ns relative to particle passage. ('Deglitch' circuit raised min latency to 100 nsec from 50 nsec).	Test	FREE Functional Test (ACD-TBD-XX)		
AC D4-41	5.8.2 Fast VETO (VETO_AEM) Signal Width				
AC D4-42	The fast VETO output signal shall have a commandable width of 50 – 400 nsec, after 'de-glitching' on 2 successive clock pulses. The leading and trailing edges must be synchronous with clock pulses.	Test	FREE Functional Test (ACD-TBD-XX)	A limited verification of this requirement can be tested in the CPT. We may be able to fully test this requirement in CPT. Comment by Bob Hartman.	
AC D4-43	5.8.3 Fast VETO (VETO_AEM) Retriggering				
AC D4-44	The Fast VETO discriminator shall be capable of retriggering less than 50 ns after the trailing edge of the VETO output signal.	Test	FREE Functional Test (ACD-TBD-XX)	A limited verification of this requirement can be tested in the CPT.	
AC D4-45	5.8.4 Logic VETO (VETO_Hitmap) Signal				
AC	A map of VETO signals shall be	Test	Hitmap		

D4-46	generated for each TACK, indicating which ACD PMT's produced signals above their thresholds within ~200 ns of the time of the event causing the TACK. (Note: The ~200 ns window is required because of time jitter in the TACK signal).		Syncronization Test (ACD-TBD-XX) ACD CPT ((ACD-PLAN-000038)		
AC D4-47	5.8.5 Logic VETO (VETO_Hitmap) Signal Latency				
AC D4-48	In response to a TACK, the map of VETO signals shall be latched by the time the ADC conversions are complete.	Test	GARC Functional Test (ACD-TBD-XX)	This test will likely be a subset of the FREE Functional Test	
AC D4-49	5.8.6 High-Threshold Signal Latency				
AC D4-50	A highly-ionizing particle hitting the top or upper side row of tiles of the ACD shall produce a High-Threshold fast signal that will be delivered to the AEM with latency of no more than that the latency as defined for the fast VETO in specification 5.8.1. Command-selected signals out of the eighteen (18) High-Threshold fast signals generated on a single electronics board shall be OR'ed to produce a single signal for transmission to the AEM.	Test	ACD CPT(ACD-PLAN-000038) GAFE Functional Test (ACD-TBD-XX)	The CPT will test to the upper limit of the TCI circuit. The GAFE Functional will test for the full range of the design (up to 1000 MIPs) Cannot test because we have no source of highly-ionizing particles.	
AC D4-51	5.8.7 Discriminator Masking				
AC D4-52	Each ACD electronics board shall have the capability to disable any combination of the Fast VETO and HLD discriminator outputs. This is to mask unused HLD signals, unpopulated veto channels, and signals due to channel failure.	Test	ACD CPT (ACD-PLAN-000038)		
AC D4-53	5.8.8 5.8.8 ACD Trigger Primitives				

ACD4-54	This requirement deleted for ACD. The ACD will produce no trigger primitives internally. The VETO signals caused by the individual PMT's will be transmitted to the AEM, where they will be OR'ed together (for each tile or ribbon), and used by the AEM to generate trigger primitives.		N/A	This is a requirement on the AEM.	
ACD4-55	5.9 ACD Performance Monitoring				
ACD4-56	The AEM will scale and telemeter count rates for ACD VETO and HLD signals, as well as various trigger primitives. ACD voltages and currents will be monitored by the AEM.	Test	ACD CPT (ACD-PLAN-000038)	This is a requirement on the AEM.	
ACD4-57	5.9.1 Low-Threshold Signal				
ACD4-58	Requirement deleted.			check level 3 req	
ACD4-59	5.9.2 Low-Threshold Adjustability				
ACD4-60	Requirement deleted.				
ACD4-61	5.9.3 Pulse Digitization (was Signal Content)				
ACD4-62	When a TACK signal is received, the ACD electronics shall digitize all PMT signal amplitudes with the following precision: --for a pulse below 6.4 pC (10 MIP), precision of <0.0128 pC (0.02 MIP) or 5%, whichever is larger; --for a pulse above 6.4 pC (10 MIP), precision of ≤0.64 pC (1 MIP) or 2%, whichever is larger. The largest signal amplitude to be digitized is at least 128 pC (200 MIP) goal of 640 pC (1000 MIP).	Test	ACD CPT (ACD-PLAN-000038)	We don't have high-Z particles source for testing.	

	The ACD shall transmit to the AEM only digitized signals above the command-adjustable threshold for the specific channel (zero-suppress threshold).				
ACD4-66	5.9.4 Pulse Height Measurement Latency				
ACD4-67	The PMT pulse amplitudes shall be digitized within 18.5 microseconds after a Level 1 trigger is received. (NOTE : Transmission to AEM not included in 18.5 microseconds, for example for the maximum data case, we put out 18 PHA words. This ends up taking ~ 29.5 or 30 usec of time for the PHA)	Test	FREE Functional Test (ACD-TBD-XX)		
ACD4-68	5.9.5 Integral Non-Linearity				
ACD4-69	The integral non-linearity should be ≤ 2% over the top 95% of the signal input range for the low-energe range (below 6.4 pC) for ease of analysis.	Test	ACD CPT (ACD-PLAN-000038)		
ACD4-70	5.9.6 Differential Non-Linearity				
ACD4-71	Based on 1024 channels, the differential non-linearity shall be less than ±10% of the average channel width.	Test	ACD CPT (ACD-PLAN-000038)		
ACD4-72	5.9.7 Temperature Stability				
ACD4-73	The analog signal processing chain shall exhibit temperature stability of gain better than 500 ppm per degree C over the operating temperature range. For both the low range (0 to 6.4 pC ±20%, = 10 MIPs) and the high range (6.4 ±20% to 640 pC, 10 to 200 MIPs, the requirement is 200 MIPs but design goal is 1000 MIPs), the analog signal processing chain shall exhibit	Test	FREE Functional Test (ACD-TBD-XX)		

	temperature stability of its baseline better than 0.05% of full scale per degree C.				
AC D4-74	5.9.8 Test Pulse Injection				
AC D4-75	For test purposes, the ACD electronics shall incorporate the capability to be artificially stimulated by a test charge, via commands. The test charge injection range shall be 0 - 200 MIP with a goal of 0 - 1000 MIP.	Test Simulation	ACD CPT (ACD-PLAN-000038) GAFE Functional Test (ACD-TBD-XX)	This will change if SLAC implements full high-range TCI.	
AC D4-76	5.9.9 Digital Housekeeping				
AC D4-77	The state of all ACD command registers shall be available for readout via AEM commands. The AEM will scale all ACD VETO and HLD rates and transmit the results in low rate telemetry.	Test	ACD CPT (ACD-PLAN-000038)	This is a requirement on the AEM.	
AC D4-78	5.9.10 Temperature Monitoring				
AC D4-79	ACD shall provide temperature transducer signals for survival, safe, and operational modes. Signals are specifically defined in ACD ICD. ACD does not provide the actual temperature monitoring.	Test	ACD CPT (ACD-PLAN-000038)		
AC D4-80	5.10 High Voltage Bias Supply				
AC D4-81	5.10.1 HVBS Output Voltage Range				
AC D4-82	The HVBS shall operate from +400 V to +1310 V.	Test	HVBS Functional (ACD-TBD-XX) ACD CPT	The HVBS shall be characterized in the Functional and exercised in the CPT.	

			(ACD-PLAN-000038)		
ACD4-83	5.10.2 5.10.2 HVBS Output Current				
ACD4-84	The HVBS shall provide sufficient current to drive all PMTs (max 18) on each FREE circuit card at the maximum voltage (+1310V).	Test	ACD CPT (ACD-PLAN-000038)		
ACD4-85	5.10.3 HVBS Limiting Output Current				
ACD4-86	The HVBS output current shall be limited to protect the ACD from one PMT short. At maximum output voltage, each HVBS shall be capable of supplying a total output current of 60 μA. The nominal output current will be 36 μA.	Test	HVBS Functional (ACD-TBD-XX)		
ACD4-87	5.10.4 HVBS Output Voltage Adjustment				
ACD4-88	The HVBS output voltage shall be programmable with an analog input. The limiting output current of each HVBS shall be ~80 μA.	Test	HVBS Functional (ACD-TBD-XX)		
ACD4-89	5.10.5 HVBS Input Power				
ACD4-90	Each HVBS shall operate from a supply voltage of 28V ± 1V, with possible input ripple of 10 mV (frequency range 50 Hz to 50 MHz). The noise shall be less than 100 mV RMS from DC to 1.0 MHz.	Test	HVBS Functional (ACD-TBD-XX)	This is the requirement for the AEM power. The HVBS will be tested to verify it can operate over this range.	
ACD4-91	5.10.6 HVBS Line and Load Regulation				
ACD4-92	The HVBS output voltage shall be regulated to ±0.5% for all combinations of input voltage and load current. (This produces ~5% change in PMT gain).	Test	HVBS Functional (ACD-TBD-XX)		

ACD4-93	5.10.7 HVBS Output Ripple				
ACD4-94	The HVBS output voltage ripple shall be compatible with the ACD ASIC design. The HVBS output voltage ripple shall not exceed ±2 mV p-p over the frequency range 100 Hz to 50 MHz	Test	HVBS Functional (ACD-TBD-XX)		
ACD4-95	5.10.8 HVBS Power Consumption				
ACD4-96	The HVBS power dissipation at maximum output voltage and limiting current shall be <300 mW.	Test	ACD CPT (ACD-PLAN-000038)		
ACD4-97	5.10.9 HVBS Ramp Up/Down Time				
ACD4-98	For either application or removal of input power, the time for the HVBS output voltage to reach its final level (for turn-on, within regulation tolerance) shall be between 5 and 30 seconds. Note: The 5 second requirement is driven by the PMT, the 30 seconds is driven by the maximum tolerable time for HVBS to stabilize when entering/exiting the SAA.	Test	HVBS Functional (ACD-TBD-XX)		
ACD4-99	5.10.10 HVBS Temperature Stability				
ACD4-100	The HVBS output voltage temperature stability shall be no worse than 500 ppm/C.	Test	HVBS Functional (ACD-TBD-XX)		
ACD4-101	5.10.11 HVBS Output Voltage Monitoring				
ACD4-102	The HVBS shall provide a linear output voltage monitor (for transmission to the AEM) in the range 0.0 to 2.5 V.	Test	ACD CPT (ACD-PLAN-000038)		
ACD4-103	5.10.12 HVBS Ground				

	Isolation				
AC D4-104	The DC impedance between input and output grounds shall be 100 ohms ±20%.	Test	HVBS Functional (ACD-TBD-XX)		
AC D4-105	5.10.13 HVBS Oscillator Frequency				
AC D4-106	The HVBS shall utilize an oscillator frequency ≥100 kHz (to minimize EMI issues).	Test	HVBS Functional (ACD-TBD-XX)		
AC D4-107	5.10.14 HVBS EMI and Susceptibility				
AC D4-108	The HVBS shall neither generate nor be susceptible to electromagnetic interference exceeding the EMI/EMC test requirement, GSFC-433-RQMT-0005.	Analysis Test	ACD EMI Test (ACD-TBD-XX)		
AC D4-109	5.115.11 PMT				
AC D4-110	5.11.1 PMT Bias Chain Total Resistance				
AC D4-111	The total resistance of a PMT bias chain shall be such as to result in a nominal current (at the maximum HVBS voltage) of 2 microamps (~100 times the PMT average anode current.)	Test	Resistor Network Acceptance Test (ACD-TBD-XX)		
AC D4-112	5.11.2 PMT Bias Chain Filter Resistance				
AC D4-113	At least four percent of the total resistance of the bias chain shall be in a filter resistor(s) at the high voltage input. This PMT bias chain filter resistance protects against a PMT short with a current limiting resistor and filters out HVBS ripple.	Analysis	Schematic Control Number	Verify from schematics	
AC D4-114	5.11.3 PMT Bias Chain Resistor Distribution				

AC D4-115	The number and values of the remaining resistors in the bias chain shall be selected to be compatible with the selected PMT, Hamamatsu R4443.	Analysis	Schematic Control Number	Verify from schematics	
AC D4-116	5.11.4 PMT Anode Signal Coupling				
AC D4-117	The PMT anode signal shall be coupled into the associated analog electronics via two capacitors of 680 pF in series. A charge leakage bleed-off resistor of at least 1-mega ohms shall be incorporated on the low-voltage side of the capacitor pair.	Analysis	Schematic Control Number		
AC D4-118	5.11.5 PMT Bias Chain Load Resistor				
AC D4-119	A load resistor of $\geq$ 10 KΩ shall be incorporated into the bias network.	Analysis	Schematic Control Number	Verify from schematics	
AC D4-120	5.11.6 PMT Bias Chain Dynode Decoupling				
AC D4-121	The resistors biasing the last three-dynode stages shall be bypassed by capacitors to prevent a drop in gain for very large pulses or the maximum expected high rate of pulses (<1% gain change for 3kHz rate).	Analysis	Bias Chain Dynode Decoupling Test (ACD-TBD-XX)	Verify from schematics	
AC D4-122	5.12 Radiation Tolerance				
AC D4-123	The ACD electronics shall remain within specifications after a total ionizing radiation dose of 4.5 kRad(Si).	Analysis Test	ACD Parts Radiation Test Procedure		

			(ACD-TBD-XX)		
ACD4-124	5.12.1 Single Event Upset Tolerance				
ACD4-125	A single event upset (SEU) shall not cause the ACD electronics to transition to an unsafe state.	Analysis Test	ACD Parts Radiation Test Procedure (ACD-TBD-XX)		
ACD4-126	5.12.2 Latchup Tolerance				
ACD4-127	Parts that show any SEE's at an LET lower than 37 MeV*cm^2/mg shall not degrade the mission performance.	Analysis Test	ACD Parts Radiation Test Procedure (ACD-TBD-XX)		
ACD4-128	5.13 Reliability				
ACD4-863	The ACD reliability allotment from LAT is currently .96 over 5 years.	Analysis Simulation	Reliability Prediciton Assessments for the GLAST ACD. (ACD-TBD-XX)		
ACD4-129	5.13.1 ACD Electronics Reliability				
ACD4-130	No single failure in the ACD electronics shall result in complete loss of signal from more than one ACD detector (tile or ribbon). The overall calculated reliability of the ACD electronics assembly shall be at least 0.98 in one year.	Analysis Simulation	Reliability Prediciton Assessments for the GLAST ACD. (ACD-TBD-XX)		
ACD4-131	5.13.2 5.13.2 ACD Tile Detector Assembly and				

	Scintillator Ribbon Reliability				
ACD4-132	The probability of the loss of both VETO signals from a specific scintillator tile shall be less than 1% in 5 years). The probability of the loss of VETO signals from a scintillator ribbon shall be less than 5% in 5 years. The overall calculated reliability of ACD scintillating tiles and scintillator ribbons shall be at least 0.99 in one year.	Analysis Simulation	Reliability Prediciton Assessments for the GLAST ACD. (ACD-TBD-XX)		
ACD4-133	5.13.3 Requirement moved to 5.12.2.				
ACD4-134	5.13.4 Requirement moved to 5.12.1.				
ACD4-135	5.13.5 ACD Micrometeoroid Shield/Thermal Blanket Reliability				
ACD4-136	The overall calculated reliability of an ACD micrometeoroid shield/thermal blanket shall be at least 0.99 in one year.	Analysis Test Simulation	Johnson Shield Analysis (ACD-TBD-XX)		
ACD4-137	5.13.6 Requirement combined with 5.13.2				
ACD4-138	5.14 Commands				
ACD4-139	5.14.1 Detector On/Off Commands				
ACD4-140	The AEM will implement commands to allow each group of 18 PMT's to be powered on and off together.	Test	ACD CPT (ACD-PLAN-000038)	This is a requirement on the AEM.	GARC Functional Test (ACD-TBD-XX)

ACD4-141	5.14.2 Detector Gain Commands				
ACD4-142	The ACD shall implement adjustability of the high voltage applied to the group of 18 PMT's associated with a single board.	Test	ACD CPT (ACD-PLAN-000038)		GARC Functional Test (ACD-TBD-XX)
ACD4-143	5.14.3 Electronics On/Off Commands				
ACD4-144	The AEM will implement commands to allow each ACD electronics board to be separately powered on and off.	Test	ACD CPT (ACD-PLAN-000038)	This is a requirement on the AEM.	GARC Functional Test (ACD-TBD-XX)
ACD4-145	5.14.4 VETO Threshold Commands				
ACD4-146	The ACD shall implement adjustability of the VETO threshold for each PMT.	Test	ACD CPT (ACD-PLAN-000038)		GARC Functional Test (ACD-TBD-XX)
ACD4-147	5.14.5 High-Threshold Commands				
ACD4-148	The ACD shall implement adjustability of the High-Level Discriminator Threshold for each PMT.	Test	ACD CPT (ACD-PLAN-000038)		GARC Functional Test (ACD-TBD-XX)
ACD4-149	5.14.6 ACD Monitoring Commands				
ACD4-150	The ACD shall implement adjustability of the monitoring functions of the ACD electronics, including the zero suppression for each PMT.	Test	ACD CPT (ACD-PLAN-000038)		GARC Functional Test (ACD-TBD-XX)
ACD4-151	5.14.7 TACK Format				
AC	TACK format shall be in compliance	Test	ACD		GARC

D4-152	with ICD definition of TACK.		CPT(ACD-PLAN-000038)		Functional Test (ACD-TBD-XX)
AC D4-153	5.14.8 Command Format				
AC D4-154	Command formats shall be in compliance with ICD format definitions.	Test	ACD CPT (ACD-PLAN-000038)		GARC Functional Test (ACD-TBD-XX)
AC D4-155	5.14.9 SAA Mode commands				
AC D4-156	The ACD photomultiplier HVBSs shall switch into a low-gain mode to protect the phototubes in very high intensity particle conditions (> 10 kHz in an individual tile) such as the South Atlantic Anomaly. (Accomplished by HVBS command from AEM to GARC)	Test	ACD CPT (ACD-PLAN-000038)		GARC Functional Test (ACD-TBD-XX)
AC D4-157	5.14.10 Notification of Mode Change				
AC D4-158	The ACD shall identify times when it switches into low-gain mode for high counting rate conditions.	Test	ACD CPT (ACD-PLAN-000038)		GARC Functional Test (ACD-TBD-XX)
AC D4-159	5.15 Output Data Formats				
AC D4-160	ACD Output data formats shall be in compliance with ICD format definitions.	Test	ACD CPT (ACD-PLAN-000038)		GARC Functional Test (ACD-TBD-XX)
AC D4-161	5.16 Power Consumption				
AC D4-162	The ACD total electronics power consumption shall not exceed 31 W conditioned.	Analysis Test	ACD CPT (ACD-PLAN-000038)		

ACD4-163	5.17 Total ACD Mass				
ACD4-164	The total mass of the ACD shall not exceed 280 Kg. (The mass was increased from 235 Kg pending signature approval of CR# XR1200-01)	Analysis Test	Post ACD I&T Mass Properties CAD Model Mass Properties	Mass number will probably increase shortly	
ACD4-165	5.18 Environmental Requirements				
ACD4-166	The ACD shall meet all structural, thermal, EM and radiation environment requirements.				
ACD4-167	5.18.1 Ground – Handling and transportation Vibration and Shock				
ACD4-168	Deleted in LAT level IIb 12/10/01, see ACD Transportation and Procedure (ACD-TBD-XX)	Analysis	Structural Analysis	Refer to trans plan, monitoring of loads during transport ?	
ACD4-169	5.18.2 Orbit - Flight temperature ranges				
ACD4-856	ACD shall be able to handle orbit survival and operational temperature ranges specified in the ACD ICD (LAT-SS-363)	Analysis Test	ACD Thermal Vacuum Procedure (ACD-TBD-XX), ACD CPT (ACD-TBD-XX)	Refer to trans plan, monitoring of loads during transport	
ACD4-185	5.18.3 Launch - Static Load				
ACD4-186	ACD shall be capable of normal operation after exposure to launch loads as given in SI/SC IRD (sec 3)	Analysis Test	Structural Analysis ACD Vibration Test Plan (ACD-	The metallic structure of the BFA is being designed to factors of safety that require no qual testing (ie, 2.0 yeild, 2.6 ultimate) while the composite structure static	

			TBD-XX)	strength is being validated through a program of static test coupons (and vibration testing for workmanship) . We have used sine burst testing on the TDT vibration tests to 'qualify' much of the composite design and the TDA designs. (Vibration Test Plan - unwrapped and wrapped tiles). ACD may propose variances from loads and tests on some assemblies specified here in referenced documents, in the LAT Verification Plan and the LAT Environmental Limits document LAT-SS-00788 to avoid over loading and or over testing some items.	
AC D4-187	5.18.4 Launch - Random Vibrations				
AC D4-188	ACD shall be capable of normal operation after exposure to ASD levels referred to in the SC IRD which are given in GEVS Table D-6	Analysis Test	Structural Analysis ACD Vibration Test Plan (ACD-TBD-XX) (Electronics and Mechanical Random tests will be listed separetly in the above	ACD may propose variances from some loads and tests on some assemblies specified here in referenced documents, in the LAT Verification Plan and the LAT Environmental Limits document LAT-SS-00788 to avoid over loading and or over testing some items.	

			test plan, see Table 2 - Test Matrix for what assemblies and components see what accept and qual tests)		
ACD4-189	5.18.5 Launch - Acoustic Loads				
ACD4-190	Capable of normal operation after exposure to acoustic loads given in SI/SC IRD which refers to spec 433-SPEC-0003, the acoustic equivalant design loads are derived in ACD SPEC-3006 (this used to refer to GEVS Table D-3 T but has been changed). (Note : information on acoustic abatement at the GLAST launch pad and preliminary acoustic loads analyses for ACD have reduced acoustic loads)	Analysis Test	Structural Analysis ACD Acoutics Test Plan (ACD-TBD-XX)	The reduced acoustic loads have also been converted to equivalent random vibration inputs for qualification testing of the TSA and TDA. Acoustic loads may be the highest loads applied during ACD full assembly verification testing!	
ACD4-191	5.18.6 Launch – Shock				
ACD4-192	Capable of normal operation after exposure to external shock levels given in GEVS Table D-8 or D-9, as applicable, attenuated to SI/SC interface values.	Analysis	Structural Analysis		
ACD4-193	5.18.7 Launch – temperature				
ACD4-194	Tolerate 0 to 30 °C in launch configuration (Note - Considering asking for lower temp (~0 to 15C) to help Tile Gap issue)	Analysis	Thermal Analysis Structural Analyisis		
ACD4-195	5.18.8 Launch – Pressure				

AC D4-196	Flux Environment				
AC D4-197	Tolerate Earth IR loads of 265 W/m^2 (hot case), and 208 W/m^2 (cold case), plus Earth Albedo factor of 0.40 (hot case), and 0.25 (cold case) . See LAT Thermal Design Parameters Study LAT-TD-00224.	Analysis	Thermal Analysis		
AC D4-198	Environment				
AC D4-199	Solar Flux - 1419 W/m^2 (hot case), and 1286 W/m^2 (cold case), sustained exposure on +X side. See LAT Thermal Design Parameters Study LAT-TD-00224.	Analysis	Thermal Analysis		
AC D4-200	5.18.9 On-orbit – Thermal				
AC D4-857	Handle orbit interface, survival and operational thermal values specifed in ICD.	Analysis Test	ACD Thermal Vacuum Procedure (ACD-TBD-XX), ACD CPT (ACD-TBD-XX)	Refer to trans plan, monitoring of loads during transport	
AC D4-202	5.18.10 On-Orbit Charged Particle Radiation				
AC D4-203	Deleted from LAT IIb				
AC D4-204	5.18.11 On-Orbit - Meteoroid and Debris Flux				
AC D4-205	Instrument must withstand meteoroid and debris flux estimates given in GLAST MSS Section 'Micrometeoroid and Debirs Flux' for impact probabilities of 0.001 and above	Analysis Test	Johnson Shield Analysis		
AC D4-	5.19 Performance Life				

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ACD4-207	The ACD shall maintain the specified performance for a minimum of five years in orbit.	Analysis	Reliability Prediciton Assessments for the GLAST ACD. (ACD-TBD-XX)		
ACD4-208	5.20 Rate Requirement for Operation within Specification				
ACD4-209	Each ACD PMT and its associated electronics shall be capable of operating within the specifications above at MIP rates up to 3 kHz. (The 3kHz per tile is just above the high count rate.)	Test	BEA Functional Test (ACD-TBD-XX)	This is a LAT level issue. The BEA Functional will include a high rate test.	
ACD4-210	5.21 Testability				
ACD4-211	The ACD electronics shall incorporate additional capabilities as needed to enable thorough and efficient testing, throughout the GLAST mission, of the functions required of the ACD.	Test Inspection		Our tests will confirm efficient testing ability	
ACD4-212	5.22 Center of Mass				
ACD4-213	The ACD center of mass shall be X=Y<5 mm and Z<393 mm as listed in the ACD-LAT ICD (LAT-SS-00363)	Analysis Test	Post ACD I&T Mass Properties CAD Model Mass Properties		
ACD4-214	5.23 Volume				
ACD4-215	As shown in the ACD IDD (Interface Definition Drawings) (LAT-DS-00309, 00040 & 00038), the ACD volume shall be:	Analysis Inspection	CAD model		
ACD4-	Inside LAT Grid: 1574 x 1574 x -204.7 mm				

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AC D4-217	Inside LAT Tracker: 1515.5 x 1515.5 x 650 mm				
AC D4-218	Outside: 1806 x 1806 x 1050 mm (these dimensions have been agreed upon by all of the necessary individuals, however, they will be finalized upon the signature approval of the LAT ACD Interface Definition Drawings. The previous outside volume is 1796 x 1796 x 1015 mm.				
AC D4-219	5.24 Instrument Coverage				
AC D4-220	The ACD TDA's shall cover the top and sides of the LAT trackers down to 0.5 mm below the top of the CsI in the Calorimeter. See ACD IDD (Interface Definition Drawings) (LAT-DS-00309, 00040 & 00038).	Analysis Inspection	CAD model		
AC D4-221	5.25 LAT to ACD Gap.				
AC D4-222	The minimum ACD distance from the LAT Trackers shall be as defined in LAT-DS-00038 or ACD IDD (Interface Definition Drawings) (LAT-DS-00309, 00040 & 00038).	Analysis	CAD model		
AC D4-223	5.26 Material interaction of gamma radiation (Gamma radiation due to ACD material interactions)				
AC D4-224	The ACD shall cause interaction of less than 6% of the incident gamma radiation.	Analysis	Interaction Analysis report		
AC D4-225	5.27 Thermal Blanket/ Micrometeoroid Shield Areal Mass Density				
AC D4-226	The thermal blanket/micrometeoroid shield shall have mass per unit area of ~ <0.32 g/cm^2 which should minimize	Analysis			

	secondary gamma-ray production by undetected cosmic ray interactions.				
AC D4-227	5.28 Gaps between scintillating tiles				
AC D4-228	The gaps between scintillating tiles shall be small enough over the operating temperature range to meet the ACD efficiency requirement. See tile gap analysis trade study.	Analysis Inspection Simulation	Thermal Analysis Structural Analysis Acoustical Analysis CAD Model Post Tile Integration Inspection		
AC D4-229	5.29 Light Throughput				
AC D4-230	The amount of light transmitted from the scintillating tiles to the PMT shall be sufficient to produce a signal of 18 P.E. for one MIP.	Test Simulation	Channel characterization Test (ACD-TBD-XX)		

6 Verification and Environmental Test Programs

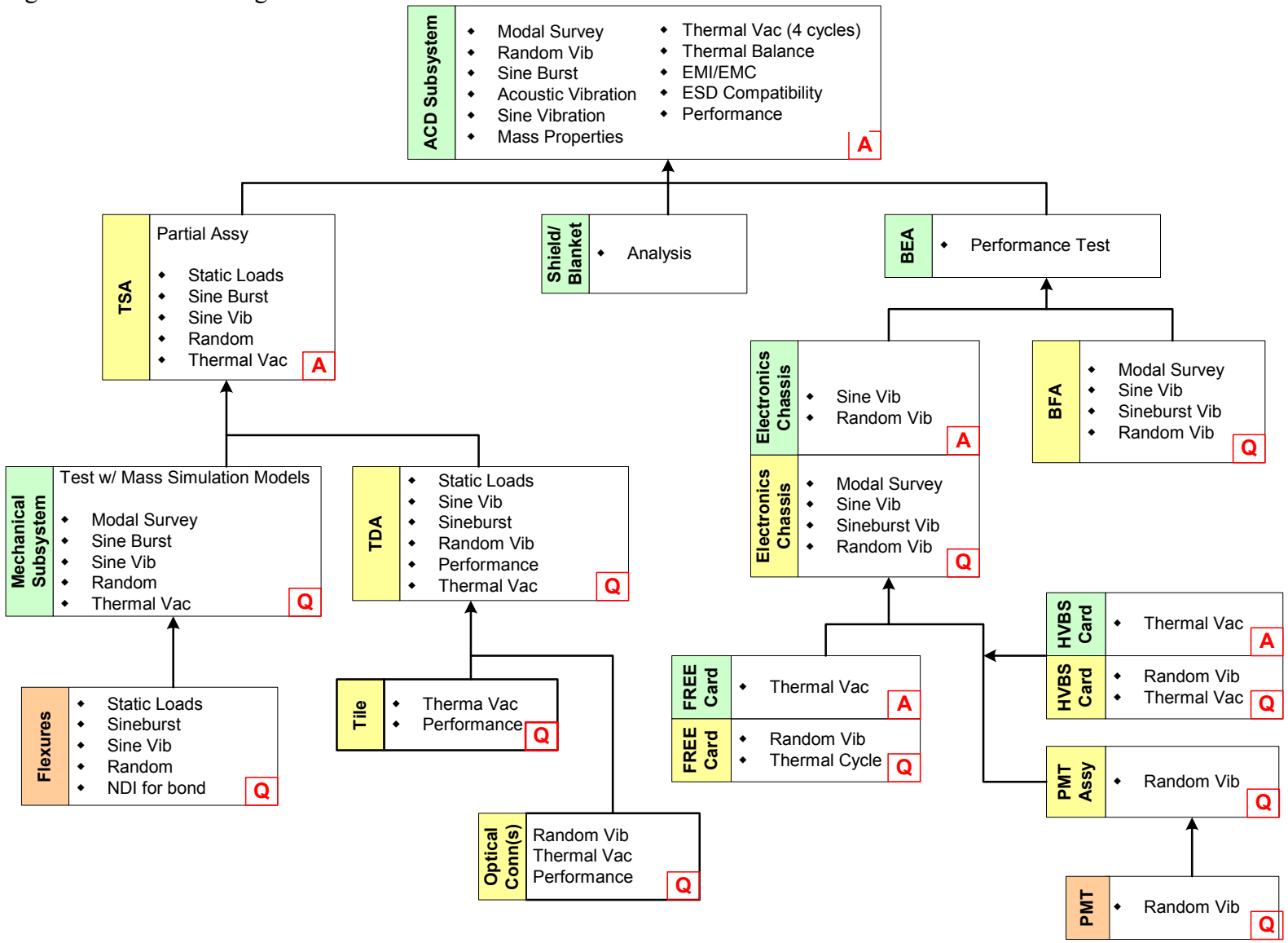
6.1 ACD ICD Verification

Many of the major items in the ACD ICD (Interface Control Document) and ACD IDD (Interface Definition Drawing) are flowed to the Level 4 requirements and therefore their verification methods and tests are shown above in the verification table. Many of the other Electrical specifications are verified in the same performance tests referred to in the table. See those test plans for details. Mechanical inspection procedures will exist which will verify many mechanical interface items in the ICD and IDD. A few items in the ICD (some thermal and interface loads) are not verifiable in ACD level tests and are verified by analysis. All ICD item verification will be tracked in an ICD checklist which will be re-reviewed before fabrication and tracked throughout the I&T process.

6.2 ACD Environmental Test Flow and Test Matrix

Because ACD is a protoflight instrument it may propose variances from test guidelines stated in LAT-SS-00788, LAT Environmental Specification. The following diagram (Figure 1) attempts to summarize the various environmental tests performed on ACD and its subsystems as it comes together.

Figure 1. ACD Test Diagram



Below is the ACD Test Matrix (Table 2) which primarily covers environmental tests performed on ACD and its subassemblies and components. Performance tests are covered only at a top level, refer to the verification table above to match individual performance tests to individual requirements

Table 2 ACD Test Matrix – Note : The test matrix is not yet final, a very few tests mentioned in section 6.2 below are not yet shown in the matrix for all components at all levels. See the notes in section 6.2 for comments on some of these. The 'h' in some boxes(to show tested at higher level) is not inclusive, in other words it is not put in every box where that test is done at a higher level just boxes where the comment is important or where questions may arise

TABLE LEGEND:

LEVEL OF ASSEMBLY

S - Subsystem

SA - Subassembly

C - Component

P - Part

UNIT TYPE

D - Development Model

EM - Engineering Model

F - Flight

S - Spares

C - Calibration

BB - Breadboard

NOTES:

a. Composite structure

b. Test-to-failure

c. May be tested at next higher ass'y

d. Test for light yield and repeatability

h. Will be tested at higher level

r. random test covered by acoustic test

e. Test with mass models

s. Tested by supplier

	Hardware			Structural/Mechanical											Electrical						Thermal		
Item	Level of Assembly	Unit Type	Supplier	Test Levels	Test Status	Modal Survey (low level sine survey)	Static Loads	Sine Burst	Sine Vibration	Random Vibration	Mechanical Function	Performance Testing (Optical)	Acoustics	Mass Properties	Interface Verif.	EMC/EMI	ESD Compatibility (Grounding)	Magnetics	Screening Process	Aliveness (A) / Functional (F) / Comprehensive (C)	Thermal-Vacuum Cycle	Thermal Cycle	Thermal Balance
ACD Subsystem (Integrated AC	**S**	**F**	**GSFC**	**Acpt**		**X**			**X ?**	**X?-r**		**X**	**X**	**X**	**X**	**X**	**X**			**C**	**4**		**X**
Tile Shell Assembly	SA	F	GSFC	Acpt										X ?									
Tile Shell Assembly - partial	SA	D	GSFC	Qual			X-b	X	X	X	X			X							6		
ACD Mech S/S (no elect or Det)	S	F	GSFC	Qual		X-e		X-e	X-e	X-e	X			X							2		
Shell	C	F	TBD	Par Qual		X-e		X-e	X-e	X-e				X							2 ?		
Shell - partial	P	D	GSFC	Qual			X-b	h	h	h													
Tile Detector Assembly	SA	F	Fermilab	Acpt				X		X		X-d	h	X						A, F-h			
Tile Detector Assembly	SA	S	Fermilab	Acpt						X		X-d									8		
Tile Detector Assembly	SA	EM	Fermilab	Qual				X	X	X		X-d		X						F	6		
Tile Detector Assembly	SA	D	Fermilab	Qual			X	X		X		X-d									6		
TDA Tiedown (Flexure)	P	F	GSFC	TBD			X-c							X									
TDA Tiedown (Flexure) ?	P	EM	GSFC	Par Qual			X-c	X	X	X	X			X							h		
TDA Tiedown (Flexure)	P	D	GSFC	Qual			X-b														h		
WSF/Clear Fiber Connector	C	F	GSFC	TBD										X						A, F-h			
WSF/Clear Fiber Connector	C	EM	GSFC	Par Qual						h	X	X-c		X						F	h		
WSF/Clear Fiber Connector	C	D	GSFC	Qual				X ?		h	X	X-d								A?	h	8-d	
Base Frame	C	F	GSFC	Par Qual		X-e-c		X-e-c	X-e-c	X-e-c				X							4-c		
Partial BFA & Electronics Chassis	SA	EM	GSFC	Qual		X		X-?	X	X						X	X?	X?		F		2?	
Base Frame - partial	C	D	GSFC	Par Qual			X		X-e	X-e													
Shield & Thermal Blanket	C	F	GSFC											X							4-c		
Shield & Thermal Blanket	C	EM	GSFC											X									
Shield & Thermal Blanket	C	D	JSC, GSF	Qual																	6		
Clear fiber cable assembly	SA	F	GSFC	Qual					X-c	X-c		X								A			
PMT/Fiber Connector	C	F	GSFC	TBD						X-c	X-c	X-c		X						A			
PMT/Fiber Connector	C	EM	GSFC	Par Qual							X	X-c		X						F	6-c		
PMT/Fiber Connector	C	D	GSFC	Qual						X	X	X-d								F		8-d	
Base Electronics Assembly	S	F	GSFC	Acpt					X-?	X-?										F			
Electronics Chassis	SA	F	GSFC	Acpt					X	X				X	X					F	2?		
Electronics Chassis	SA	EM	GSFC	Qual		X		X	X	X				X						F	10		
Electronics Chassis	SA	D	GSFC	Qual																F	2		
Electronics Chassis	SA	BB	GSFC																	F			

	Hardware			Structural/Mechanical											Electrical						Thermal		
Item	Level of Assembly	Unit Type	Supplier	Test Levels	Test Status	Modal Survey (low level sine survey)	Static Loads	Sine Burst	Sine Vibration	Random Vibration	Mechanical Function	Performance Testing (Optical)	Acoustics	Mass Properties	Interface Verif.	EMC/EMI	ESD Compatibility (Grounding)???	Magnetics	Screening Process	Aliveness (A) / Functional (F) / Comprehensive (C)	Thermal-Vacuum Cycle	Thermal Cycle	Thermal Balance
FREE Board (12)	C	F	GSFC	Acpt						X-c					X					F		X ?	
FREE Board (2)	C	S	GSFC	Acpt						X					X					F	12 ?	8	
FREE Board (4)	C	EM	GSFC	Qual		h		h	h	X				X	X	h	?			F	2	X	
FREE Board (4)	C	D	GSFC	Par Qual											X					F			
FREE Board (2)	C	BB	GSFC																	F			
FREE Board Parts	P	F,D	Multiple	*																			
PMT Rail	SA	S	GSFC	Acpt					X	X													
PMT Rail	SA	D	GSFC	Qual					X	X													
PMT Subassembly (194)	P	F	H, GSFC	Acpt						X-c					X					F		X ?	
PMT Subassembly (46)	P	S	H, GSFC	Acpt						X					X					F	12 ?		
PMT Subassembly (qual PMTs)	P	EM	H, GSFC	Qual		h		h	h	X				X	X	h	?			F	2		
PMT Subassembly (6)	P	D	H, GSFC	Par Qual			X-b			X					X					F	6		
PMT Subassembly (30)	P	C	H, GSFC												X					F		X	
PMTs (not bonded) (240)	P	F	H			h		h	h	h		h							X	F-s			
PMTs (not bonded) (10)	P	D	H							X ?		X							X	F-s			
PMTs (not bonded) (30)	P	C	H																	?			
Resistor Network (194)	C	F	GSFC							h										F			
Resistor Network (46)	C	S	GSFC							h										F			
Resistor Network (calibration)	C	EM	GSFC							h				X	X					F			
Resistor Network (6)	C	D	GSFC												X					F			
Resistor Network (46)	C	C	GSFC																	F			
HVBS (24)	C	F	GSFC	Acpt					X ?	X-c					X					F	2		
HVBS (2)	C	S	GSFC	Acpt					X	X					X					F	12 ?		
HVBS (4)	C	EM	GSFC	Qual		h		h	h	X					X	h	?			F	2		
HVBS (3)	C	D	GSFC	Par Qual																F			

6.3 Test Programs

The tests ACD will undergo as part of this verification plan are listed and briefly discussed below.

Subsystem Qualification Test Program
A complete qualification program will be executed for the LAT subsystem components. The objective of this test program is to qualify for flight all subsystem components prior to production.

Qualification tests will be performed on all components that are subject to environmental acceptance tests. These tests will be conducted to the qualification test level outlined in the LAT Environmental Limits LAT-SS-00788 (Note - ACD is still reviewing those levels, has some comments and may propose some variances).

Electrical Interface Tests
Electrical interface tests are conducted to insure integrity of the electrical interfaces. Depending on the circumstances, one or more of the following tests will be performed:

- Signal distribution
- Power Distribution
- Command Distribution
- Grounding
- Isolation
- Insulation Resistance
- Hi-Pot

Thermal Vacuum
Thermal vacuum testing with thermal cycling will be performed on all components. All components will be subjected to 12 cycles (however ACD may propose variances to this based on our protoflight status) at unit/component level for qualification. A soak/dwell of 12 hours minimum at each temperature extreme will be observed. One hot and cold turn on sequence will be performed at the appropriate dwell points. Comprehensive Performance tests will be performed at each dwell point.

Limited performance tests will be performed during transitions for the purpose of monitoring the instrument systems for failures and intermittent operations.

To verify a previously qualified component for the LAT, it will be subjected to 4 Thermal Vacuum cycles to acceptance temperature limits. A soak/dwell of 4 hours minimum at each temperature extreme will be observed.

One hot and cold turn on sequence will be performed at the appropriate dwell points. This test is used for credit against the LAT level requirements. Limited Performance tests will be performed at each dwell or soak point as well as during
transitions.

Thermal Cycling
Thermal cycling at ambient pressure will be performed on a case by case basis to perform workmanship tests.

Thermal Balance
A thermal balance test will be conducted during the planned thermal vacuum test program to demonstrate the operational capability of the LAT Thermal control system and the LAT thermal design itself. The thermal balance test data will be used to validate the LAT thermal models and to predict on-orbit performance.

Humidity /Storage Tests
The LAT program will use analysis supported by test when necessary to demonstrate that the hardware produced for flight use meets the storage and humidity requirements set for the program. The results of the test or analysis will become part of the qualification data package.

Comprehensive Performance Tests
Comprehensive performance tests as appropriate will be conducted prior to, during and after each environmental test. These tests will exercise all unit operating modes as well as primary and redundant circuits and paths. Parameters will be varied over their specification ranges to insure that the unit performs as designed.

Limited Performance Tests
LPTs will be performed during, and between environmental tests, as appropriate, to demonstrate that the functional capability of the unit has not been degraded by an environmental test.

Burn In Tests
Burn in tests at the Acceptance Level high temp will be used to achieve 150 hours of failure free power on time prior to delivery to LAT integration on all units which have been acceptance tested. This will be done on ACD ASICs

Structural, Mechanical & Alignment Tests
Mechanical tests are performed at successively higher levels of integration to provide the minimum program risk and maximum risk reduction benefit and cost to the program. Tests will be performed to the levels published in the LAT-SS-00788, LAT Environmental Spec (Note - ACD is still reviewing those levels, has some comments and may propose some variances).

Random Vibration
All units will be subjected to a random vibration test to qualification levels. The Random vibration qualification levels are defined in LAT-SS-00788, LAT Environmental Specification (Note - ACD is still reviewing those levels, has some comments and may propose some variances). The ACD does not have to be subjected to a 3-Axis random vibration test sequence. (Note - The ACD acoustic tests may effectively replace this to avoid over testing). All ACD electrical subsystem assemblies will be subjected to random vibration tests as a workmanship test (some mechanical components may not). Random vibration will be conducted on at least the electrical qualification units (Keep in mind many ACD subsystems and the ACD assembly are ‘protoflight’ units).

Sine Vibration

Sine vibration tests will be conducted on all qualification hardware. The Sine vibration qualification levels are defined in LAT-SS-00788, LAT Environmental Specification (Note - ACD is still reviewing those levels, has some comments and may propose some variances).

Mechanical Shock Test
Mechanical shock tests will be performed at observatory level if required. The mechanical shock qualification levels will be defined after analysis of the coupled loads and transfer of shock through the spacecraft. The LAT has no shock inducing components.

Proof Tests
Proof tests will be conducted on composite materials used on the LAT as called out in the GEVS, section 2.4.1.4.1 regarding the use of composites on primary and secondary structures.

Static Load Tests
All LAT subsystem mechanical components will be subjected to static load tests. These tests will be conducted on Qualification level components. (TBD - A few components are not scheduled to see static load tests at this time)

Dynamics Tests
Dynamics tests are to be performed in the mode which the equipment will observe the environment. The LAT will be launched in a "powered off" mode. All dynamics tests which are for launch environment verification will be performed with the test article powered off.

Sine Burst Vibration
The ACD will (TBD not currently shown on test matrix) conduct a sine burst vibration test on the proto-flight ACD subsystem.

Sinusoidal Sweep Vibration
Sine-Sweep vibration tests will be performed on some select components prior to integration to reduce design risk as described. The ACD will conduct a sine sweep vibration test on the flight subsystem.

Vibro-acoustic Tests
ACD will conduct vibro-acoustic tests on the ACD subsystem.

Modal Survey Test
A modal survey test of the flight LAT will be performed to assess the design against the expected modal frequencies and to reduce the risk of incompatibility of the LAT with environmental conditions. The ACD will conduct a stand-alone Modal Survey test on the ACD subsystem. (Note – is a low-level sine survey enough?)

Mechanical Shock
The LAT program will conduct mechanical shock testing at the integrated observatory level.

Pressure Profile
Pressure profile verification will be verified by analysis on each subsystem. (TBD)

Mass Properties

The ACD will collect mass properties and CG information.

Dimension & Fit Checks
Dimensions and fit checks will be made on all subsystem components prior to integration with the LAT.

Electrical Tests

Interface Verification Tests
Interface verification tests will be performed on all subsystem electrical components prior to integration. Measurements will be made of all interface electrical signals. Grounding, isolation and insulation resistance (hi-pot) tests will be performed prior to connecting a new subsystem component to an integrated assembly.

Electrical interface cables will be tested for continuity, impedance, isolation and insulation resistance (hi-pot) prior to integration with flight hardware.

Electromagnetic Interference / Compatibility (EMI/EMC)

Electronics Assemblies and Components
Tests will be performed on all subsystem electrical hardware assemblies (electronics) and the integrated LAT instrument to satisfy the requirements of the SC/IRD with respect to Electromagnetic Interference And electromagnetic Compatibility. Tests for radiated emissions and susceptibility will be performed on each component at the qualification level.

Abbreviated tests will be conducted on the flight components to verify that the measurements taken on qualification hardware are similar to those observed on flight articles. The LAT instrument will be tested for radiated /conducted emissions and radiated / conducted susceptibility as an integrated instrument.

Optical Tests
The ACD will perform optical performance tests on the flight ACD optical components (PMTs, optical fibers, tiles, etc.).

Electrical Static Discharge (ESD) Compatibility Tests
ESD compatibility tests will be conducted on each subsystem electrical component at the qualification level. These tests are to ensure proper grounding of the electrical/electronics assemblies with the LAT structure.

Comprehensive Performance Tests (CPT)
Comprehensive performance tests will be developed for use in support of LAT testing. LAT CPT testing will demonstrate the operation of all primary and redundant circuitry and paths for all operational modes. Parameters will be varied over their specification ranges to insure that the unit performs as designed. These tests will be performed to provide baseline data for each level of assembly. A CPT will also be conducted during the hot and cold extremes of the temperature test or the thermal-vacuum test and at the conclusion of the environmental test sequence as well as at other times as needed in the verification procedures.

The LAT CPT will demonstrate that the hardware and software meet their performance requirements. The CPT will also demonstrate that the instrument produces the expected responses. At lower levels of assembly, the test will demonstrate that, when provided with appropriate inputs, internal performance is satisfactory and outputs are within acceptable limits.

Limited Performance Tests (LPT)

LPTs will be performed at the instrument level before, during, and after environmental tests, as appropriate, to demonstrate that the functional capability of the instrument has not been degraded by an environmental test.

Limited Performance tests will be a subset of the CPT. Electrical tests include the application of expected voltages, impedance, frequency, pulses, and waveforms at the electrical interfaces. Mechanical tests shall include application of torque, load, and motion as appropriate.

Aliveness Tests

An aliveness test will be performed to verify that the instrument and its major components are functioning and that changes or degradation have not occurred as a result of environmental exposure, handling, transportation, or faulty installation. Aliveness tests will be performed at various locations in the test flow where it is necessary to determine that the test article still functions.

Radiation

Compliance with radiation environments of Total Ionizing Dose (TID) and Single Event Effects (SEE) will be performed by analysis. No specific radiation testing is planned (Note – with one possible exception, radiation testing of ASICs is planned). Specification for the TID is contained in the LAT-SS-00788, LAT Environmental Specification.