Reliability Assessments Scope

- **Per paragraph 8.2.4 of the MAR and PAIP**

" When necessary/prudent or when agreed upon with the GSFC Project Office, Glast LAT will perform ***comparative numerical reliability assessments*** to**:**

a) ***Evaluate alternate design concepts, redundancy and cross-strapping approaches, and part substitutions***

b) Identify the elements of design which are the greatest detractors of system reliability

c) Identify those potential mission limiting elements and components that will require special attention in part selection, testing, environmental isolation, and/or special operations

d) Assist in evaluating the ability of the design to achieve mission life requirement and other reliability goals as applicable

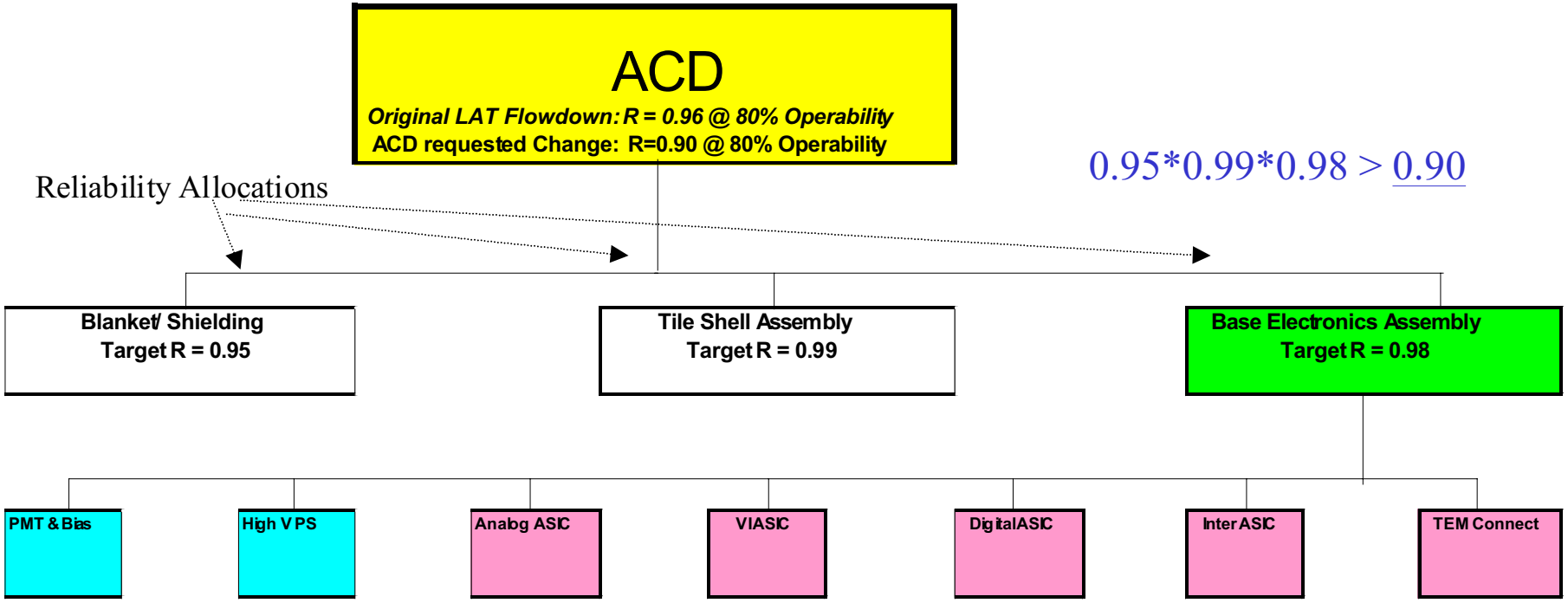
e) Evaluate impact of proposed engineering changes and waiver requests on Reliability

Reliability Assessments Scope (cont.)

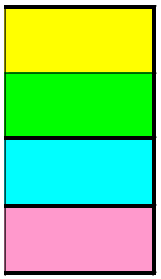
In accordance with ***a) of paragraph 8.2.4*** of the PAIP and MAR, a numerical assessment was performed to evaluate different High Voltage Power Supply redundancy approaches in order to maximize the probability for mission success over the life (*5 Year MINIMUM*!!) of GLAST

The ACD Reliability Target, flowed-down from the LAT, was originally 0.96 at 80% operability (that is, less than 20% degradation of the effective LAT area) over 5 years minimum. A change from 0.96 to 0.90 was requested in order to maintain the 0.95 target for the meteorite shield as defined in our Level 3 specification (1% chance of a puncture somewhere per year), which is documented on the next page.

GLAST ACD - Comparative Numerical Assessments



Legend:



Reliability/Operability Goal flowdown from SLAC

Target area for Comparative Numerical Assessments

Reliabilty Estimates based on Mil-217F and supplier data

Reliability allocated as needed to meet SLAC flowdown

GLAST ACD - Comparative Numerical Assessments (cont.)

Base Configuration: 12 ACD Event Processor boards with 18 PMTs, 18 VI_ADC ASICs, 18 Analog ASICs, 2 Digital ASICs, 1 Interface ASIC, & 1 TEM Interconnect each

High Voltage P/S Redundancy configurations analyzed:

A - 1 P/S per board, 0 stand-by (1 active P/S per 18 PMTs)

B - 2 P/S per board, 1 stand-by (1 active P/S per 18 PMTs)

C - 3 P/S per board, 2 stand-by (1 active P/S per 18 PMTs)

D - 2 P/S per board, 0 stand-by (2 active P/S per 9 PMTs)

E - 4 P/S per board, 2 stand-by (2 active P/S per 9 PMTs)

F - 6 P/S per board, 4 stand-by (2 active P/S per 9 PMTs)

Key Points

- Assumptions (see next page) are subject to change
- Intent of analysis is to show sensitivity to P/S redundancy

GLAST ACD - Comparative Numerical Assessments (cont.)

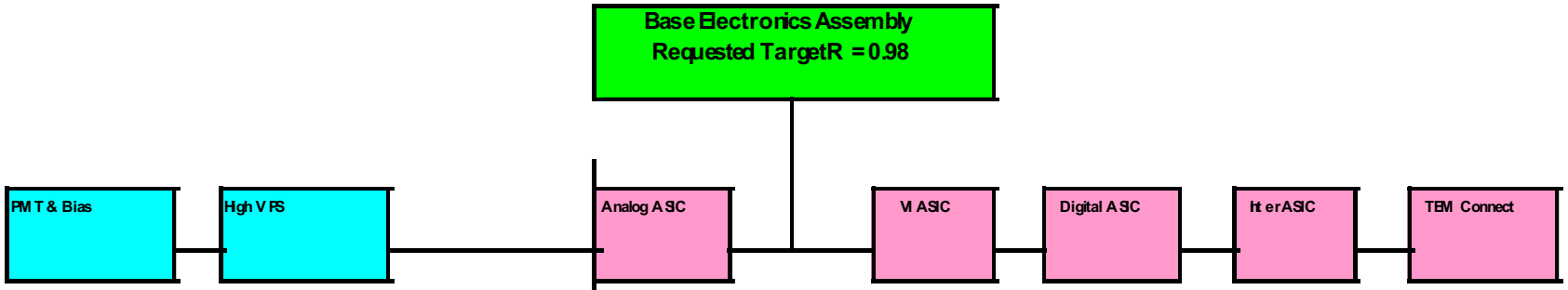
Assumptions/Ground Rules

- ACD Base Electronics Assembly allocation is 0.98, flowed down from the ACD reliability target of 0.96 reliability at 80% operability or, in other words, no more than 20% degradation of the overall effective LAT area

TEAM requesting that the ACD reliability target be lowered to 0.90

- Inability to process information from more than 1 tile constitutes failure (where data from at least one tile PMTs is required in order to process data)
- The ACD is broken down into 7 major components: PMT & Bias, High Voltage P/S, Analog ASIC, VI ASIC, Digital ASIC, Interconnect ASIC, & TEM Connect. Failure rates are estimated for the PMT & Bias and High Voltage P/S only. All other reliability values are represented as allocations
- P/S failure rates are based on Mil-STD-217F (notice 2) without considerations to temperature or derating. PMT failure rates are based on Hamamatsu projections for fully screened space parts. Solder connection and board reliability are not considered
- Fourteen of 18 PMTs are to be functional per board
- Stand-by switching is perfect

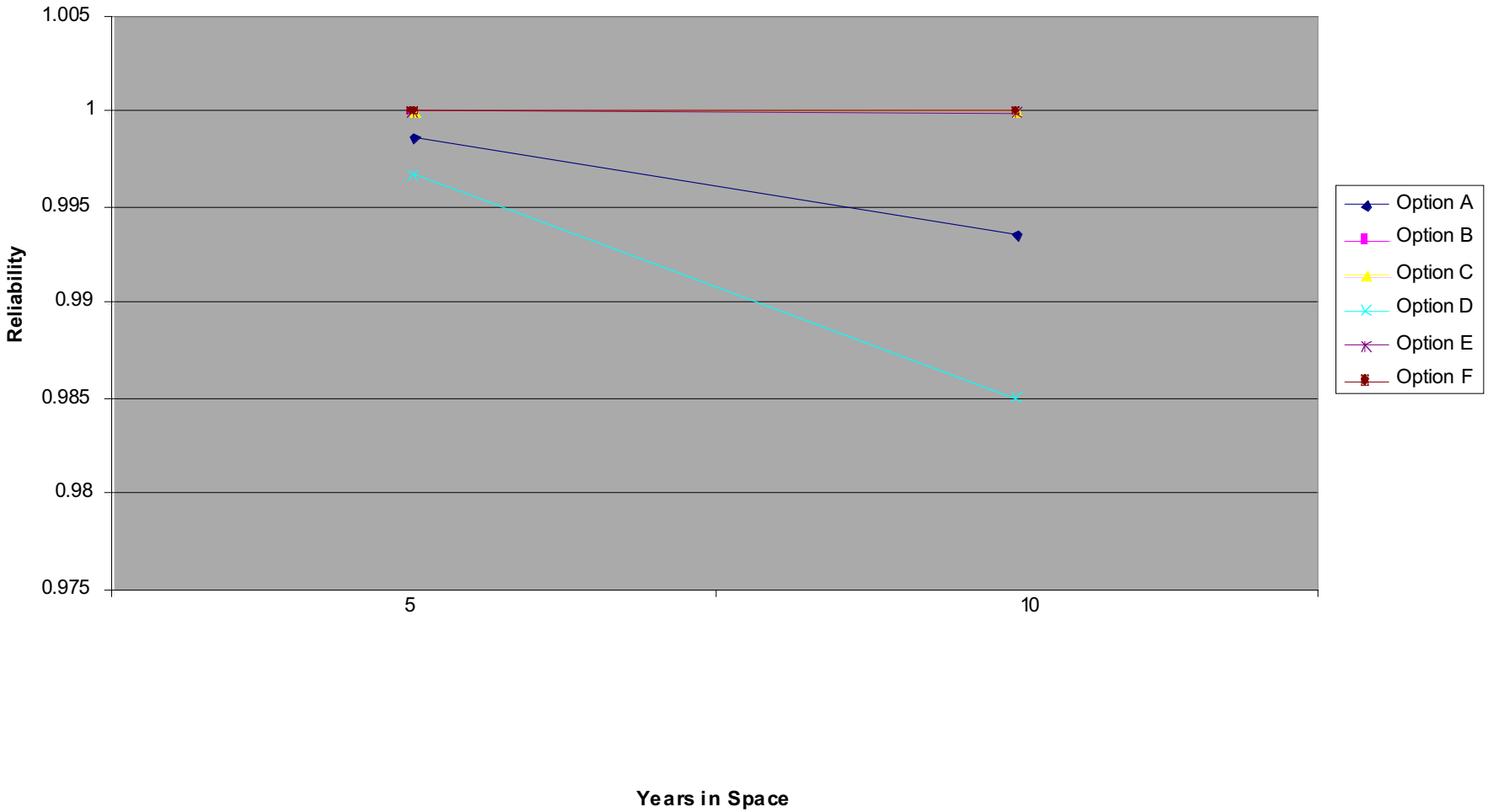
GLAST ACD - Comparative Numerical Assessments (cont.)



Options	Estimated Reliabilty (5 yr)					Required Allocation (5 yr)
A	0.999999994	x	0.998704116	=	0.998704154	0.98127158
B	0.999999994	x	0.999999814	=	0.999999808	0.98000019
C	0.999999994	x	0.99999997	=	0.999999964	0.98000004
D	0.999999994	x	0.9967	=	0.996699994	0.98324471
E	0.999999994	x	0.999970726	=	0.99997072	0.9800287
F	0.999999994	x	0.999999	=	0.999998994	0.98000099

Options	Estimated Reliabilty (10 yr)					Required Allocation (10 yr)
A	0.999999994	x	0.993601386	=	0.99360138	0.98631103
B	0.999999994	x	0.99998553	=	0.999985524	0.98001419
C	0.999999994	x	0.99999997	=	***0.999999964***	0.98000004
D	0.999999994	x	0.98499	=	0.984989994	0.99493396
E	0.999999994	x	0.999937697	=	0.999937691	0.98006107
F	0.999999994	x	0.999999	=	***0.999998994***	0.98000099

Power Supply Reliability over time



Back-up Materials

PER MIL217-F /HV in series,

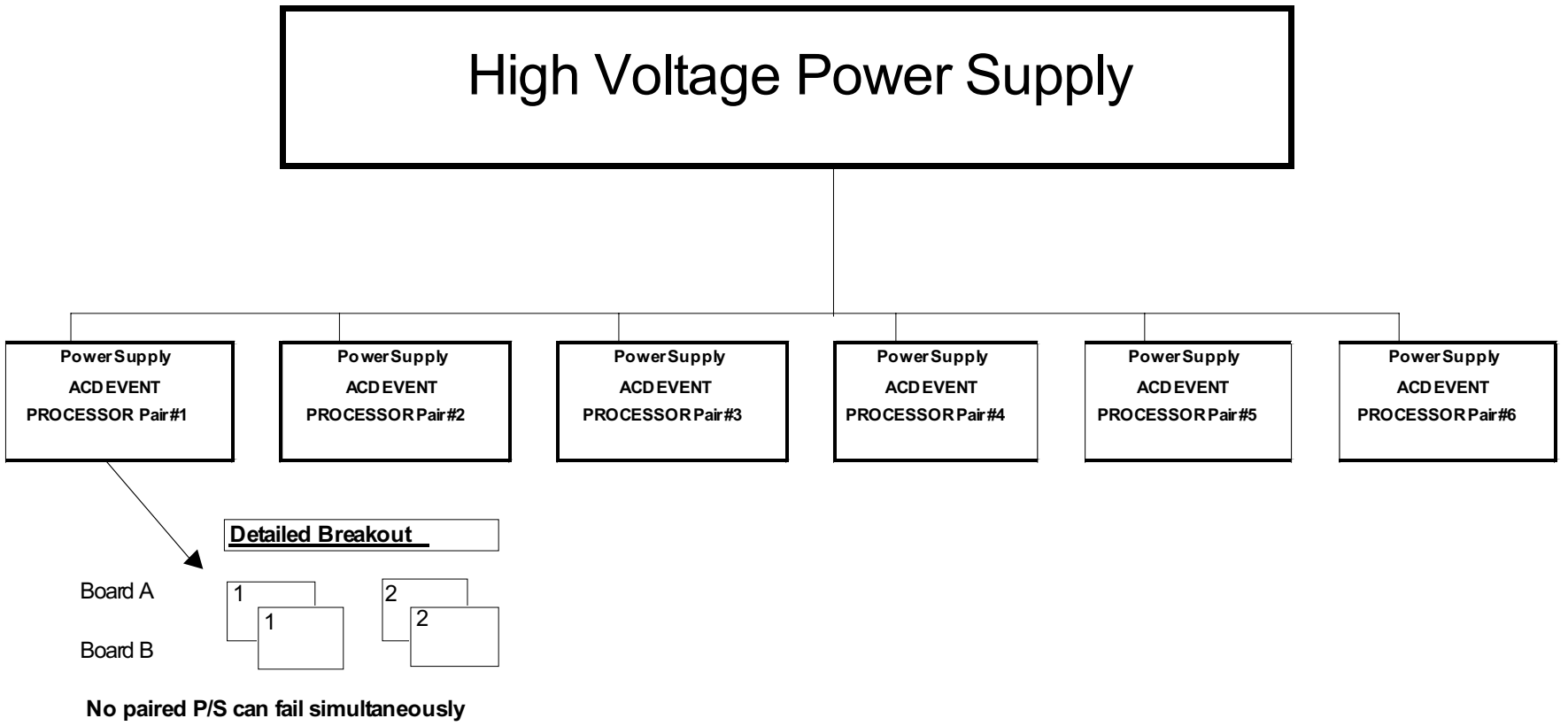
ACD - HVPS Failure 3.79E-01 failures/10 ^{6} hours *Translates into 3.32E-03 failures/year*

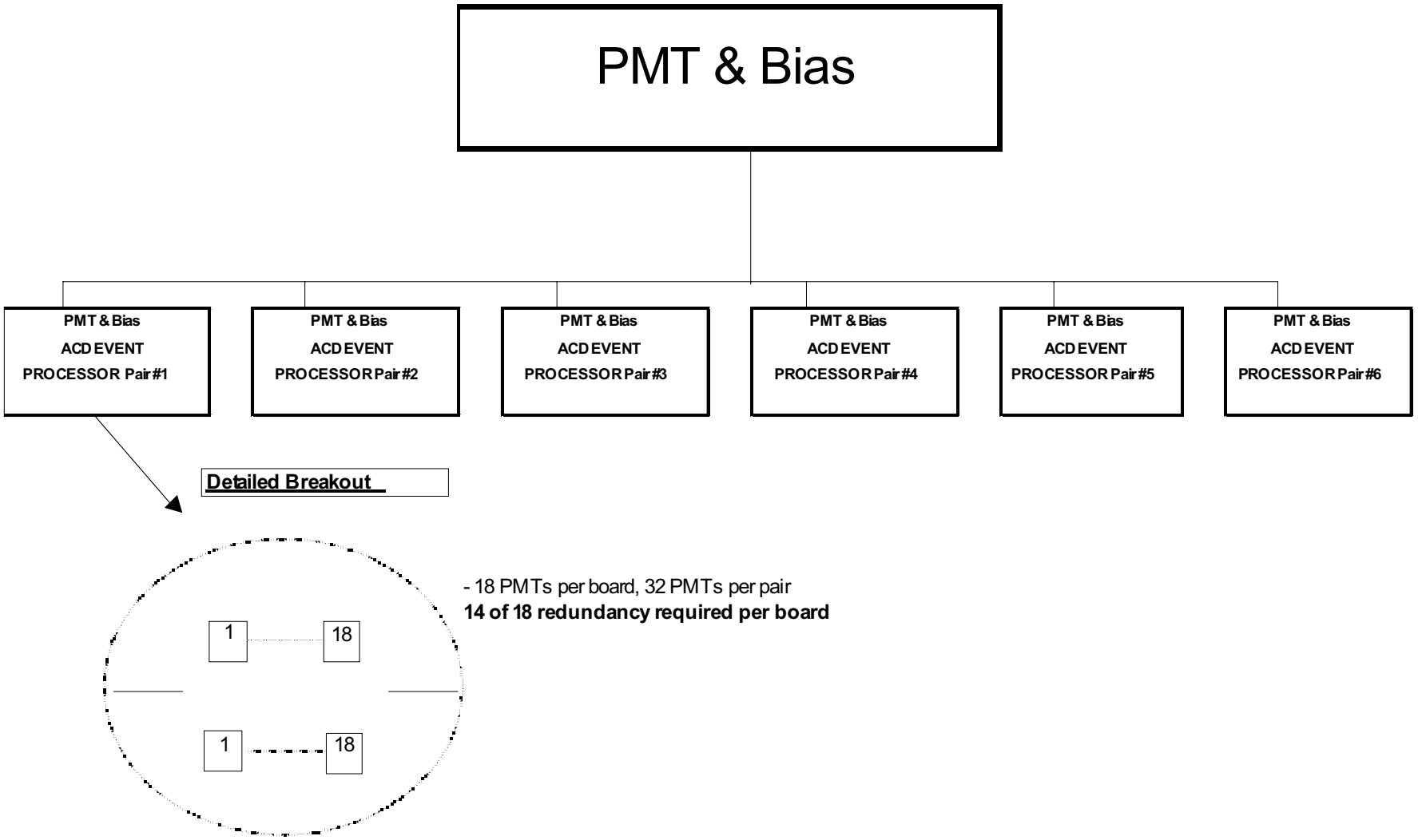
MTBF - Years/failure 301.20

Hours/Year	8760
Transistor, NPN	**ST1, ST2**
Years/Failure	146917.96
L_P_Total (fail/10 ^{6} hours)	7.77E-04
Quanity	3
L_g (fail/10 ^{6} hours)	7.40E-04
PI_Q	7.00E-01
PI_E	5.00E-01
Switching/Zenor Diode	**ST3, ST4**
Years/Failure	15531.33
L_P_Total (fail/10 ^{6} hours)	7.35E-03
Quanity	7
L_g (fail/10 ^{6} hours)	3.00E-03
PI_Q	7.00E-01
PI_E	5.00E-01
High Voltage Diode	**ST5**
Years/Failure	415.11
L_P_Total (fail/10 ^{6} hours)	2.75E-01
Quanity	20
L_g (fail/10 ^{6} hours)	5.00E-03
PI_Q	5.50E+00
PI_E	5.00E-01
Op Amp	**ST6**
Years/Failure	3004.09
L_P_Total (fail/10 ^{6} hours)	3.80E-02
Quanity	1
L_g (fail/10 ^{6} hours)	3.80E-02
PI_Q	1.00E+00
PI_E	1.00E+00
RM1206 Resistor	**ST7**
Years/Failure	24682.22
L_P_Total (fail/10 ^{6} hours)	4.63E-03
Quanity	25
L_g (fail/10 ^{6} hours)	3.70E-03
PI_Q	1.00E-01
PI_E	5.00E-01

Hours/Year	8760
Capacitor, Ceramic	**ST8**
Years/Failure	11891171.99
L_P_Total (fail/10 ^{6} hours)	9.60E-06
Quanity	8
L_g (fail/10 ^{6} hours)	2.40E-03
PI_C	1.00E-03
PI_S	5.00E-01
HV Resistor	**ST9**
Years/Failure	1585489.60
L_P_Total (fail/10 ^{6} hours)	7.20E-05
Quanity	2
L_g (fail/10 ^{6} hours)	2.40E-03
PI_Q	3.00E-02
PI_E	5.00E-01
Inductor MPP Core	**ST10**
Years/Failure	253678335.87
L_P_Total (fail/10 ^{6} hours)	4.50E-07
Quanity	1
L_g (fail/10 ^{6} hours)	3.00E-05
PI_Q	3.00E-02
PI_E	5.00E-01
Transformer, CM	**ST11**
Years/Failure	21139.86
L_P_Total (fail/10 ^{6} hours)	5.40E-03
Quanity	1
L_g (fail/10 ^{6} hours)	5.40E-03
PI_Q	1.00E+00
PI_E	5.00E-01
Transformer, Pulse	**ST12**
Years/Failure	3.03E+09
L_P_Total (fail/10 ^{6} hours)	1.10E-02
Quanity	1
L_g (fail/10 ^{6} hours)	2.20E-02
PI_Q	1.00E+00
PI_E	5.00E-01

Hours/Year	8760
Transformer, Osc.	**ST13**
Years/Failure	4659.40
L_P_Total (fail/10 ^{6} hours)	2.45E-02
Quanity	1
L_g (fail/10 ^{6} hours)	4.90E-02
PI_Q	1.00E+00
PI_E	5.00E-01
Capacitor, Tantalum	**ST14**
Years/Failure	475646.88
L_P_Total (fail/10 ^{6} hours)	2.40E-04
Quanity	1
L_g (fail/10 ^{6} hours)	4.00E-04
PI_C	1.20E+00
PI_E	5.00E-01
Capacitor, HV 20pF	**ST15**
Years/Failure	329452.38
L_P_Total (fail/10 ^{6} hours)	3.47E-04
Quanity	2
L_g (fail/10 ^{6} hours)	9.90E-04
PI_C	3.50E-01
PI_E	5.00E-01
Capacitor, HV 6800pF	**ST16**
Years/Failure	10676.70
L_P_Total (fail/10 ^{6} hours)	1.07E-02
Quanity	20
L_g (fail/10 ^{6} hours)	9.90E-04
PI_C	5.40E-01
PI_E	5.00E-01
Capacitor, HV 6800pF	**ST17**
Years/Failure	8.42E+08
L_P_Total (fail/10 ^{6} hours)	9.90E-04
Quanity	2
L_g (fail/10 ^{6} hours)	9.90E-04
PI_C	5.40E-01
PI_E	5.00E-01


High Voltage Power Supply
Power Supply ACD EVENT PROCESSOR Pair#1
Power Supply ACD EVENT PROCESSOR Pair#2
Power Supply ACD EVENT PROCESSOR Pair#3
Power Supply ACD EVENT PROCESSOR Pair#4
Power Supply ACD EVENT PROCESSOR Pair#5
Power Supply ACD EVENT PROCESSOR Pair#6
Detailed Breakout
Board A
Board B
1
1
2
2
No paired P/S can fail simultaneously


PMT & Bias
PMT & Bias ACD EVENT PROCESSOR Pair #1
PMT & Bias ACD EVENT PROCESSOR Pair #2
PMT & Bias ACD EVENT PROCESSOR Pair #3
PMT & Bias ACD EVENT PROCESSOR Pair #4
PMT & Bias ACD EVENT PROCESSOR Pair #5
PMT & Bias ACD EVENT PROCESSOR Pair #6
Detailed Breakout
1
18
1
18
- 18 PMTs per board, 32 PMTs per pair
14 of 18 redundancy required per board