	Document # **LAT-TD-00429-D2**	Date Effective 12/06/01
	Prepared by George Shiblie	Supersedes None
GLAST LAT TECHNICAL REPORT	Subsystem/Office Anticoincidence Detector Subsystem	
Document Title **LAT Anticoincidence Detector Subsystem Preliminary Design Report**		

Gamma-ray Large Area Space Telescope (GLAST)

Large Area Telescope (LAT)

Anticoincidence Detector (ACD) Subsystem Preliminary Design Report

CHANGE HISTORY LOG

Revision	Effective Date	Description of Changes	DCN #
1	12/06/01	Initial Release	

Table of Contents

1 Purpose 7
2 Acronyms and Definitions 7
2.1 Definitions 9
3 Applicable Documents 11
3.1 ACD Specifications 11
3.2 GLAST References 11
3.3 LAT and ACD Supporting Documentation 12
3.4 GSFC Procedure and Guidelines 12
3.5 Publications 12
3.6 ACD Drawings 12
4 Introduction 13
4.1 LAT Science Requirements 13
4.2 LAT Technical Description 13
4.3 ACD Design Overview 14
5 ACD Subsystem Organization 14
6 ACD Subsystem WBS 15
7 ACD Subsystem Deliverables and Receivables 17
8 ACD Requirements and Specifications 18
9 ACD Development and Prototyping 19
10 ACD Subsystem Design 23
10.1 Detector Design 23
10.2 Mechanical Design 26
10.3 Thermal Design 38
10.4 Electronics Design 40
11 ACD Subsystem Interface Description 49
11.1 Mechanical and Thermal Interface Control 49
11.2 Electrical Interface Control 49
12 ACD Safety and Mission Assurance 50
12.1 Reliability 50
12.2 Parts and Materials 52
12.3 Quality Control and Work Order Authorization (WOA) 54
12.4 Safety 55
12.5 Contamination Control 56
13 ACD Assembly, Integration and Test 56
13.1 Key Mechanical Components Assembly Flow 57
13.2 Key Electrical Components Assembly Flow 58
13.3 Integration and Test 60
13.4 Ground Support Equipment 62
14 ACD Key Milestones and Schedule 64
14.1 Key Level III and Level IV Milestones 64
14.2 Schedule 65

List of Figures

Figure 1. View of the LAT Science Instrument with one Tracker tower module and one Calorimeter module pulled away from the Grid. GLAST is a 4 × 4 array of identical Tracker and Calorimeter modules and the ACD tile cover. 13
Figure 2. ACD Subsystem Organization 15
Figure 3. Fraction of events giving a backsplash signal as a function of incident photon energy and ACD threshold. Black dots: results from 1997 SLAC test. Red and blue dots: results from two separate runs at CERN in 1999 20
Figure 4. Three of the scintillator tiles with waveshifting fiber readout produced for the 1999 beam test. 20
Figure 5. The ACD for the Beam Test Engineering Model (BTEM). Left: individual wrapped tiles and phototubes mounted on a support structure. Center: one of the electronics cards. Right: the full ACD with its light shield. 21
Figure 6. Pulse height spectra from the 13 ACD tiles on the BFEM. In all cases, the signal peak due to charged particles is cleanly separated from the noise 21
Figure 7. The overall layout of the GLAST LAT ACD system, showing the scintillator tile placement. 23
Figure 8. Block diagram of the active ACD detector system. 23
Figure 9. Scintillator tile with waveshifting fibers in the flight design. Alternate fibers are routed to separate phototubes for redundancy. 24
Figure 10. Pulse height distributions of muons from four phototubes 25
Figure 11. Efficiency for flight prototype tiles. 25
Figure 12. Technique for sealing gaps on the top surface of the ACD. The ribbons are made of square scintillating fibers. 25
Figure 13. ACD Assembly with Exploded View 27
Figure 14. Base Electronics Assembly 28
Figure 15. BEA Corner Mount 28
Figure 16. BEA Center Mount Side View 29
Figure 17. BEA Center Mount Front View 29
Figure 18. Tile Shell Assembly 29
Figure 19. Shell Assembly with Flexures 30
Figure 20. TDA Tie-down Orientation 30
Figure 21. Key Hole Groove 31
Figure 22. Flat and Bent Tile Assembly 31
Figure 23. Clear Fiber Connector 32
Figure 24. PMT Fiber Connector 32
Figure 25. Finite Element Model 33
Figure 26. Corner Boundary Condition 35
Figure 27. Mid-Side Boundary Condition 35
Figure 28. Second Mode Shape 37
Figure 29. First Mode Shape 37
Figure 30. Exterior MLI 39
Figure 31. Towers and Grid 39
Figure 32. ACD Electrical System Block Diagram 41
Figure 33. Analog ASIC Design 42
Figure 34. Power Distribution 44

Figure 35. Digital ASIC Block Diagram 46
Figure 36. HVBS Block Diagram 46
Figure 37. HVBS Schematic 47
Figure 38. PMT Biasing Circuitry 48
Figure 39. Reliability Allocation and Apportionment 52
Figure 40. Power Supply Reliability Tradeoff Study 53
Figure 41. Typical Corner Joint 57
Figure 42. ACD Subsystem Integration and Test Flow 61

List of Tables

Table 1. ACD Subsystem Work Breakdown Structrure....15
Table 2. ACD Subsystem Level III Key Requirements....18
Table 3. ACD Mass Allocation.....18
Table 4. ACD Power Allocation....18
Table 5. Percent Radiation Absorbed....27
Table 6. Material Properties of GLAST components....34
Table 7. Mass Breakdown of ACD Components....34
Table 8. ACD Design Limit Loads (G's)....34
Table 9. Margins of Safety for Corner Fitting....35
Table 10. Margin of Safety of Edge Clips and Flexures....36
Table 11. Deflections under Design Loads....36
Table 12. Modal Frequencies and Effective Masses....37
Table 13. Temperature Predictions....39
Table 14. TSS Optical Properties....40
Table 15. TSS Orbital Parameters....40
Table 16. FMEA 2R Severity Classification Summary....51

1 PURPOSE

This document presents the status of the GLAST LAT ACD subsystem design and planning in support of the January 8-10, 2002 LAT I-PDR.

2 ACRONYMS AND DEFINITIONS

ACD	The LAT Anti-Coincidence Detector Subsystem
ADC	Analog-to-Digital Converter
AEM	ACD Electronics Module
ANSI/AIAA	American National Standards Institute/Aerospace Institute of Aeronautics and Astronautics
ASIC	Application Specific Integrated Circuits
BEA	Base Electronics Assembly
BFEM	Balloon Flight Engineering Model
BTEM	Beam Test Engineering Model
CAL	The LAT Calorimeter Subsystem
CIL	Critical Items List
CMOS	Complementary Metal Oxide Semiconductor
COS-B	European Gamma-ray Astronomy Satellite
CTE	Coefficient of Thermal Expansion
DAQ	Data Acquisition
DOF	Degrees of Freedom
EEE	Electrical, Electronic, and Electromechanical
EGRET	Energetic Gamma-Ray Experiment Telescope
EGSE	Electrical Ground Support Equipment
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
FEM	Fine Element Model
FM	Flight Module
FMEA	Failure Mode Effect Analysis
FREE	Front End Electronics
GAFE	GLAST ACD Front End – Analog ASIC
GARC	GLAST ACD Readout Controller – Digital ASIC

GEVS	General Environmental Verification Specification
GLAST	Gamma-ray Large Area Space Telescope
GOLF	Global Oscillations at Low Frquencies
GUI	Graphic User Interface
HEPA	High Efficiency Particle Air
HLD	High Level Discriminator
HVBS	High Voltage Bias Supply
IC	Integrated Circuit
ICD	Interface Control Document
IDT	Instrument Development Team
I&T	Integration and Test
IRD	Interface Requirements Document
JSC	Johnson Space Center
LAT	Large Area Telescope
MECO	Main Engine Cut-off
MIP	Minimum Ionizing Particle
MGSE	Mechanical Ground Support Equipment
MLI	Multi-Layer Insulation
MOSIS	Metal Oxide Semiconductor Implementation System
MPLS	Multi-purpose Lift Sling
NPSL	NASA Parts Selection List
PAIP	Performance Assurance Implementation Plan
PAPL	Program Approved Parts List
PCB	Printed Circuit Board
PDR	Preliminary Design Review
PHA	Pulse Height Analysis
PMT	Photomultiplier Tube
PPCP	Parts Program Control Plan
PPL	Preferred Parts List
P&SA	Performance and Safety Assurance
PVM	Performance Verification Matrix
QA	Quality Assurance
RXTE	Rossi X-Ray Timing Explorer
SAM	Safety Assurance Manager
SAS	Science Analysis Software

SCL	Spacecraft Command Language
SEL	Single Event Latch-up
SEU	Single Event Upset
SINDA	Systems Improved Numerical Differencing Analyzer
SLAC	Stanford Linear Accelorator Center
S&MA	Safety and Mission Assurance
SOHO	Solar and Heliospheric Observatory
SRD	Science Requirements Document
SRR	System Requirements Review
SSC	Science Support Center
SSPP	System Safety Program Plan
TACK	Trigger Acknowledge
TDA	Tile Detector Assembly
T&DF	Trigger and Data Flow Subsystem (LAT)
TID	Total Ionizing Dose
TBD	To Be Determined
TBR	To Be Resolved
TQFP	Thin Quad Flat Package
TSA	Tile Shell Assembly
TSS	Thermal Synthesizer System
TKR	The LAT Tracker Subsystem
VME	Versa Module Eurocard
WBS	Work Breakdown Structure
WSB	Wave Shifting Bars
WSF	Wave Shifting Fibers
WOA	Work Order Authorization

2.1 Definitions

γ	Gamma Ray
μsec, μs	Microsecond, 10^{-6} second
A_{eff}	Effective Area
Analysis	A quantitative evaluation of a complete system and /or subsystems by review/analysis of collected data.
Background Rejection	The ability of the instrument to distinguish gamma rays from charged particles.
Backsplash	Secondary particles and photons originating from very high-energy gamma-

	ray showers in the calorimeter giving unwanted ACD signals.
Beam Test	Test conducted with high energy particle beams
cm	centimeter
Cosmic Ray	Ionized atomic particles originating from space and ranging from a single proton up to an iron nucleus and beyond.
Dead Time	Time during which the instrument does not sense and/or record gamma ray events during normal operations.
Demonstration	To prove or show, usually without measurement of instrumentation, that the project/product complies with requirements by observation of results.
eV	Electron Volt
Field of View	Integral of effective area over solid angle divided by peak effective area.
g	unit of gravitational acceleration, $g = 9.81\ m/s^2$
Geometric factor	Field of View times Effective Area
GeV	Giga Electron Volts. 10^9 eV
Inspection	To examine visually or use simple physical measurement techniques to verify conformance to specified requirements.
MeV	Million Electron Volts, 10^6 eV
ph	photons
s, sec	seconds
Simulation	To examine through model analysis or modeling techniques to verify conformance to specified requirements
Testing	A measurement to prove or show, usually with precision measurements or instrumentation, that the project/product complies with requirements.
Validation	Process used to assure the requirement set is complete and consistent, and that each requirement is achievable.
Verification	Process used to ensure that the selected solutions meet specified requirements and properly integrate with interfacing products.

3 APPLICABLE DOCUMENTS

The documents listed in Section 3.1 are primary to the organization and specification of the LAT ACD subsystem and its interfaces. References in Sections 3.2 through 3.3 provide key references, test specifications, plans and procedures, and other technical documentation relevant to the design of the ACD.

Documents that are relevant to the development of the GLAST mission concept and its requirements include the following:

3.1 ACD Specifications

1. LAT-SS-00016, LAT ACD Subsystem Requirements – Level III Specification
2. LAT-SS-00352, LAT ACD Electronics Requirements – Level IV Specification
3. LAT-SS-00437, LAT ACD Mechanical Requirements – Level IV Specification
4. LAT-SS-00448, LAT ACD Electronics Subsystem Specification
5. LAT-SS-00449, LAT ACD Mechanical Subsystem Specification
6. LAT-TD-00438, Light Collection/Optical Performance Tests
7. LAT-TD-00435, LAT ACD Grounding and Shielding Plan
8. LAT-MD-00039-01, LAT Performance Assurance Implementation Plan (PAIP)
9. LAT-MD-00099-002, LAT EEE Parts Program Control Plan
10. LAT-SS-00107-1, LAT Mechanical Parts Plan
11. LAT-MD-00078-01, LAT System Safety Program Plan (SSPP)
12. LAT-TD-00430, LAT ACD Assembly, Integration, and Test
13. ACD-QA-8001, ACD Quality Plan
14. ACD-RPT-12001, FMEA & CIL
15. ACD-RPT-1250, Limited-Life Items List
16. ACD-REQ-7002, Requirements for ACD MGSE

3.2 GLAST References

17. Response to AO 99-OSS-03. "GLAST Large Area Telescope, Flight Investigation: An Astro-Particle Physics Partnership Exploring the High-Energy Universe." Volume 1: Scientific and Technical Plan. Foldouts: A, B, C, D.
18. GSFC 433-SRD-0001, "GLAST Science Requirements Document", P.Michelson and N.Gehrels, eds., July 9, 1999
19. LAT-SS-00010, "LAT Instrument Performance Specification."
20. GSFC 433-SPEC-001, "GLAST Project Mission System Specification," April 24, 2001
21. GSFC 433-IRD-0001, "GLAST Science Instrument – Spacecraft Interface Requirements Document", Draft July 14, 2000
22. GSFC 433-MAR-0001, "Mission Assurance Requirements (MAR) for Gamma-Ray Large Area Telescope (GLAST) Large Area Telescope (LAT)", June 9, 2000
23. GSFC 433-RQMT-0005, "GLAST EMI Requirements Document."
24. GSFC 433-OPS-0001, "GLAST Operations Concept", Sept 7, 2000
25. LAT-SS-00047, "LAT Mechanical Performance Specification."
26. LAT-MD-00099, "LAT EEE Parts Program Control Plan," March 2001
27. LAT-MD-00039, LAT Performance Assurance Implementation Plan

28. LAT-MD-00033, "LAT Work Breakdown Structure," May 9, 2001
29. LAT-TD-00125, "LAT Mass and Power Allocation Recommendations"
30. "Gamma Ray Large Area Space Telescope Instrument Technology Development Program", NRA 98-217-02, NASA Office of Space Science, January 16, 1998.

3.3 LAT and ACD Supporting Documentation

31. LAT-SS-00363, LAT Dataflow Subsystem Specification – ACD-TEM Interface
32. LAT-DS-00241, LAT Mechanical Systems – ACD to Grid Interface Control Description

3.4 GSFC Procedure and Guidelines

33. GPG-5340.3, Preparation and Handling of Alerts and Safe Alerts
34. GPG-5330.1, Product Processing, Inspection and Test
35. GPG-8621.1, Mishap, Incident, and Close Call Investigation
36. 302-PG-1410.2.1, Goddard Non-Conformance Reporting and Corrective Action System Configuration Control Board (CCB)

3.5 Publications

37. W.B.Atwood et al., NIM A446 (2000), 444
38. do Couto e Silva et al., NIM A474/1 (2001), 19

3.6 ACD Drawings

39. GE2054500, ACD Assembly Drawing

4 INTRODUCTION

GLAST is a next generation high-energy gamma-ray observatory designed for making observations of celestial gamma-ray sources in the energy band extending from 20 MeV to more than 300 GeV. It follows in the footsteps of the Compton Gamma Ray Observatory EGRET experiment, which was operational between 1991-2000. The GLAST Mission is part of NASA's Office of Space and Science Strategic Plan, with launch anticipated in 2006. The principal instrument of the GLAST mission is the Large Area Telescope (LAT) that is being developed jointly by NASA and the US Dept. of Energy (DOE) and is supported by an international collaboration of 26 institutions led by Stanford University.

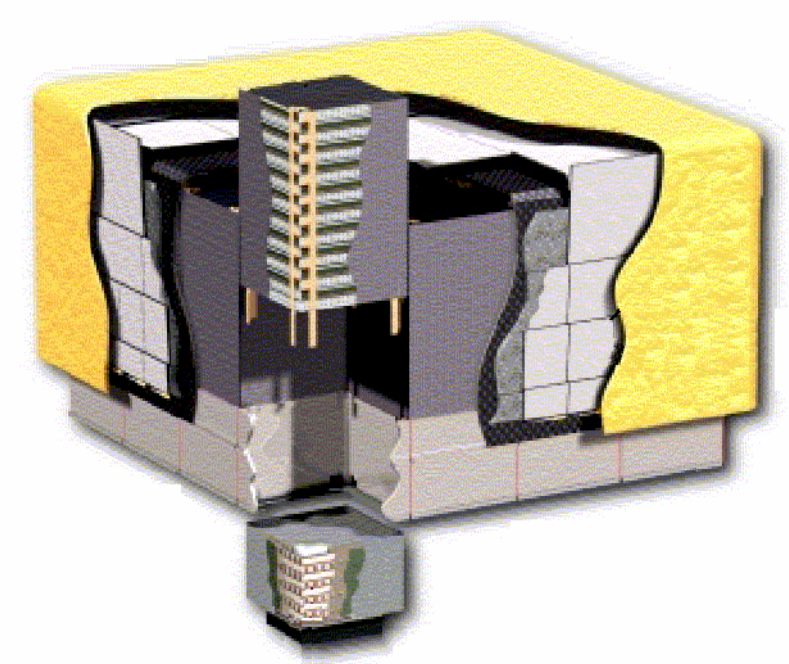


Figure 1. View of the LAT Science Instrument with one Tracker tower module and one Calorimeter module pulled away from the Grid. GLAST is a 4 × 4 array of identical Tracker and Calorimeter modules and the ACD tile cover.

The GLAST LAT is a high-energy pair conversion telescope that has been under development for over 7 years with support from NASA, DOE and international partners. It consists of a precision converter-tracker, CsI hodoscopic calorimeter, plastic scintillator anticoincidence system and a data acquisition system. The design is modular with a 4 × 4 array of identical tracker and calorimeter modules. The modules are ~ 38 x 38 cm. Figure 1 shows the LAT instrument concept.

4.1 LAT Science Requirements

The GLAST science requirements are given in Reference 18. An updated set of requirements, as they pertain to the LAT science instrument, is specified in Reference 19. General constraints and requirements on the instrument design are specified in GLAST mission documents (References 20, 21 and 24). The flowdown of the science requirements and instrument constraints to the LAT design is summarized in Foldout-D of our NASA proposal (Reference 17).

4.2 LAT Technical Description

The LAT science instrument consists of an Anti Coincidence Detector (ACD), a silicon-strip detector Tracker (TKR), a hodoscopic CsI Calorimeter (CAL), and a Trigger and Data Flow system (T&DF). The principal purpose of the LAT is to measure the incidence direction, energy and time of cosmic gamma rays while rejecting background from charged cosmic rays and atmospheric albedo gamma rays and particles. The data, filtered by onboard software “triggers”, are streamed to the spacecraft for data storage and subsequent transmittal to ground-based analysis centers. The Tracker provides the principal trigger for the LAT, converts the gamma rays into electron-positron pairs, and measures

the direction of the incident gamma ray from the charged-particle tracks. It is crucial in the first levels of background rejection for providing track information to extrapolate cosmic-ray tracks to the ACD scintillator tiles, and it is important for further levels of background analysis due to its capability to provide highly detailed track patterns in each event.

4.3 ACD Design Overview

The primary task of the GLAST ACD is to detect energetic cosmic ray electrons and nuclei for the purpose of removing these backgrounds. It is the principal source for detection of other than gamma-ray particles. This detector element covers the Tracker. It consists of an array of 89 plastic scintillator tiles (1 cm thick, various sizes), plus eight (8) scintillating fiber "ribbons" that cover the gaps between the tiles. Signals produced by the ACD are used by the T&DF system to identify cosmic ray electrons and nuclei entering the instrument.

5 ACD SUBSYSTEM ORGANIZATION

NASA Goddard Space Flight Center (NASA/ GSFC) has the overall responsibility for the ACD Subsystem by direction of Peter F. Michelson, the Instrument Principal Investigator (IPI). GSFC's responsibility to NASA is identified, with management oversight and concurrence from P.F. Michelson.

David Thompson of GSFC, ACD Subsystem Manager, has overall responsibility for the ACD Subsystem of the GLAST LAT instrument. The ACD Instrument Manager, Thomas Johnson, performs the project management. The ACD design and development is done at the NASA Goddard Space Flight Center (NASA/ GSFC). Figure 2 shows the organization of the ACD program.

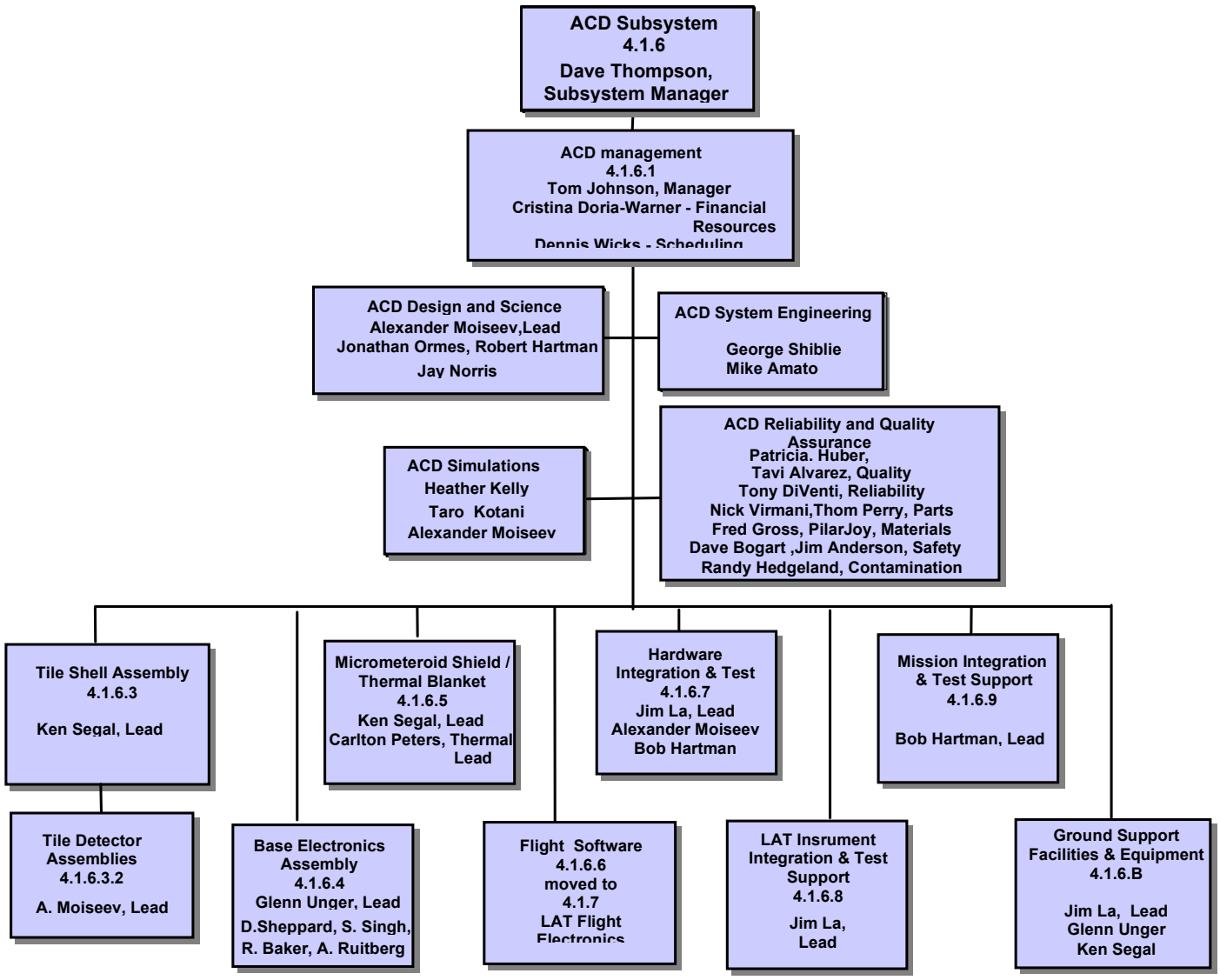


Figure 2. ACD Subsystem Organization

6 ACD SUBSYSTEM WBS

Table 1 provides a top-level summary of the ACD WBS to Level 5.

Table 1. ACD Subsystem Work Breakdown Structrure

WBS	Task
4.1.6	ACD
4.1.6.1	ACD Management
4.1.6.1.1	Project Management
4.1.6.1.2	System/Subsystem Engineering
4.1.6.1.3	Science Support
4.1.6.1.4	Simulations

WBS	Task
4.1.6.2	Reliability and Quality Assurance
4.1.6.2.1	Reliability
4.1.6.2.2	Safety
4.1.6.2.3	Flight Assurance
4.1.6.2.4	Parts Control
4.1.6.2.5	Materials
4.1.6.3	Tile Shell Assembly (TSA)
4.1.6.3.1	Tile Shell Assembly (TSA) Analysis/Design
4.1.6.3.2	Tile Detector Assemblies (TDAs)
4.1.6.3.3	Shell Subassembly
4.1.6.3.4	Tile Mounting Hardware & Assemblies
4.1.6.3.5	Reserved
4.1.6.3.6	Reserved
4.1.6.3.7	Cal Unit components I&T
4.1.6.3.8	Flight Model TSA I&T
4.1.6.4	Base Electronics Assembly (BEA)
4.1.6.4.1	Base Electronics Assembly (BEA) Analysis/Design
4.1.6.4.2	BEA Base Frame Electronics Assembly
4.1.6.4.3	High Voltage Power Supply Analysis/Procurement
4.1.6.4.4	Analog ASIC Design/Procurement
4.1.6.4.5	Digital ASIC Design/Procurement
4.1.6.4.6	Front-Ent Electronics and Event (FREE) Circuit Card Assembly (CCA)
4.1.6.4.7	Reserved
4.1.6.4.8	Reserved
4.1.6.4.9	BEA Electronics Mounting/Assembly Hardware
4.1.6.4.A	Reserved
4.1.6.4.B	Reserved
4.1.6.4.C	Cal Unit BEA I&T
4.1.6.4.D	Flight Model BEA I&T
4.1.6.4.E	Photo-Multiplier Tubes (PMT) & Divider Assembly
4.1.6.5	Micrometeoroid Shield/Thermal Blanket Assembly
4.1.6.5.1	Micrometeoroid Shield/Thermal Blanket Assembly
4.1.6.5.2	Micrometeoroid Shield/Thermal Blanket Assembly Mounting/Assembly H/W
4.1.6.5.3	Reserved
4.1.6.5.4	Reserved
4.1.6.5.5	Reserved
4.1.6.5.6	Micrometeoroid Shield/Thermal Blanket Assembly Flight Unit I&T
4.1.6.6	Reserved
4.1.6.7	Hardware/ Software Integration & Test
4.1.6.7.1	Miscellaneous LAT Interface/Assembly Hardware
4.1.6.7.2	Reserved

WBS	Task
4.1.6.7.3	Reserved
4.1.6.7.4	Calibration Model Hardware/Software I&T
4.1.6.7.5	Flight Model Hardware/Software I&T
4.1.6.8	LAT Instrument Integration & Test
4.1.6.8.1	Reserved
4.1.6.8.2	Reserved
4.1.6.8.3	Cal Unit I&T w/LAT (Support)
4.1.6.8.4	Flight Unit I&T w/LAT (Support)
4.1.6.9	Mission Integration and Test Support
4.1.6.9.1	LAT Flight Unit I&T w/Spacecraft (Support)
4.1.6.9.2	Reserved
4.1.6.A	Reserved
4.1.6.B	Ground Support Facilities & Equipment
4.1.6.B.1	Reserved
4.1.6.B.2	Mechanical Ground Support Equipment
4.1.6.B.3	Electrical Ground Support Equipment
4.1.6.B.4	Front End Electronics and Event (FREE) Circuit Card Assembly (CCA) Test Set

7 ACD SUBSYSTEM DELIVERABLES AND RECEIVABLES

The ACD Subsystem deliverables and receivables due dates are documented in the ACD schedule.

The ACD subsystem will deliver the following items to the project:

1. One (1) ACD Subsystem FLIGHT Unit
2. One (1) DAQ I/F test unit (test screening board with digital ASIC) – delivered to T&DF for ACD Electronics Module (AEM) Development
3. The parts necessary to assemble 12 Front End Electronics circuit cards (to be assembled at SLAC) – delivered to T&DF for AEM Development.
4. Calibration unit components.
5. ACD mechanical and thermal finite-element models.
6. Mechanical ground support equipment for module handling and installation.
7. Design documentation and as-built documentation for the ACD, including the fabrication database.
8. The ACD operating and handling manual, including test scripts.

The ACD subsystem will receive the following items for the development of the project:

1. Five ACD Electronic Modules (AEM) units with cable interfaces to ACD.
2. Three (3) Front End Workstations with SCL control executive and LabVIEW GUI.
3. AEM operating and handling manuals.
4. AEM timing diagrams that describes every mode of operation.

8 ACD REQUIREMENTS AND SPECIFICATIONS

The ACD Subsystem requirements and specifications are found in the ACD Subsystem Level III Specification (Reference 1 in Section 3.1). It specifies the ACD requirements necessary to meet the overall LAT system performance (Reference 19 in Section 3.2). The ACD Level III Specification was formally reviewed and approved in April, 2001; however, extensive changes have occurred since then because of descoping to ACD. The change version is under review for final approval. Table 2 is a summary of the most important level III requirements.

The ACD Level IV requirements (Reference 2 and 3) are derived for the specific implementation of the LAT ACD and its interface requirements to other LAT subsystems. In this implementation, the major components of the ACD subsystem and their specifications are:

- ACD Electronics Subsystem Specification, LAT-SS-00448, Reference 4
- ACD Mechanical Subsystem Specification, LAT-SS-00449, Reference 5

The resources allocated to the ACD subsystem are documented in Reference 29 and are summarized below. As shown in Table 3, the baseline ACD mass was established at the System Requirements Review at 199.3 kg. Based on ANSI/AIAA standards a reserve of 60.9 kg was identified, but only 5.7 kg of that reserve have been allocated to the ACD. Thus, the ACD is designing to a mass limit of 205 kg. Exceeding this limit requires configuration control board allocation from the mass reserve. The LAT IDT is currently reviewing a formal request to change the allocated mass from 199.3 to 228.2 kg with no change to the reserve.

Table 4 shows a similar summary for the conditioned power allocated to the ACD. The ACD is allocated 31 watts of conditioned power.

Table 2. ACD Subsystem Level III Key Requirements

Parameter	Requirement
Detection of Charged Particles	>0.3 MIP nominally ≥ 0.9997 average detection efficiency over entire area of ACD (excluding bottom row of tiles)
Fast VETO Signal	Logic signal 400-700 nsec after passage of charge paricle
PHA signal	For each phototube, pulse height measurement for each Trigger Acknowledge (TACK) <10MIP, precision of <0.02 MIP or 5% >10MIP, precision of <1 MIP or 2 %
False backsplash VETO rate	< 20% false VETOs due to calorimeter backsplash at 300 GeV
High Threshold (Heavy Nuclei) Detection	> 25MIP detection of highly-ionized particles.
Size	Outside: 1796 x1796 x 1015 mm Inside Grid: 1574 x 1574 x -204.7 mm Inside TKR: 1515.5 x 1515.5 x 650 mm
Mass	< 205 kg
Power	< 31 Watts (conditioned)
Instrument Lifetime	Minimum 5 yrs

Table 3. ACD Mass Allocation.

	Mass (kg)
SRR Est. (Adj.)	199.3
ANSI/ AIAA Reserve Recom'd	60.9
Subsystem Reserve Allocation	5.7
Subsystem Budget Allocation	**205**

Table 4. ACD Power Allocation

	Power (Watts)
SRR Est. (Adj.)	24.1
ANSI/ AIAA Reserve Recom'd	22.0
Subsystem Reserve Allocation	6.9
Subsystem Budget Allocation	**31**

9 ACD DEVELOPMENT AND PROTOTYPING

Plastic scintillator has been used in all previous gamma-ray telescopes for anticoincidence against charged particles; however, segmenting the tiles is a new design. The GLAST LAT design is the first instrument to have the twin requirements of high efficiency for charged particles and low susceptibility to backsplash self-veto. Segmenting the scintillator attacks the backsplash problem but increases the challenge of achieving high efficiency. Unlike a monolithic anticoincidence detector, which has no gaps and uses many phototubes to collect light, a segmented anticoincidence detector may have gaps between segments and can use few phototubes to collect light.

A series of development and trade studies have been carried out in order to verify and optimize the ACD design:

- A trade study of readout techniques led to the conclusion that conventional PMT tubes remained the light collector of choice <http://lhea-glast.gsfc.nasa.gov/gsfc/acd/acdpdr/acdsnsr.pdf>

- A study was conducted to determine the most effective way to collect the light from the scintillator tiles. Wave-shifting bars (WSB) and direct-coupled PMTs were considered as alternatives to the baselined wave-shifting fibers (WSF). Laboratory tests were conducted to compare their light collection responses. The test results conclude that the WSF provide much better uniformity of response and that it is still the best choice. This result was reported in the report on the NASA Technology Development contract.

For the 1997 beam test at SLAC, we built a set of 15 scintillator tiles with waveshifting fiber/photomultiplier readout. These tiles demonstrated the required efficiency and quantified the backsplash generated in the calorimeter. Results were reported in the beam test paper, W.B.Atwood et al., NIM A446 (2000), 444

- A follow-up test of backsplash using the same scintillator tiles was carried out at CERN in 1999, in order to extend the measurement to 300 GeV. The probability of a backsplash signal (seen in Figure 3) is given by the following empirical formula:

$$P_{backsplash} = \left(0.85 \times \frac{0.3}{E_{thr}} + 0.15 \right) \times 10^{-3} \times \frac{A}{144} \times \left(\frac{55}{x + 10} \right)^2 \times E^{0.75}$$

Where **E** is the energy of incident electron/photon in GeV
E_{thr} is the threshold value in units of *mip*
X is the distance from the top of calorimeter
A is area in cm^2
$P_{backsplash}$ is the probability that there was an energy deposition above E_{thr} in 1cm scintillator

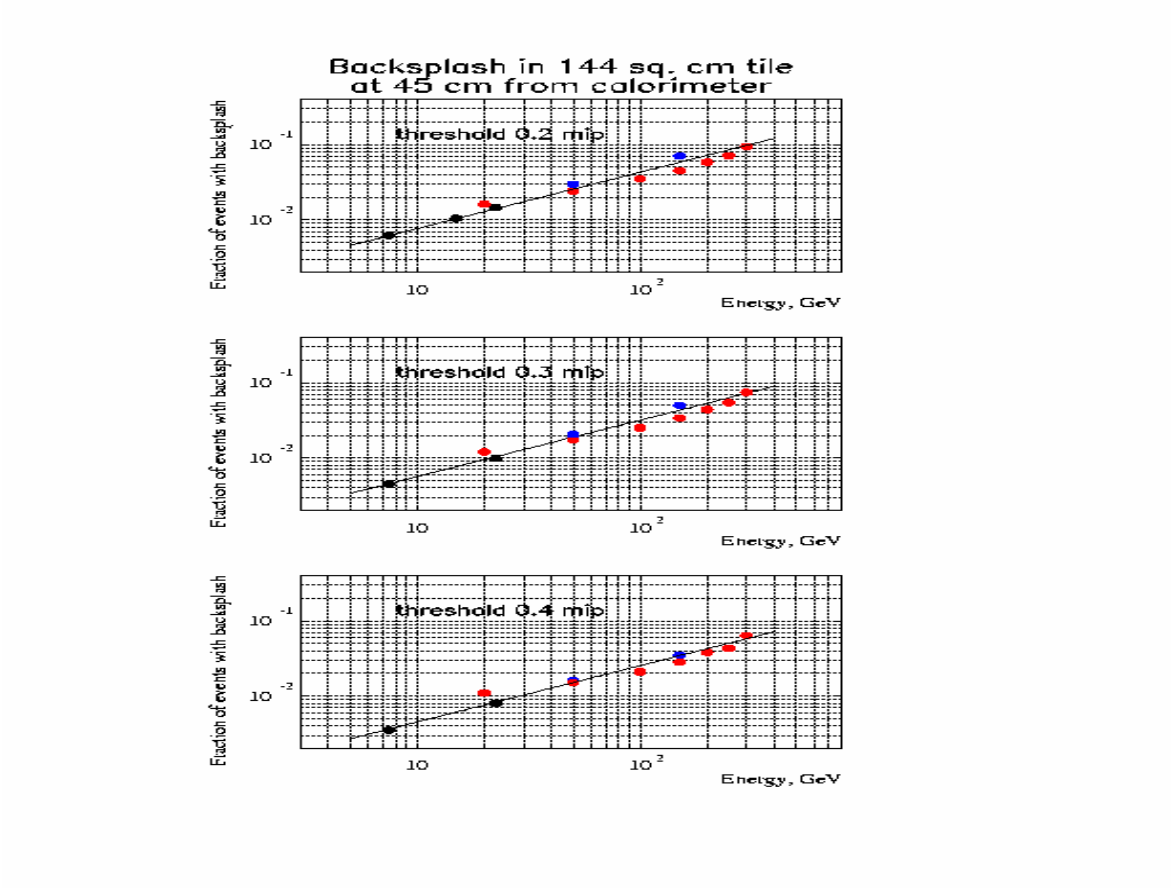


Figure 3. Fraction of events giving a backsplash signal as a function of incident photon energy and ACD threshold. Black dots: results from 1997 SLAC test. Red and blue dots: results from two separate runs at CERN in 1999

- Also in 1999, we built a set of 13 scintillators with waveshifting fiber/photomultiplier readout for a SLAC beam test of a prototype tower. Several different tile/fiber configurations were made, with examples shown in Figure 4. The assembled prototype tower ACD is shown in Figure 5.

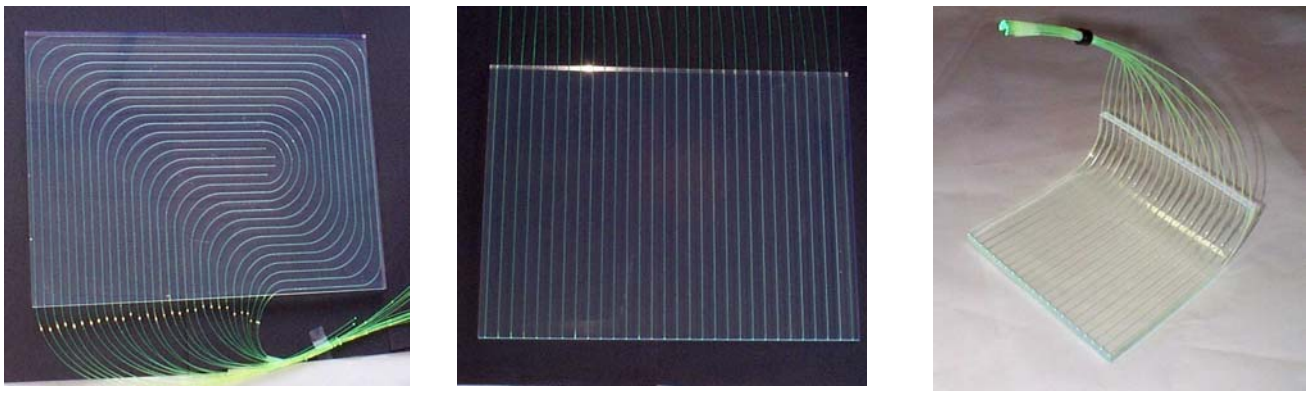


Figure 4. Three of the scintillator tiles with waveshifting fiber readout produced for the 1999 beam test.

Figure 5. The ACD for the Beam Test Engineering Model (BTEM). Left: individual wrapped tiles and phototubes mounted on a support structure. Center: one of the electronics cards. Right: the full ACD with its light shield.

- Results on the ACD from the 1999 beam test were consistent with those found in the previous beam test (do Couto e Silva et al., NIM A474/1 (2001), 19). The same ACD was used for the Balloon Flight Engineering Model (BFEM), where it performed successfully on the August, 2001, balloon flight (Figure 6). Data from that flight are still being analyzed.

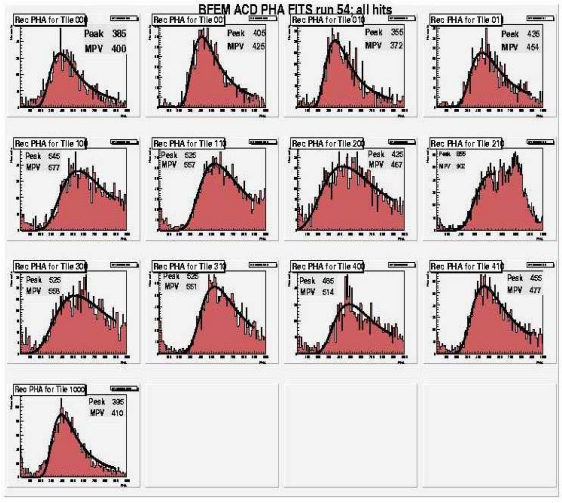


Figure 6. Pulse height spectra from the 13 ACD tiles on the BFEM. In all cases, the signal peak due to charged particles is cleanly separated from the noise

- Several studies have been carried out on the segmentation of the LAT ACD. The effect of backsplash can be reduced with a larger number of smaller tiles, but at a cost of increased complexity and expense. A detailed study, based on simulations, <http://lhea-glast.gsfc.nasa.gov/gsfc/acd/acdpdr/ACD_segmentation.pdf> found that the segmentation could be reduced from the 145 tiles of the AO response to 105 tiles, with minimal loss of performance.

- The effect of gaps between tiles (hermeticity) was studied in detail with simulations. Simple butt joints would require at least 2 mm spacing to allow for thermal expansion, and this spacing is too large to achieve the required overall efficiency of 0.9997. Overlapping the tiles in two dimensions is quite complex to design, build, and test. A one-

dimensional overlap still leaves some gaps, but these could be covered with ribbons made of scintillating fibers. A detailed study <http://lhea-glast.gsfc.nasa.gov/gsfc/acd/acdpdr/ACD_transparency.pdf> found this last option to be attractive.

- The scintillator tile design was carefully studied for the maximization of the light collection. The parameters studied are the following:

  - fiber spacing effect
  - effect of wrapping material - light reflection
  - aluminization of the fiber ends
  - fiber cladding
  - scintillator manufacturer
  - other different designs

We measured the absolute efficiency of a tile of the chosen design and estimate the light yield to be around 35 photoelectrons for two PMT operations, and 19 photoelectrons for single PMT operation. Assuming 15% light loss in the clear fiber extension, the efficiency for single PMT operation will be slightly below the required 0.9997 at the nominal threshold of 0.3 MIP. The default-operating mode must be with both PMT's operating, which provides the required efficiency with margin. We also studied the effect of broken fibers and found that we have good redundancy in the fibers. The minimal requirement for launch is that there must be no tile with more than 4 broken fibers, and no more than 3 tiles in total with broken fibers. To be qualified for assembly into the ACD, a tile may have NO broken fibers. Our 4 years' experience working with these detectors provide confidence that, with proper handling of the tiles, there should not be any occurrence of broken fibers.

Results from these studies are documented in LAT-TD-00438, “Light Collection/Optical Performance Tests”.

Wherever possible, these design and trade studies were backed up with measurements of test articles, either in the laboratory or in one of the LAT tower prototypes. In particular, More than 45 different tile prototypes with WSF readout have been fabricated by us since 1997. Also, a fiber ribbon prototype was built and tested demonstrating at least 6 photoelectrons as required. The result of this work is the design described in the following section.

10 ACD SUBSYSTEM DESIGN

10.1 Detector Design

.

An overview of the ACD detector assembly is shown in Figure 7, and a block diagram of the readout is shown in Figure 8. The following paragraphs will describe the specifics of the detector design, starting with the overall configuration and then working through the specific detector elements

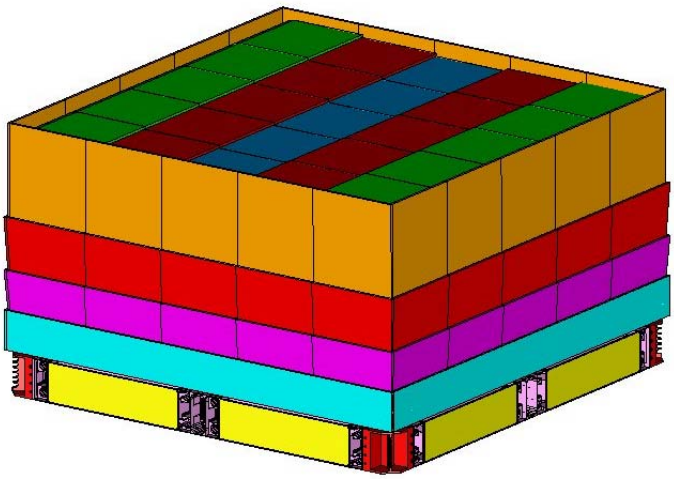


Figure 7. The overall layout of the GLAST LAT ACD system, showing the scintillator tile placement.

10.1.1 Segmentation

The ACD segmentation was optimized by evaluating the effective area and geometric factor degradation for high-energy (300 GeV) photons. Taking into account the fact that the first tracker tray with the radiator is situated at >18cm from the calorimeter, we considered those events which enter the ACD side at least 15 cm from the ACD bottom (calorimeter top). With this approach we were able to reduce the number of tiles from 145 to 89, with only a few percent loss in effective area. The final segmentation of active area on the sides is 3 rows of 5 tiles each, plus a bottom row consisting of a single tile. The reduced segmentation design for the ACD is 5 by 5 tiles on the top and 16 tiles on each side (89 tiles in total).

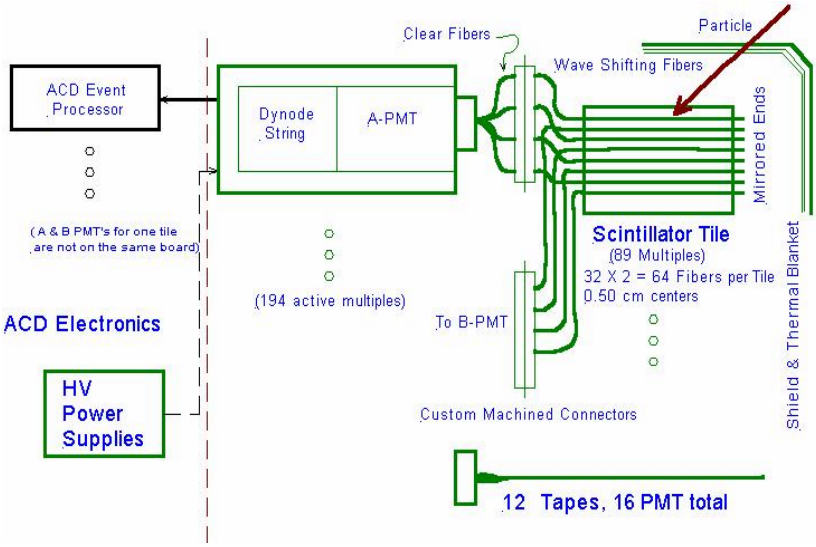


Figure 8. Block diagram of the active ACD detector system.

10.1.2 Scintillator Tile Design

The chosen design is (example shown in Figure 9):

- 1 cm thick plastic scintillator (BC-408 or ElJen 200)
- 5 mm spaced, 1.6 mm deep straight grooves
- 1 mm diameter BCF-91A/MC wave-shifting multiclad fibers (WSF) glued into grooves by BC-600 optical cement
- High light reflecting TETRATEC wrapping
- Aluminized fiber ends
- Clear 1.2 mm diameter fibers BCF-98, connected to WSF near the tile, to bring the light to the PMT with minimal light loss (for the longest bundles, the use of waveshifting fibers for the entire length would result in a 30-40% light loss due to absorption; the connection to the clear fibers has a 15% light loss, but the clear fibers themselves add essentially no additional light loss).

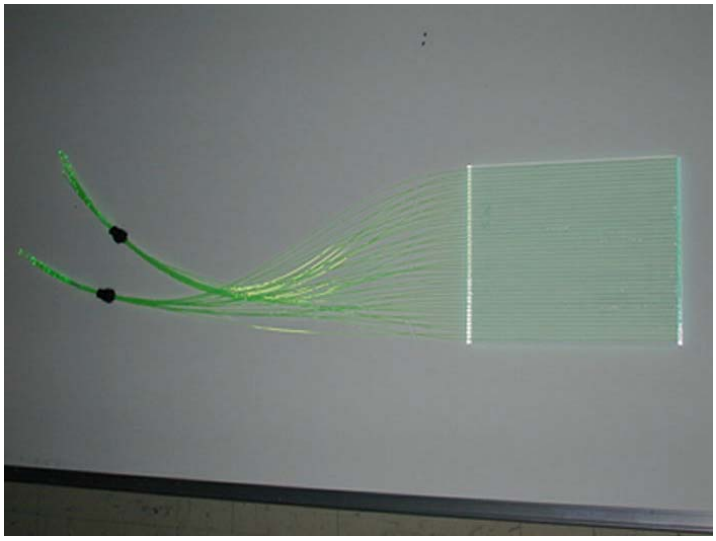


Figure 9. Scintillator tile with waveshifting fibers in the flight design. Alternate fibers are routed to separate phototubes for redundancy.

Performance of two tiles (four phototubes) with this design was verified in the laboratory using atmospheric muons. Figure 10 shows pulse height distributions of muon signals from four phototubes attached to waveshifting fiber bundles from two scintillator tiles. The characteristic Landau distribution is clearly seen, along with the fact that few signals fall below the lower end of the distribution. Figure 11 shows detection efficiency as a function of threshold for the individual phototubes and combinations. The required 0.9997 efficiency can be met with a threshold of 0.3 MIP (minimum ionizing particle). If required, higher efficiency could be achieved with a lower threshold or by combining signals from the two tubes.

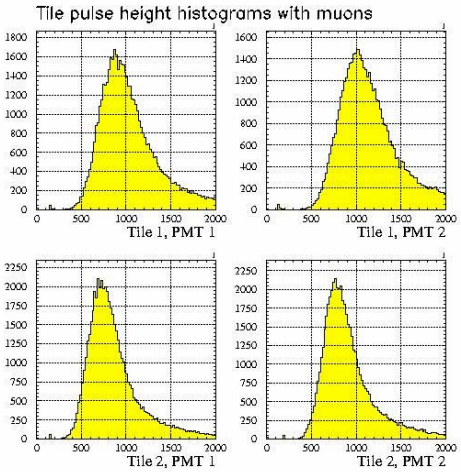


Figure 10. Pulse height distributions of muons from four phototubes

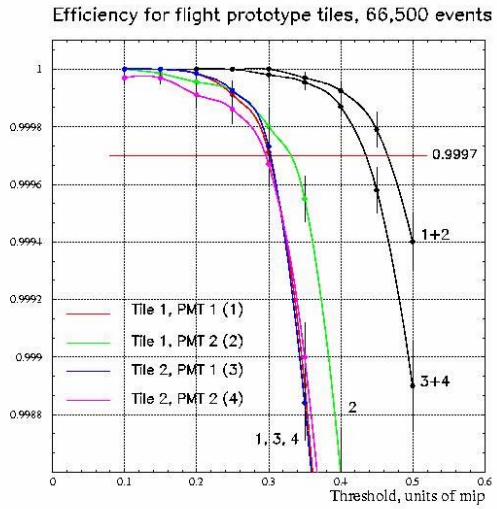


Figure 11. Efficiency for flight prototype tiles.

10.1.3 Hermeticity

In order to minimize the effects of gaps between scintillator tiles, all tiles are overlapped by 1cm in one direction, and have gaps in the other. The gaps are required to be ~ 3 mm (0.7mm for wrapping and 2mm for thermal expansion). These gaps are covered by scintillating fiber ribbons, as shown in Figure 12. Simulations show that the ACD as a whole can meet the 0.9997 efficiency requirement with this design.

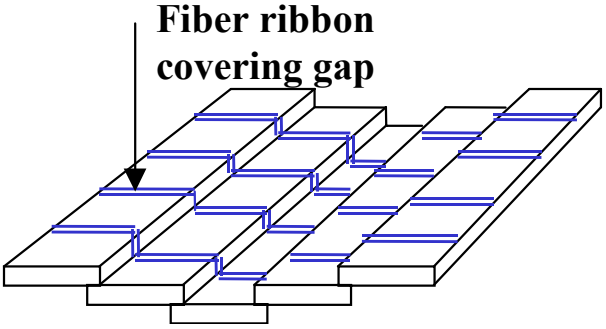


Figure 12. Technique for sealing gaps on the top surface of the ACD. The ribbons are made of square scintillating fibers.

10.1.4 Photomultiplier Tube

Because the ACD requires 194 phototubes, the tube must be small, in addition to having gain and noise characteristics suitable for detecting small numbers of photoelectrons. The tube selected is the Hamamatsu R4443, a ruggedized version of the R647 that we used for the 1997 beam test. The R647 tube (the non-ruggedized version) was used on the RXTE satellite mission and a nearly equivalent R4444 was used successfully on the GOLF instrument aboard the SOHO satellite.

10.1.5 Thermal Blanket/Micrometeoroid Shield/ACD "Crown"

As the outer detector element of the LAT, the ACD must be covered by some sort of thermal insulation. A second requirement in addition to thermal control is protection of the light-sensitive scintillator from a penetration by space debris or a micrometeoroid that could allow a light path. In full sun, even a tiny light leak would disable the TDA. The design issue is that the outer shield must also have very low mass, because nuclear interactions in this inert material will produce gamma rays from neutral pion decay. The experience with the COS-B gamma-ray telescope illustrates that such locally-generated background is not a hypothetical concern: the cosmic-ray-induced gamma-ray background in COS-B exceeded the flux from the high-latitude diffuse gamma radiation. The low mass requirement clearly conflicts with the protection goal. The three design rules that were used to achieve a low background for EGRET were:

1. Make the blanket/shield as lightweight as possible (low mass makes a smaller target).
2. Keep the blanket as close to the scintillator as possible (maximizing the chance that charged particles hitting the blanket will also produce a VETO signal in the scintillator).
3. Minimize the linear path length through the blanket (a shorter path reduces the chance of an interaction).

The first two of these design principles are achieved in the manufacture and placement of the thermal blanket/micrometeoroid shield itself, as described in section 10.3. The third affects the ACD scintillator design. Because the GLAST LAT ACD is box-like, it presents a long straight path through the thermal blanket on the upper (forward) face of the ACD. Simulations show that the flux of gamma-rays induced in this large, flat surface could be significant compared to the diffuse gamma radiation the LAT is trying to measure. Details are given in "Does ACD Need a Crown?" http://lhea-glast.gsfc.nasa.gov/gsfc/acd/acdpdr/ACD_Crown.pdf

Our solution is to extend the upper side scintillator panels upward around the edge of the top panels. This "crown" of scintillator will flag those cosmic rays that go through the top blanket horizontally. Even then, special analysis will be required, because the ACD signal will not come from the tile that the gamma-ray points toward.

10.2 Mechanical Design

The ACD Mechanical Subsystem is comprised of two primary assemblies, the Base Electronics Assembly (BEA) and the Tile Shell Assembly (TSA). The BEA is the mechanical support structure for the ACD. It supports the TSA and houses the ACD electronics as well as provides the mechanical and electrical interfaces to the LAT. It is an aluminum structure and it is mechanically symmetric. The TSA supports the Tile Detector Assemblies (TDA's) and their associated fiber cables as well as the Micrometeoroid Shield/Thermal Blanket.

Figure 13 shows an exploded view of the ACD. The ACD Assembly drawing number is (GE2054500).

The estimated mass of the ACD is 228.2 kg and the calculated center of gravity is 0,0,332 mm (in the LAT coordinate system). The 24 electrical cables from the LAT are mated to the ACD using electrical bulkhead connectors on the BEA.

The calculated average percent gamma radiation absorbed by the ACD is 4.5%, which is less than the required maximum of 6.0%. Table 5 shows a breakdown of the radiation absorbed by each layer of material used in the construction of the ACD.

The primary advantages to the ACD mechanical design is that it provides a clean and simple interface to the LAT, is easy to integrate to the LAT, and allows the TSA and BEA to be integrated and tested in parallel.

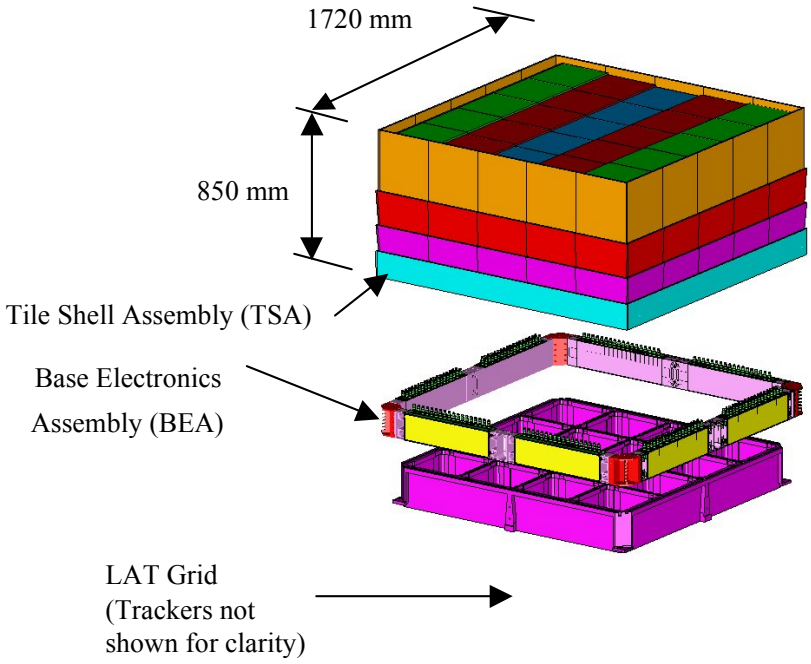


Figure 13. ACD Assembly with Exploded View

Table 5. Percent Radiation Absorbed

Layer	Equivalent Thickness (cm)	Radiation Length (cm)	% Radiation Absorbed
Nextel Woven Fabric 312*	0.0283	6	0.47%
Solimide Foam* (2.8 cm)	0.016	28.6	0.06%
Thermal Blanket	0.1	28.7	0.35%
Kevlar*	0.05	20	0.25%
TDA Wrap (Tetratec)	0.025	15.8	0.16%
TDA Wrap (Tedlar)*	0.025	28.6	0.09%
Scintillator	1	42.5	2.33%
GrEP Facesheets	0.1	23.1	0.43%
Korex Core*	0.0587	17.8	0.33%
* Materials radiation length calculated and/or		TOTAL	4.46%

10.2.1 Base Electronics Assembly

The BEA serves as the primary support structure for the ACD. It supports the TSA as well as provides the mechanical interface to the LAT. It is an aluminum structure, which utilizes similar parts in its construction to keep the part count to a minimum. The BEA also houses and protects the ACD onboard electronics as well as provides the electrical interface to the LAT. The BEA is shown in Figure 14.

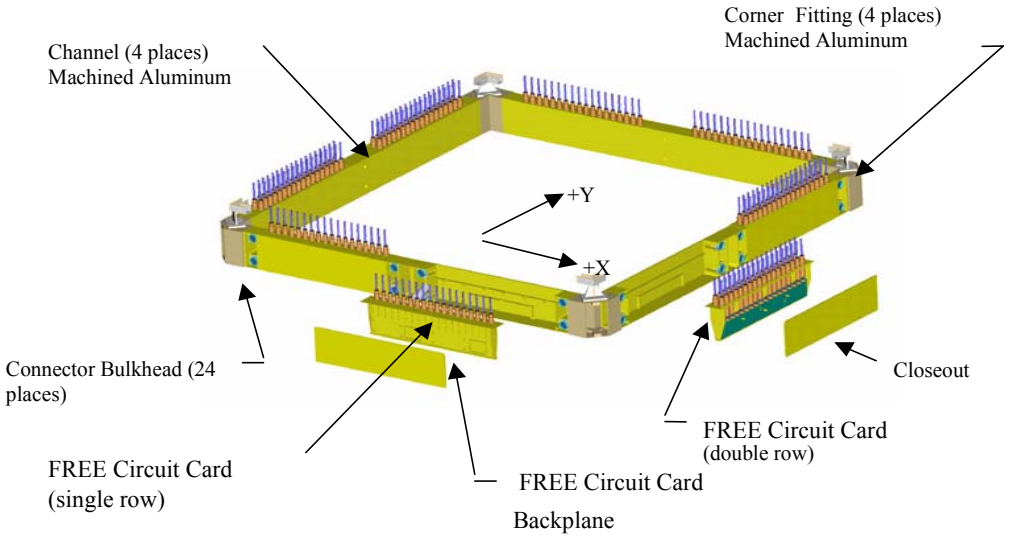


Figure 14. Base Electronics Assembly

The mechanical subsystem in the BEA is the Base Frame. There are four components that make up the Base Frame: corner fittings (4 places), channel sections (4 places), event board backplanes (8 places), and the closeout panels (8 places).

On the Y sides there are two single row Event Board Modules. Each Event Board Module has the capability to hold 18 PMT's. Therefore on each of the Y sides there are a total of 36 PMT's. Thirty-Two of the PMT's are for the TDA's and the other 4 PMT's are for the fiber ribbons. We are currently modeling the fiber routing on the Y sides.

On the X sides there are two double row Event Board Modules. This is because the output from the TDA's on the top (+Z side) is read out on the X sides. Essentially half of the TDA outputs from the top go to the +X side and the other half go to the –X side. Therefore each of the Event Board Modules on the X sides will have inputs from both the top (+Z) and their respective X side. The fiber routing on the X sides has been modeled, and while it is fairly complicated, it is feasible.

The Base Frame also provides the mechanical interface between the ACD and LAT. There are eight mounting points between the ACD and LAT, at the four corners and at the center of each side. Figure 15 shows the corner mount design, Figure 16 show the center mount design side view, and Figure 17 shows the center mount design front view.

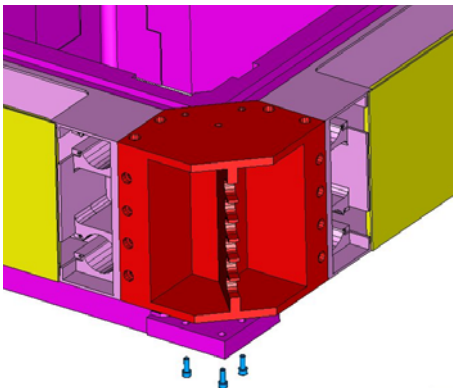


Figure 15. BEA Corner Mount

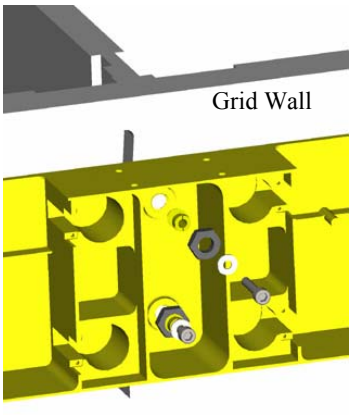


Figure 16. BEA Center Mount Side View

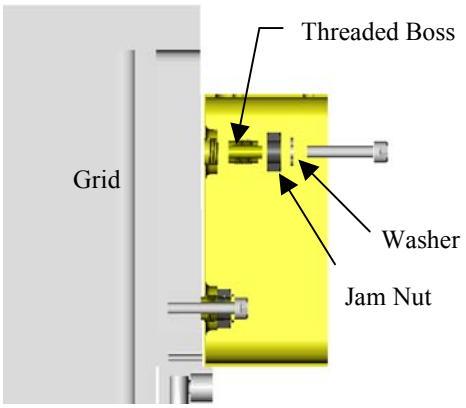


Figure 17. BEA Center Mount Front View

10.2.2 Tile Shell Assembly

The TSA consists of the following components: a composite shell, 8 titanium flexures which attach the TSA to the BEA, 89 TDA's and their associated fiber cables and cable tie-downs, 8 fiber ribbons, and TDA tie-downs.

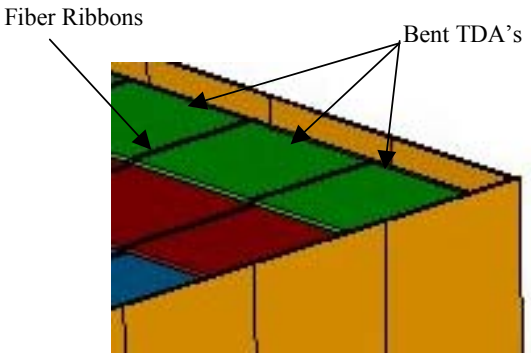


Figure 18. Tile Shell Assembly

There are 25 TDA's on the top and 16 TDA's on each side, shown in Figure 13. On the topside there are two different types of TDA's, flat TDA's and bent TDA's, shown in Figure 18, and Figure 22. There are 15 identical flat TDA's and 10 identical bent TDA's. The bent TDA's are positioned along two edges. They are required to provide routing access for the TDA fibers from the top TDA's to the PMT's, that are mounted on the BEA. The 16 side TDA's are arranged in four rows with five TDA's in each of the upper three rows and one single TDA for the lowest row. The TDA's are shingled in one dimension to eliminate gaps in that dimension; the gap in the other dimension is covered using fiber ribbons. The fiber ribbons are made of scintillating material with PMT connectors on both ends. There are a total of eight ribbons, four ribbons to cover the gaps along the X-axis and the other 4 ribbons to cover the gaps along the Y-axis.

10.2.2.1 SHELL ASSEMBLY

The composite shell (Figure 19) is constructed using honeycomb panels bonded together at the edges using edge clips. The honeycomb panel facesheet material is 0.5 mm thick M46J/RS-3 and the core is Korex 3/16"-2.0psf. The top panel is 51.8 mm thick and the side panels are 26.4 mm thick. 50 mm x 0.5 mm doublers are used around the base of the sides for additional strength. The edges of the panels are filled with lightweight filler and machined so that the panels can be bonded together at their edges as well. Since the edges of the panels are filled and bonded, the facesheets are perforated on the outside to provide venting of the core.

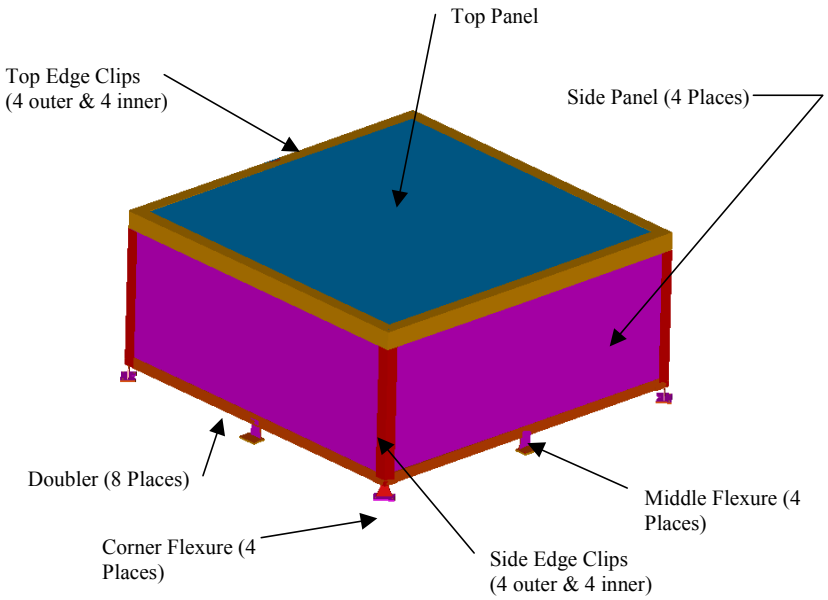


Figure 19. Shell Assembly with Flexures

10.2.2.2 TITANIUM FIXURES

The 8 titanium flexures are all single blade flexures and they are oriented so that they are normal to the center of gravity of the ACD. The flexures are required because of the coefficient of thermal expansion (CTE) difference between the composite shell and the base frame. There are two different types of flexures; one type is used at the corners and the other type is used at the midpoint of the sides. They both have a top and bottom flange and are bolted to the composite shell and base frame. The overall height of the flexures is 75mm and the flanges are 8 mm thick.

10.2.2.3 TDA TIE DOWNS

The TDA tie-downs (Figure 20) provide the interface between the composite shell and the TDA's. They are kinematic mounts to provide compliance for the thermal expansion and contraction of the TDA's. To minimize weight and radiation absorption the TDA Tie-downs are surface bonded to the composite shell. A stud protruding from each TDA

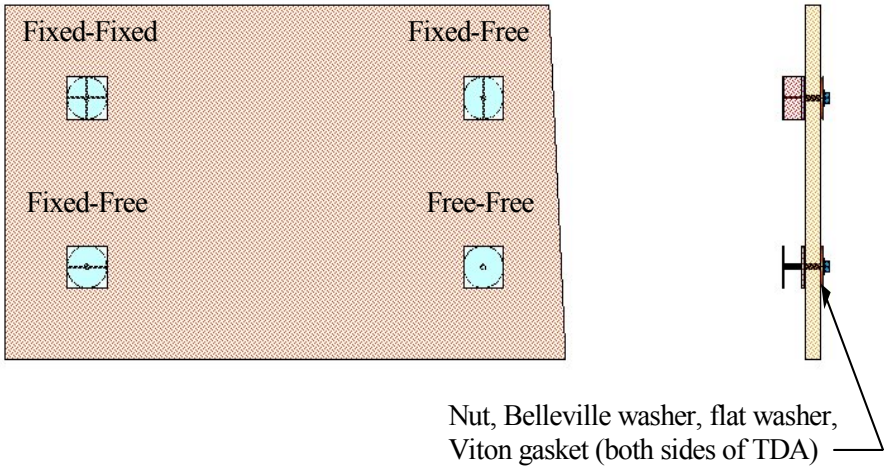


Figure 20. TDA Tie-down Orientation

Tie-down and is used to secure the TDA. This will be accomplished using a combination of seals and gaskets.

10.2.2.4 TILE DETECTOR ASSEMBLY

There are a total of 89 TDA's with 14 different tile geometries. All tiles are 10.00 +/-0.15 mm thick and there are two basic types of tiles, flat and bent. One (1) mm diameter wave shifting fibers are bonded into the tiles at a spacing of 5 mm. Every TDA will have a connector to transmit the light to the PMT's.

Figure 21. Key Hole Groove

In order to facilitate the bonding of the fibers into the bent tiles a keyhole groove (Figure 21) is cut into the tiles before bending. This groove holds the fibers in place while they are bonded in position. The minimum bend radius for the tiles is 4x the thickness of the tile and the minimum bend radius of the fibers is 25x the diameter of the fiber. See ACD-MPML-10001 for a list of the materials used for the TDA's. In addition, clear fiber cables (Figure 22) are required to transmit the light from the TDA's to the PMT's, except on the bottom two rows. These clear fiber cables are required to facilitate the integration and testing of the ACD, lessen the chance that the TDA's will be damaged during handling, and to minimize light loss over the length of fiber (the attenuation length of clear fiber is over 4x greater than for the wave shifting fiber). To transmit the light from the TDA to the PMT two connectors are required. One connector is required to switch from the wave shifting fiber to clear fiber, and the other connector is required to feed the light into the PMT.

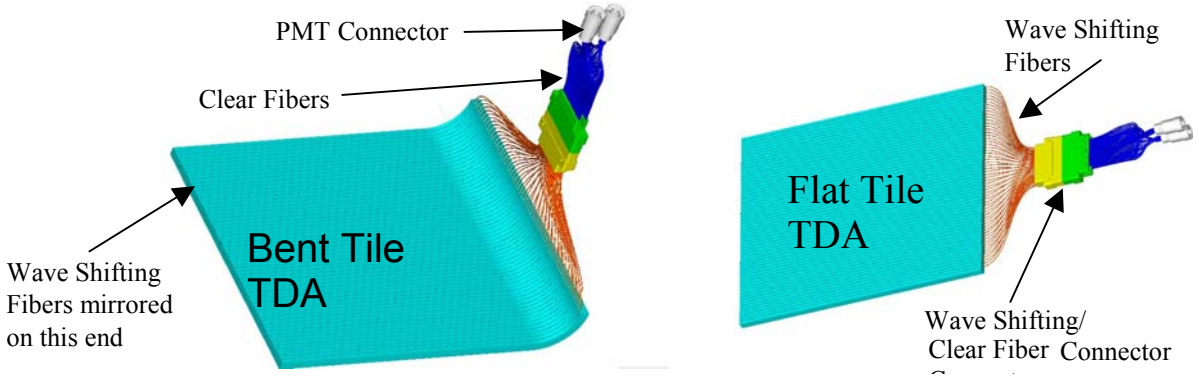


Figure 22. Flat and Bent Tile Assembly

10.2.2.4.1 Clear Fiber Connector

The clear fiber connector, Figure 23, will hold up to 68 fibers in two rows. The clear fiber diameter will be 1.2 mm to provide an additional 0.2 mm of alignment tolerance. The connector will be bolted and pinned together to maintain alignment during all environmental conditions. A vent path is also built into the connector to enable venting of the TDA and clear fiber cable.

10.2.2.4.2 PMT Fiber Connector

The PMT fiber connector, Figure 24, is a circular connector that connects the fiber bundle to the PMT window. It is spring loaded to eliminate overstressing the PMT window, eliminate gapping, and to reduce the positioning accuracy requirement.

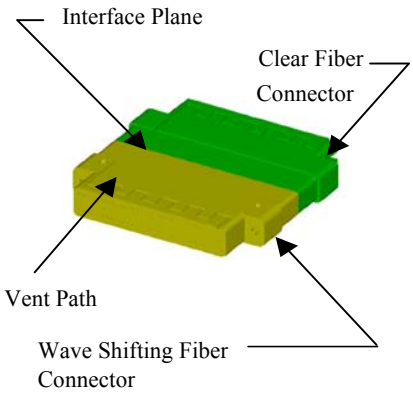


Figure 23. Clear Fiber Connector

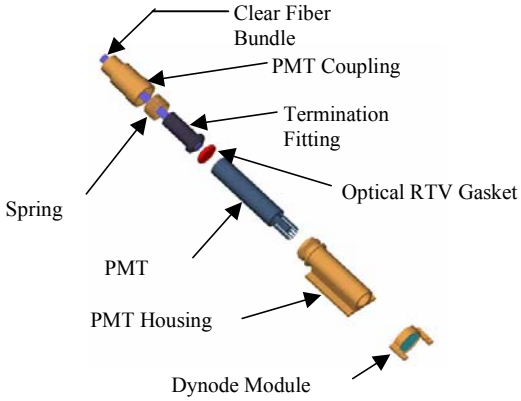


Figure 24. PMT Fiber Connector

10.2.3 Micrometeoroid Shield/Thermal Blanket

The sole purpose of the micrometeoroid shield is to prevent light leaks to the TDA's caused by the impact of orbital debris. However, it also has the benefit of providing thermal protection as well. A preliminary design of the MS/TB is shown below in Table below. NASA's Micrometeoroid experts at the JSC have been tasked with verifying and optimizing the current design. They have performed orbit simulations using a 3D model of the GLAST Observatory. Several high velocity impact tests have been performed to date and materials studies and characterization is underway. When the final shield design is complete, it will be tested for its thermal properties and then the required amount of thermal blanketing will be added to the micrometeoroid shield.

Layer	Thickness (cm)	Areal Density (g/cm^2)
Kevlar (innermost layer)	0.05	0.034
Solimide Foam	0.7	0.0054
Nextel Woven Fabric 312	0.025	0.043
Solimide Foam	0.7	0.0054
Nextel Woven Fabric 312	0.025	0.043
Solimide Foam	0.7	0.0054
Nextel Woven Fabric 312	0.025	0.043
Solimide Foam	0.7	0.0054
Nextel Woven Fabric 312	0.025	0.043
Thermal Blanket (outer layer)	0.32	0.0368
TOTAL	3.27	0.2644

The shield will be secured to the TSA using the same studs that attach the TDA's to the composite shell. A hat type fitting along with a threaded nut will be used to secure the micrometeoroid shield/thermal blanket to the attachment stud.

10.2.4 Mechanical Analysis

A NASTRAN™ Finite Element Method (FEM) mathematical structural model was developed for the Gamma-ray Large Area Space Telescope (GLAST), Anti-Coincidence Detector (ACD). The FEM, which contains 8,528 elements and 8,899 nodes, was used to determine stress margins, displacements under inertial loads and to obtain the natural modal frequencies of the system.

The Tile Shell Assembly (TSA) was modeled using CQUAD4 plate elements that encompassed the honeycomb paneling of the structure. The base frame that supports the TSA was modeled using a combination of CQUAD4 plate elements and CHEXA solid elements. The CHEXA solid elements are within the corner fittings of the base frame. The flexures were modeled using CBAR elements. The overall dimensions of the ACD and the base frame are illustrated in Figure 25.

The ACD shell is made from composite honeycomb panels consisting of M46J/RS-3 isotropic laminate facesheets with a Korex (Dupont) 3/16-2.0 core. The base frame is aluminum 6061-T6, and the flexures are Titanium. The actual tiles that mount onto the ACD were not physically modeled but were represented by non-structural mass. The material properties for the various materials within the FEM are presented in Table 6.

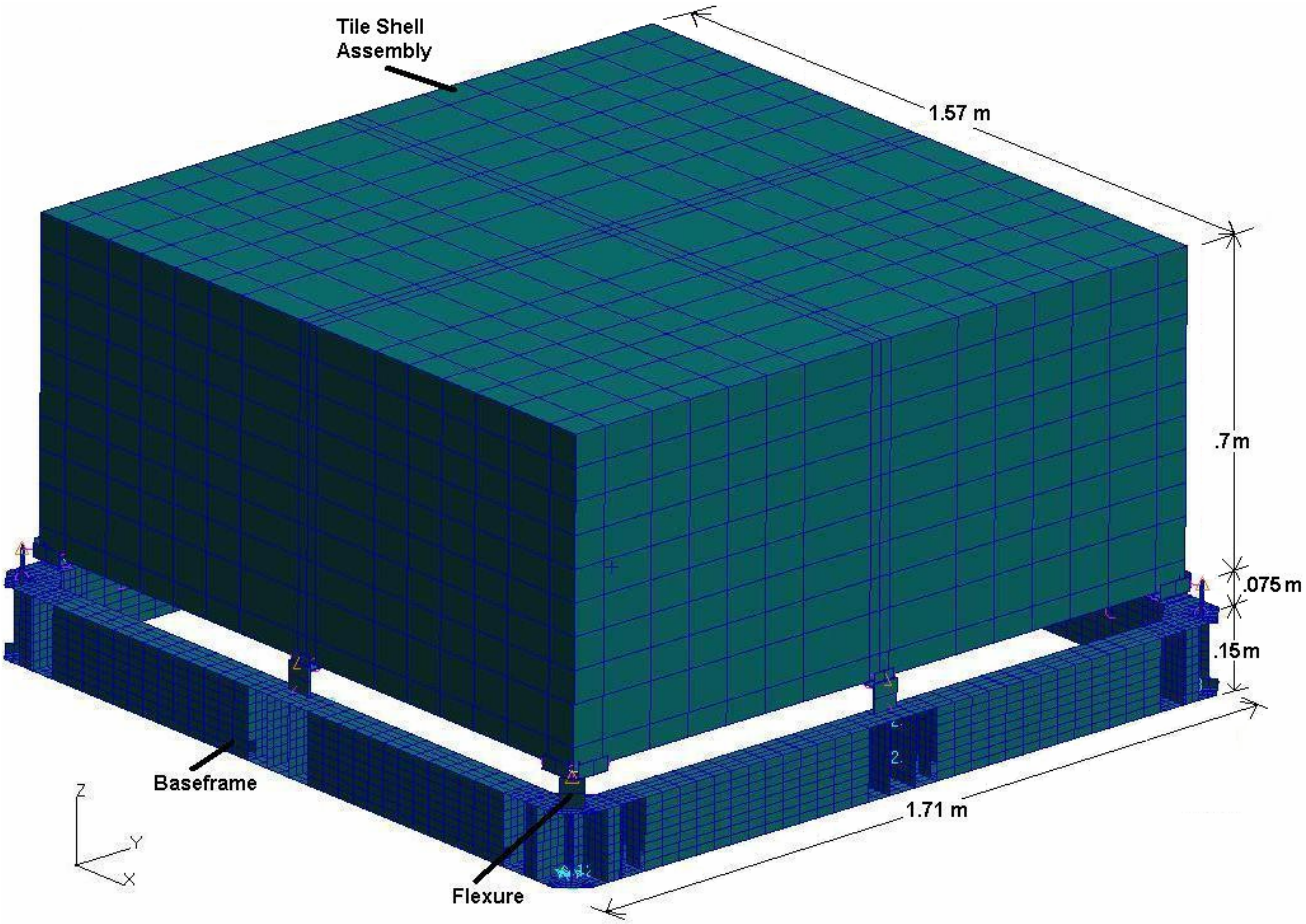


Figure 25. Finite Element Model

Table 6. Material Properties of GLAST components

Component	Material	Young's Modulus (N/m^2)	Shear Modulus (N/m^2)	Density (kg/m^3)
ACD composite facesheets	M46J/RS-3 Quasi-Isotropic Laminate	8.96E+10		1.66E+03
ACD composite core	Korex (Dupont), 3/16-2.0		5.86E+07	3.20E+01
Base frame	Aluminum 6061-T6	6.83E+10		2.71E+03
Flexures	Titanium Ti-6Al-4V	1.10E+11	4.27E+10	4.43E+03

The total modeled mass of the ACD is 247.6 kg, including mass contingency for analysis purposes. The mass shown for the TSA includes the tiles and MS/TB, which were represented with non-structural mass. As shown in Table 7, the total mass includes the mass of the electrical cables that were represented with non-structural mass at the sixteen cable tie-down locations. The actual PMT's were not modeled but were also represented with non-structural mass. The mass of the PMT's is included within the mass of the FREE circuit card assembly. The mass breakdown of each component is presented in Table 7.

Table 7. Mass Breakdown of ACD Components

Component	FEM (kg)
TSA	173.74
Flexures	4.42
Base Frame	28.78
FREE	24.67
Cables	16.03
Total	**247.64**

10.2.4.1 ANALYSIS

To validate the FEM, a free-free dynamics analysis with a stiffness equilibrium check was performed on the model. This check verified that the model behaves as a rigid body when it is unconstrained. This verification entails obtaining six rigid body modes, which the model did produce when the boundary conditions were removed. In addition to verifying rigid body motion, it also checked the stiffness matrix to verify that it did not contain any grounding effects.

10.2.4.1.1 Static Analysis

Static analysis was performed to verify that the system is structurally adequate when subjected to the design limit loads. The components were analyzed using the General Environmental Verification Specification's (GEVS) factors of safety, 1.4 for ultimate and 1.25 for yield. The ACD design limit loads are given in Table 8 and are defined from preliminary in-house GLAST Coupled Loads Analysis specified in the ACD Design and Test Loads Specification, ACD-SPEC-3006. The thrust and lateral loads are applied simultaneously for each event in all combinations. There are two events, Liftoff/Transonic (Max Lateral) and MECO (Max Axial). The thrust direction of the loads will be applied along the z-axis and the lateral loads will be applied along the x-y plane (See Figure 25).

Table 8. ACD Design Limit Loads (G's)

ACD Design Limit Loads (G's)		
	Event	
Direction	Liftoff/Transonic (Max Lateral)	MECO (Max Axial)
Thrust	+3.25/-0.8	+6.6
Lateral	± 4.0	± 0.1

The boundary conditions of the FEM consist of three nodes constrained in 3 DOF to represent the bolt pattern at the corner of the base frame. This connection represents the attachment to the LAT (See Figure 26). The base frame is also constrained at the four mid-side locations with two nodes to represent the two bolts that connect to the grid (See Figure 27). The mid-side nodes are constrained in 3 DOF to represent the connection to the Grid.

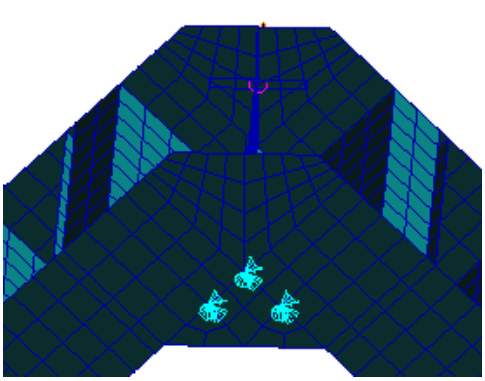


Figure 26. Corner Boundary Condition

A detailed stress analysis was performed on the Base Electronics Assembly (BEA). The design limit loads were applied to a combined LAT and ACD model. Two configurations were considered to obtain an envelope of loads for the components to be analyzed. The first configuration assumed the mid-spans (Figure 27) were connected in shear and tension. This case maximized the loads at the mid-span locations. The second configuration assumed that the mid-span connections take tension only, which resulted in maximizing the loads on the corner fittings (Figure 26).

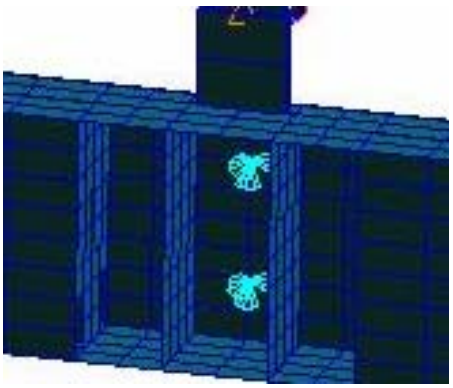


Figure 27. Mid-Side Boundary Condition

Once the loads from the FEM were obtained, hand calculations were performed to determine the structural integrity of the corner fittings, the mid-span connections are currently being analyzed. The analysis of the corner fitting showed positive margins (See Table 9) even when conservative assumptions were used.

In addition to the stress analysis of the corner-fittings and the mid-span sections, stress analysis was also performed on the tile shell assembly (TSA). Design limit stresses are based on a supported weight including a contingency of at least 1.15. A fitting factor of 1.15 is included where applicable. A summary of the margins of safety for the TSA Edge clips and the tile flexures are presented in Table 10.

Table 9. Margins of Safety for Corner Fitting

ITEM	FAILURE MODE	MS
Corner Fitting Bottom Bolts	bolt failure	4.4
Corner Fitting Bottom Bolts	insert failure	4.3
Corner Fitting	ultimate axial loading	0.16
Corner Fitting	yield axial loading	0.05
Corner Fitting	ultimate shear loading	1.9
Corner Fitting	end pad bending	1.3
Corner Fitting Side Bolts	bolt failure	9.2
Corner Fitting Side Bolts	shear tear out	19.3
Mid-Span Connection to Grid	rib failure	0.02
Mid-Span Connection to Grid	bolt failure	in work

Detailed stress analysis of the edge clip and concepts for the panel interfaces are in Table 10. The details of the preliminary analysis performed on the flexures are also included in Table 10.

Table 10. Margin of Safety of Edge Clips and Flexures

PART	FAILURE MODE	LIMIT STRESS OR FORCE	ALLOWABLE	MS
Edge Clips	Delamination	430 psi	2500 psi ultimate	+3.15
	First Ply Failure	1600 psi	28,000 psi ultimate	+Large
Doublers	First Ply Failure	4675 psi	28,000 psi ultimate	+3.27
Tile Flexure Blade	Bending Thermally Induced	20,400 psi	32,000 psi ultimate	+0.12
	Tension+Bending	1680 psi	32,000 psi ultimate	+Large
	Shear	1470 psi	10,000 psi ultimate	+3.87
	Column Buckling	22 lbf	39.5 lbf ultimate	+0.28
Tile Flexure-TSA Bonded Interface	Honeycomb Core Crushing	153 psi	260 psi ultimate	+0.21
	Adhesive Shear	44 psi	5000 psi yield	+Large

The predicted ACD shell deflections under the design limit loads are tabulated in Table 11.

Table 11. Deflections under Design Loads

CASE	LOCATION	DISP (mm)
Max Lateral (RSS X & Y)	ACD Shell Side Panel	0.54
Max Vertical (Z)	ACD Top Panel	0.79

10.2.4.1.2 Dynamic Analysis

The dynamic analysis was performed to obtain the natural frequency of the system. It was a goal to have the minimum frequency above 50 Hz. The modal frequencies and effective masses are provided in Table 12.

The minimum frequency requirement of 50 Hz was achieved. As shown in Table 12, the first natural mode of the system is 54.17 Hz, which corresponds to the lateral mode of the Tile Shell Assembly (TSA) along the x-axis (See Figure 29). The second mode of 54.18 Hz is complimentary of the first mode and is along the y-axis. The third mode of 58.09 Hz is a drum-head mode of the TSA (See Figure 28).

Table 12. Modal Frequencies and Effective Masses

MOMENTS OF INERTIA ABOUT MPFPNT
BASIC COORDINATE SYSTEM

I-XX	I-YY	I-ZZ	I-XY	I-YZ	I-ZX
1.43E+02	1.45E+02	1.84E+02	7.93E-05	1.50E-05	1.62E-05

EFFECTIVE MODAL WEIGHTS								
ODE #	Frequency (Hz)	X-WT (Kg)	Y-WT (Kg)	Z-WT (Kg)	I-XX (N-m^2)	I-YY (N-m^2)	I-ZZ (N-m^2)	Description
1	54.17	161.43	0.00	0.00	1.53E-04	5.02E+01	5.74E-13	Lateral Mode of TSA, X-dir
2	54.18	0.00	161.94	0.00	4.95E+01	1.54E-04	9.22E-13	Lateral Mode of TSA, Y-dir
3	58.09	0.00	0.00	62.05	5.72E-13	6.84E-12	2.23E-08	Drum-head mode of TSA
4	65.98	0.00	0.00	0.00	1.90E-12	1.19E-12	9.12E-12	Side panels of TSA, alternating sides
5	76.83	0.00	0.00	0.00	1.17E-12	3.81E-11	5.43E+01	Rotation of TSA, about Z-axis
6	78.32	10.68	0.00	0.00	7.75E-05	2.31E+01	4.34E-11	Rotation of TSA, about Y-axis
7	78.33	0.00	10.89	0.00	2.25E+01	7.74E-05	1.62E-12	Rotation of TSA, about X-axis
8	79.62	0.00	0.00	21.17	5.23E-11	3.60E-12	2.84E-07	2nd Drum-head mode TSA, including sides
9	94.78	0.00	0.35	0.00	1.54E+00	2.13E-04	6.63E-19	TSA Side panel mode
10	94.78	0.33	0.00	0.00	2.00E-04	1.57E+00	1.92E-13	TSA Side panel mode
11	97.31	0.00	0.00	0.00	6.56E-15	8.21E-13	5.23E-05	TSA Side panel mode
12	109.82	0.00	0.00	0.00	5.11E-12	2.11E-11	6.87E+01	TSA Side panel mode w/ low mass modes
13	115.06	0.57	0.18	0.00	3.44E+00	1.95E-04	2.27E-09	Low mass mode within Baseframe
14	115.46	0.00	0.00	0.02	1.17E-09	9.60E-13	8.02E+00	Low mass mode within Baseframe
15	118.22	4.56	0.05	0.00	2.97E-01	2.65E+01	7.30E-11	2nd Bending Mode of TSA w/ low mass mode
TOTALS		177.57	173.4	83.24	7.72E+01	1.01E+02	1.31E+02	
% OF TOTAL		72.53	70.82	34	54.11	70.02	71.52	

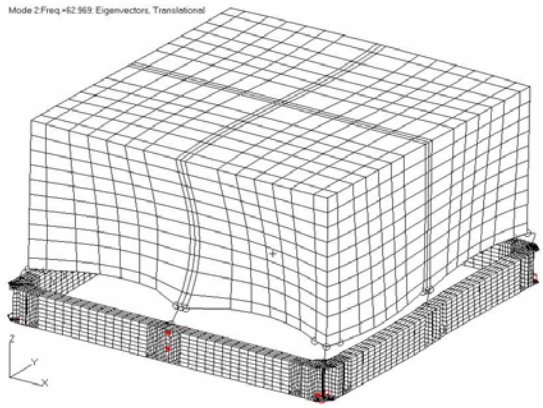


Figure 29. First Mode Shape

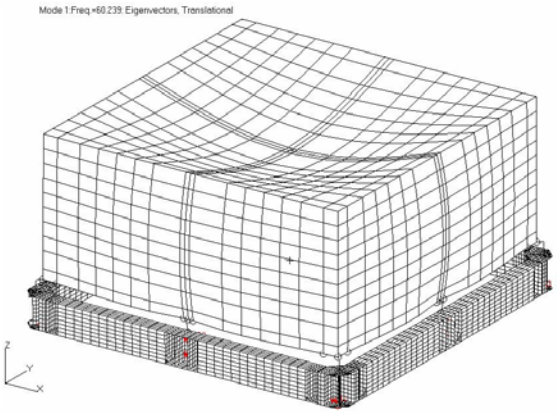


Figure 28. Second Mode Shape

10.2.4.3 ANALYSIS SUMMARY

The various components that were analyzed showed positive margins of safety once the constraint on the mid-span connection was modified. The dynamic analysis illustrated that the GLAST ACD system met the minimum requirement of 50 Hz. The first frequency of the GLAST ACD is 54.17

Hz, which corresponds to the lateral mode of the TSA. The displacements of the system, in response to the static loads, were also within the requirements previously stated.

10.3 Thermal Design

The ACD thermal design is structured about the LAT Grid and the Tracker towers. The design being a passive one utilizes the grid as a heat sink for the electronics. While the other temperature sensitive component, the Tile Detector assembly, is mainly designed around the effectiveness of the thermal shield and insulation.

The ACD electronics, the PMT's and the scintillator tiles have been identified as being temperature sensitive. The ACD contains twelve electronics boards that are mounted to the BEA frame. Each board has been estimated to have a power dissipation of 1.5 watts for a total ACD power dissipation of 18 watts. The operating temperature range that has been established for purposes of Systems Level thermal analyses is from –10 C to 40 C while the survival range is from –20 C to 45 C.

The ACD PMT's and scintillator tiles have no power dissipation. The operating temperature range for the scintillator tiles is from –50 C to 40 C. The survival range is from –60 C to 45 C. The thermal design strategy to satisfy the ACD electronics board temperatures is to utilize the LAT aluminum grid structure as a heat sink for the electronic boards. The ICD with LAT specifies that the grid will be operating in a temperature range from –10 C to 25 C. Design analyses adds and subtracts 10C from the grid operating range (-20C to 35 C) to assure a conservative design.

For the ACD TDA's, the temperatures will be balanced by the heat flow radiated from the LAT with the heat flow through the MLI blanket. The effective ACD emittance will be approximately 0.01. A thermal vacuum test will be performed to measure the thermal insulation provided by the micrometeoroid shield by itself without MLI blanket layers. Based on the results of this test and the required insulation characteristics of the ACD, an appropriate number of outer blanket layers will be added to achieve required thermal performance.

There are two orbit cases that are used to do the analysis and obtain temperature predictions. The first case being the hot case orbit where either the ±Y face is in the sun for the duration of the orbit. The second case being the cold case where either the ±X face is in the sun. In both cases the +Z is anti-nadir pointing. A safehold case has also been analyzed using the cold case orbit. With the point anytime, anywhere orbit of this mission the bounds of these two cases are sufficient in showing the worst case cold and hot environment. Table 13 displays the temperature predictions for the analysis.

Table 13. Temperature Predictions

Description	Cold Operating Temperature	Hot Operating Temperature	Safehold Temperature	Operating Temperature Range
Grid Boundary Temperature	-20	35	-30	-
Trackers Boundary Temperature	-20	35	-30	-
TDA Cold Temperature	-49	16	-55	-50 to 40 C
TDA Hot Temperature	-38	19	-38	-50 to 40 C
BEA +X Backplane 1	-14	39	-32	-
BEA +X Backplane 2	-14	39	-32	-
BEA +X Frame Temp. (-Y end)	-20	35	-30	-
BEA +X Frame Temp. (middle)	-20	35	-30	-
BEA +X Frame Temp. (+Y end)	-20	35	-30	-
BEA +Y Backplane 1	-18	36	-32	-
BEA +Y Backplane 2	-18	36	-32	-
BEA +Y Frame Temp. (+X end)	-20	35	-30	-
BEA +Y Frame Temp. (middle)	-20	35	-30	-
BEA +Y Frame Temp. (-X end)	-20	35	-30	-
Shell Hot Temperature	-31	28	-40	-
Shell Cold Temperature	-48	17	-54	-

The temperature predictions for the –X and the –Y frame and backplane temperatures are not shown because they are approximately the same as the predictions for the +X and +Y respectively.

The thermal model consists of a TSS surface model and a SINDA numerical model. The TSS model is used to calculate orbital fluxes as well as view factors to space. The TSS geometry model contains 34 surfaces with 528 active nodes. Input into the model is the geometry, the optical properties, the environmental properties and the orbit definition. TSS is initiated and radiation couplings to space and heat rates are output from the program. This output is used as input into the SINDA numerical model. The SINDA deck is a numerical network of capacitances and conductances. The SINDA deck contains 615 total nodes. With the conductances, capacitances, interfaces, sources and the output from TSS a SINDA run is initiated and temperatures are output. Shown below are images of the TSS geometry. On the left Figure 30 is the LAT exterior covered with MLI, and Figure 31 is the interior with the grid and tracker towers shown.

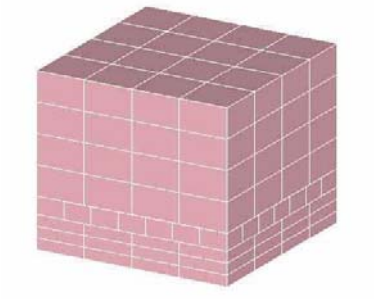


Figure 30. Exterior MLI

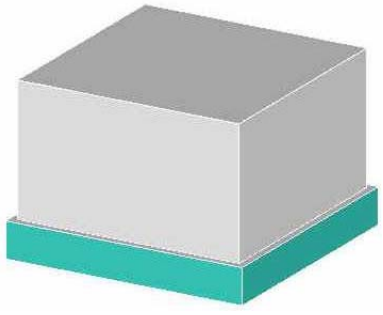


Figure 31. Towers and Grid

Shown in Table 14 are the TSS optical properties. The Kapton is predominantly used for closing out areas. The Silver Teflon is the outer layer of the MLI blanket. An aluminum finish is used as the surface property for the tracker tower exterior. The black anodize is used as the optical property for the grid exterior viewing the base frame as well as on the base frame viewing the grid. The M46J/RS-3 is the composite material on the surface of the shell.

Table 14. TSS Optical Properties

TSS Optics Name	Emissivity (BOL)	Absorptivity (BOL)	Emissivity (EOL)	Absorptivity (EOL)
3 mil Kapton	0.79	*	0.75	*
5 mil Silver Teflon	0.78	0.08	0.74	0.13
Aluminum	0.10	*	0.10	*
Black Anodize	0.82	*	0.78	*
M46J/RS-3	0.93	*	0.90	*

Table 15 shows the orbital parameters for the hot and cold cases.

Table 15. TSS Orbital Parameters

Case	Orientation	Altitude, km	Period, min	Orbit Inclination	Beta Angle
COLD	+X Facing Sun, +Z zenith pointing	550	95.5	28.5	0
HOT	-Y Facing Sun, +Z zenith pointing	550	95.5	28.5	0

10.4 Electronics Design

10.4.1 Anti-Coincidence Detector (ACD) Electronics Overview

The GLAST LAT ACD electronics is used to provide charge collection, amplification, and signal processing for the ACD scintillating tiles. The ACD interfaces to the ACD-Electronics Module (AEM) as a subsystem of the LAT. The process begins when photons generated in the scintillators by the passage of charged particles are optically collected and converted to electrical signals via photomultiplier tubes attached to the tiles. The current output of each photomultiplier tube is amplified and conditioned prior to a measurement of the signal amplitude. Fast discriminators are used for generation of VETO signals, and the analog input signal is used for a more precise pulse height measurement. Digital data are captured from these analog chains in response to LAT commands. These data are formatted and transmitted to the LAT computer for filtering, commutation, and downlink.

The block diagram below shows the arrangement of the 12 ACD FRont-End Electronics (FREE) circuit cards and their positions around the Base Electronics Assembly. There are two PMTs per tile. Two sides of the ACD can accommodate 72 PMTs each and the remaining two sides can service 36 PMTs each, for a system total of 216 analog chains, of which 194 will be used. One High Voltage Bias Supply (HVBS) will power the eighteen PMTs on each FREE circuit card. Each FREE circuit card interconnects directly to the AEM. There is no interconnection between ACD FREE circuit cards. There are no trigger primitives generated at the ACD.

In this configuration, it is required that the fibers from the top tiles be routed to the sides where there are sufficient channels to accommodate these signals.

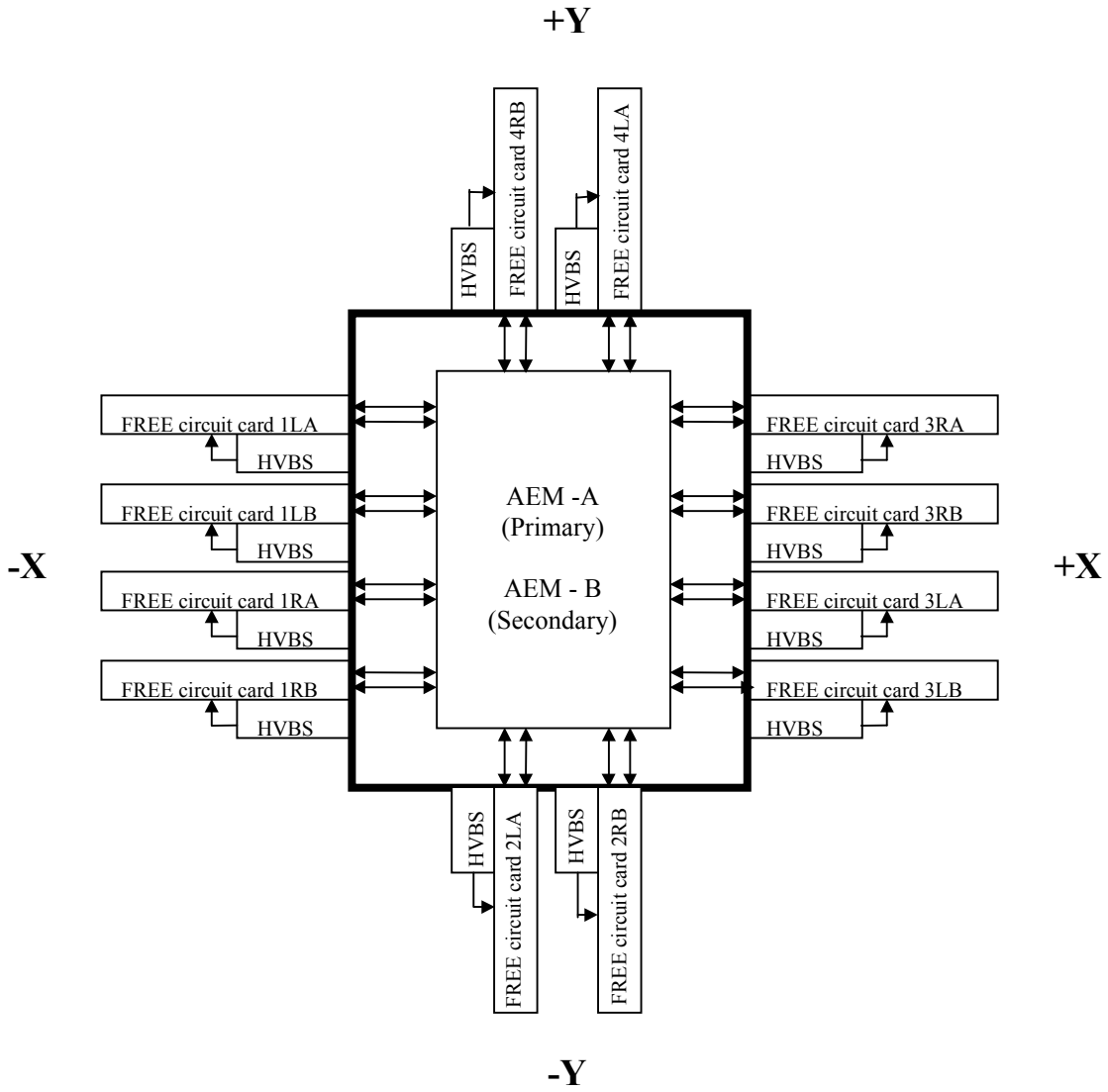


Figure 32. ACD Electrical System Block Diagram

10.4.2 Front-End Electronics

The front-end electronics provides interfaces to the AEM, the high voltage bias supply, and the PMTs. The FREE circuit card includes the analog application specific integrated circuit (ASIC), digital ASIC, and analog-to-digital converter (ADC).

10.4.2.1 ANALOG ASIC

The analog ASIC, also known as the GLAST ACD Front End (GAFE) ASIC, provides for the charge collection, amplification, shaping, and discrimination of the analog signal input from the PMT. The analog ASIC schematic is illustrated in Figure 33. The analog ASIC operates on a low voltage (3.3V) and dissipates a minimal amount of power (< 5 mW). V-to-I circuitry is required to interface the current-mode input and output signals of analog ASIC to the logic levels of the digital ASIC electronics.

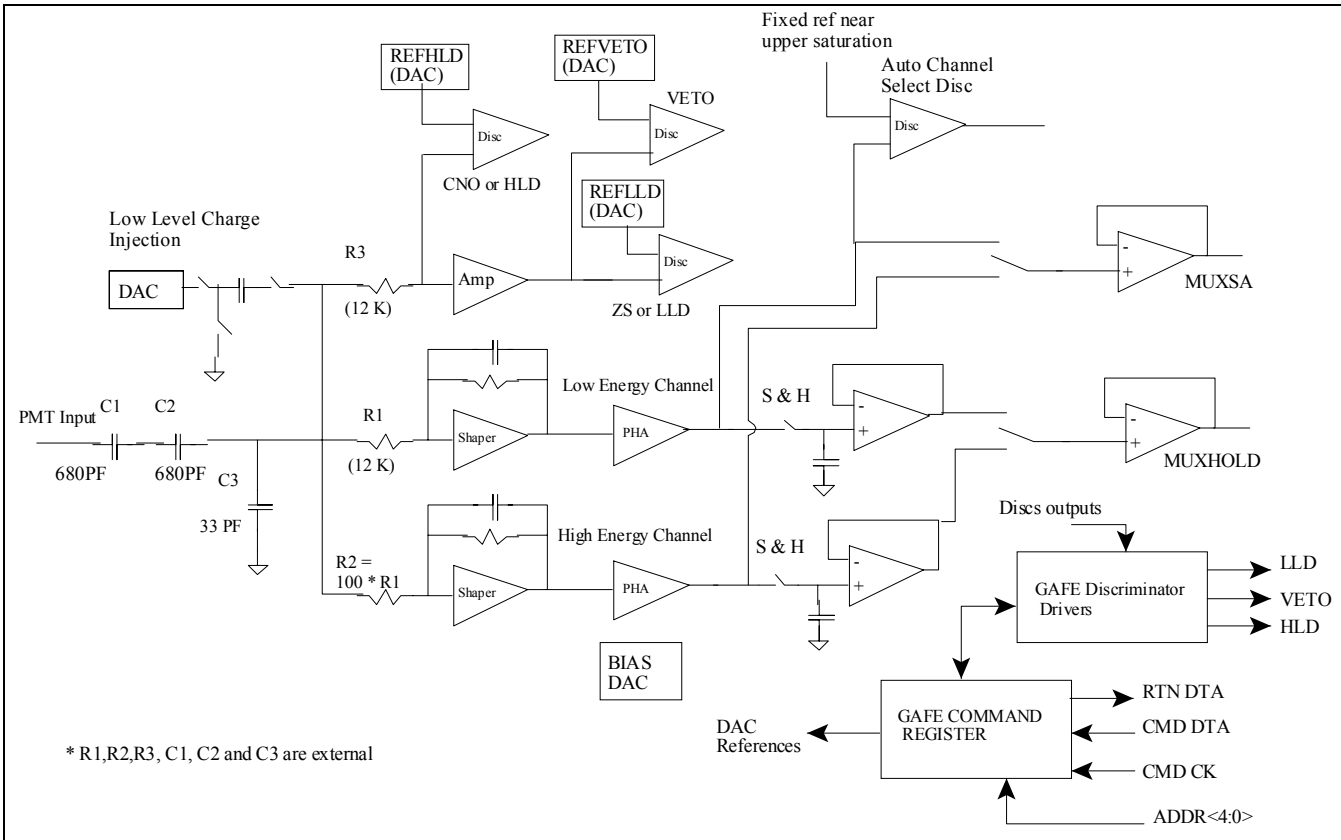


Figure 33. Analog ASIC Design

10.4.2.1.1 Analog ASIC (GAFE) Interface

The ACD analog ASIC (GAFE) is packaged in a 44 pin 10.0 mm x 10.0 mm TQFP plastic package with leads on a 0.8 mm pitch. This package is available from MOSIS through ASAT and provides for many spares. (http://www.asat.com/products/leaded/tqfp.htm)

The analog ASIC has the following pin connections. A minimum of 36 pins are required.

Power & Ground (8 pins)
VCC – analog power at +3.3V. There are 2 analog power pins.
VDD – digital power at +3.3V. There are 2 digital power pins.
AGND – analog ground. There are 2 analog ground pins.
DGND – digital ground. There are 2 digital ground pins.

Digital Address Inputs (5 pins)
AD4 – GAFE chip address most significant bit (bit 4), a voltage input (either VDD or DGND)
AD3 – GAFE chip address bit 3, a voltage input (either VDD or DGND).
AD2 – GAFE chip address bit 2, a voltage input (either VDD or DGND).
AD1 – GAFE chip address bit 1, a voltage input (either VDD or DGND).
AD0 – GAFE chip address least significant bit 0, a voltage input (either VDD or DGND).

Analog Inputs (5 pins)
DISCIN - Discriminator input for the low & high energy channels
SALO - Shaping amplifier input for the low energy channel
SAHI - Shaping amplifier input for the high energy channel
TCI - Test charge injection port
IDAC - DAC bias input

Analog Outputs (2 pins)
MUXSA – multiplexed shaping amplifier output - useful only for bench testing
MUXSH – multiplexed Sample and Hold output - used for PHA digitization

Digital Signal Inputs (8 pins)
CMDCK+ - differential, current mode, command clock (+) input from GARC
CMDCK- - differential, current mode, command clock (-) input from GARC

CMDD+ - differential, current mode, command data (+) input from GARC
CMDD- - differential, current mode, command data (-) input from GARC

STROB+ - differential, current mode, TCI strobe (+) input from GARC
STROB- - differential, current mode, TCI strobe (-) input from GARC

HOLD+ - differential, current mode, Sample/Hold (+) input from GARC
HOLD- - differential, current mode, Sample/Hold (-) input from GARC

Digital Outputs (6 pins)
RTND+ - tristate return data (+) output to the digital ASIC, common to all analog ASICs
RTND- - tristate return data (-) output to the digital ASIC, common to all analog ASICs
CHANID - single-ended current mode high/low range bit output to the digital ASIC
LLD - single-ended current mode LLD discriminator output
VETO - single-ended current mode VETO discriminator output to the digital ASIC
HLD - the single-ended OR'ed HLD discriminator output to the digital ASIC

Digital Drive Control /Bias (2 pins)

IRTN - current return for the single ended digital outputs, CHANID, LLD, VETO and HLD
ICNTRL - controls the current drive for the single ended digital outputs

10.4.2.1.2 Analog ASIC V-to-I Drivers and I-to-V Receivers

There is also an analog current-mode communications protocol for the exchange of digital information between the analog ASIC and the digital ASIC on the FREE circuit card. This communication is at a lower rate than that with the AEM.

10.4.2.1.3 Logic for the Low-Level, VETO, and High Level Discriminators

There are three discriminators for each analog channel. The low-level discriminator (LLD) can be used to allow the AEM to determine which event PHA values are below the threshold of interest. The VETO discriminator is used for signaling passage of any charged particle. The high-level discriminator (HLD) is used for signaling heavy nuclei passage.

There are three configuration bits available for each channel: LLD_EN, VETO_EN, and HLD_EN. The simplified logic schematic below demonstrates that the discriminator output function for each channel can be represented by the boolean expression (LLD AND LLD_EN) OR (VETO AND VETO_EN).

The HLD is enabled or disabled by the HLD_EN bit. For each set of 18 HLD 's on a FREE circuit card, there is one 18-input, single output OR gate provided to combine these into one signal to be forwarded to the AEM for possible use in event triggering and/or analysis.

10.4.2.1.4 Analog ASIC Power Distribution

The power distribution scheme is as follows:

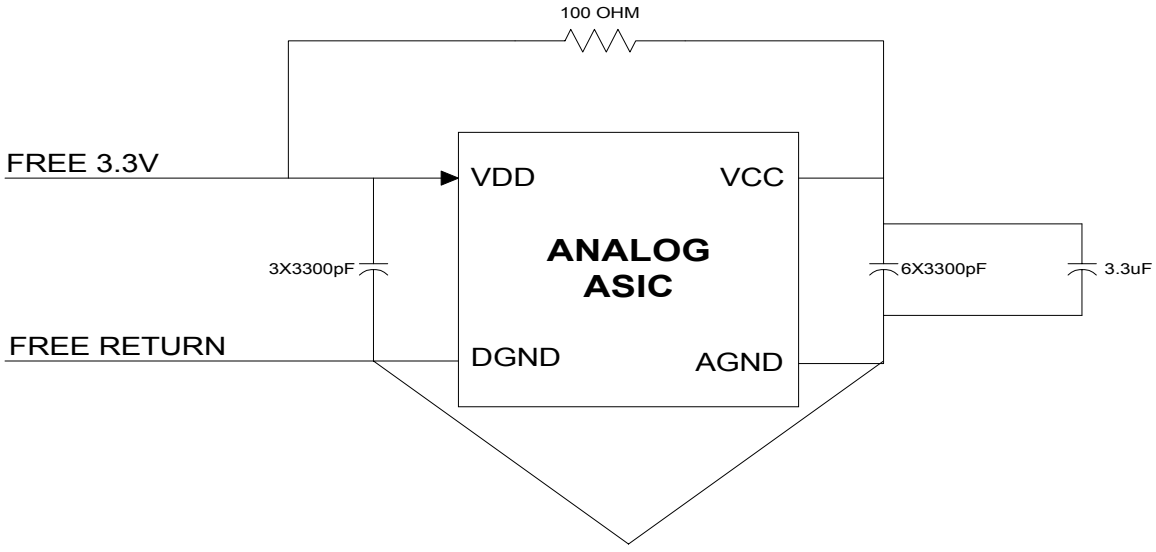


Figure 34. Power Distribution

The +3.3V power from the AEM comes to the front-end electronics processor. After local passive filtering on the FREE circuit card, this 3.3V is VDD, the digital power rail. This is locally bypassed with several ceramic capacitors. The analog power, VCC, is isolated for each ASIC by a 100-ohm resistor and locally bypassed by ceramic capacitors and one tantalum capacitor. The analog and digital grounds are tied to the FREE ground plane.

10.4.2.2 DIGITAL ASIC

The digital ASIC provides the interface to the eighteen (18) analog channels on the FREE circuit card and contains the digital logic and interface circuitry required to prepare event data for transfer to the AEM. The ASIC digital voltages are 0 and 3.3V.

The digital ASIC, also known as the GLAST ACD Readout Controller (GARC), has the following functional blocks: AEM interface, analog ASIC (GAFE) interface, command processor, data formatter, PHA logic, trigger delay logic, and hit map logic. The AEM interface that resides in the digital ASIC consists of differential drivers and receivers that are based on the standard LVDS protocol, a 3.5 mA current-to-voltage driver-receiver set. The analog ASIC interface consists of a custom-designed current-mode interface and is used by the digital ASIC to communicate to the 18 analog ASIC's. The command processor receives command information from the AEM and processes valid commands to change the state of the FREE circuit card. The data formatter is a state machine operating on a command-response protocol that will format and transmit serial data to the AEM at the command request. The PHA logic is responsible for controlling the 18 ADCs on FREE circuit card, capturing the digital pulse height information, and providing digital zero-suppression functions, if requested. The trigger delay logic provides for a commandable delay between the Trigger Acknowledge (TACK) and the shaping amplifier hold signal sent to the analog ASIC's. The hit map logic provides all combinatorial and shift-register delay functions associated with providing a serial hit map of PMT outputs above threshold prior to the TACK. This ASIC will be fabricated in the Agilent 0.5um CMOS process and packaged in a plastic quad flatpack. A block diagram of the digital ASIC is shown in Figure 35.

10.4.2.3 ANALOG-TO-DIGITAL CONVERTER

The ACD will utilize a commercial analog-to-digital converter, suitably qualified and screened. This part will be identical to the ADCs used on CAL and TKR, and will be provided to GSFC by SLAC. The specific part number is baselined to be Maxim's MAX145.

10.4.3 High Voltage Bias Supplies

The low power consuming HVBS use a simple, reliable and flight proven circuit approach. Figure 36 and Figure 37 illustrate the block diagram and schematic respectively. The voltage is generated from a 500 kHz resonant sine wave Hartley oscillator and has a 170 volt peak-to-peak output. The HVBS's ten-stage multiplier steps the voltage from 400 volts to 1500 volts. The output voltage will be adjusted by a linear control voltage with a range from 0 volts to 2.50 volts. Specific HVBS design parameters are illustrated in the table below . Output regulation is achieved by controlling the

conduction of the oscillator switching transistor. The HVBS incorporates planar transformer implementation. Each HVBS provides power to 18 PMTs, where the 18 PMTs are all on the same FREE circuit card.

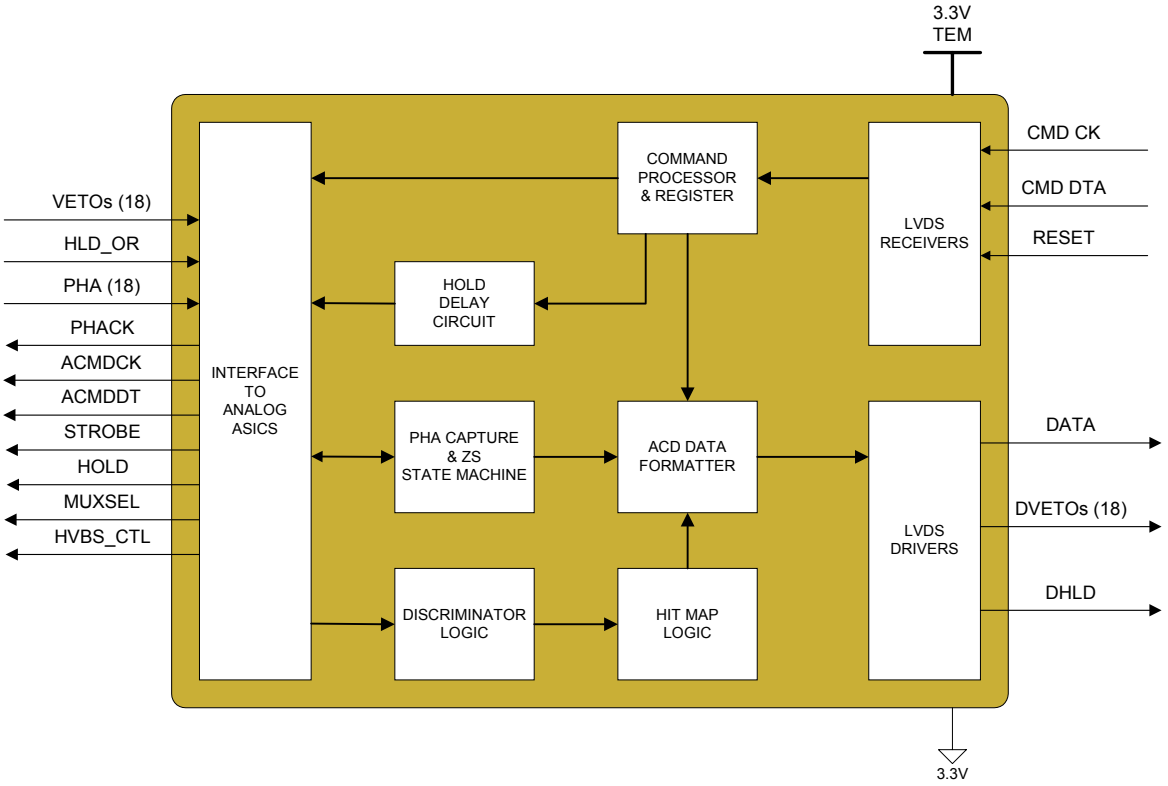


Figure 35. Digital ASIC Block Diagram

The HVBS will consist of a 2" x 4" PCB mounted onto the BEA with the mechanical assembly serving as shield/housing. The high voltage sections, multiplier & high voltage filter, utilize small capacitors, diodes, and resistors. The high voltage sense resistor is axial leaded. All of the high voltage components and conductors will be contained on the top layer of the PCB. No high voltage nodes will be carried on the PCB's inner board layers. Transformer and multiplier will be shielded from the high voltage filter and control electronics. Void free conformal coating will be used in the dielectric design.

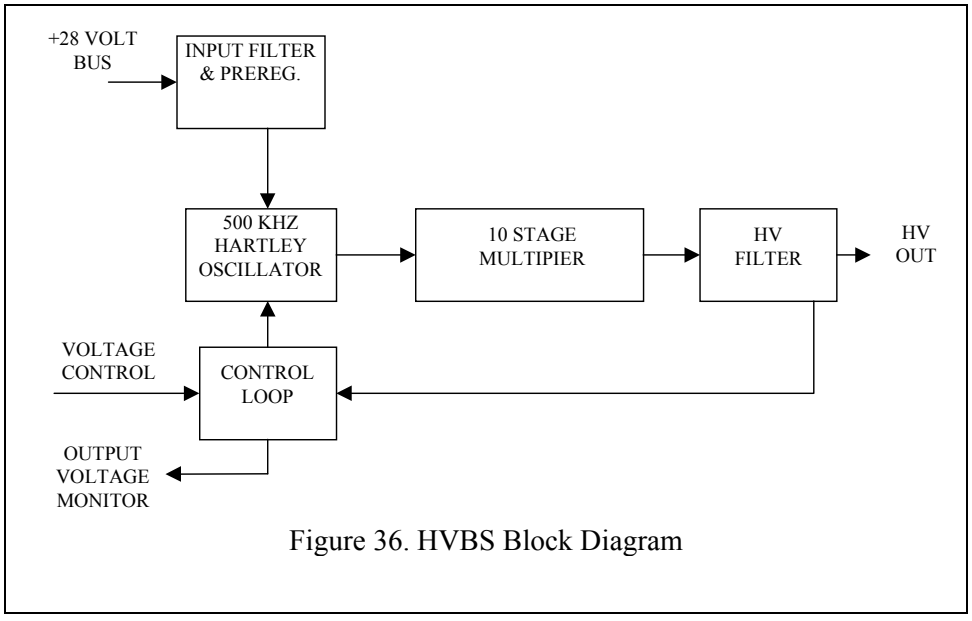


Figure 36. HVBS Block Diagram

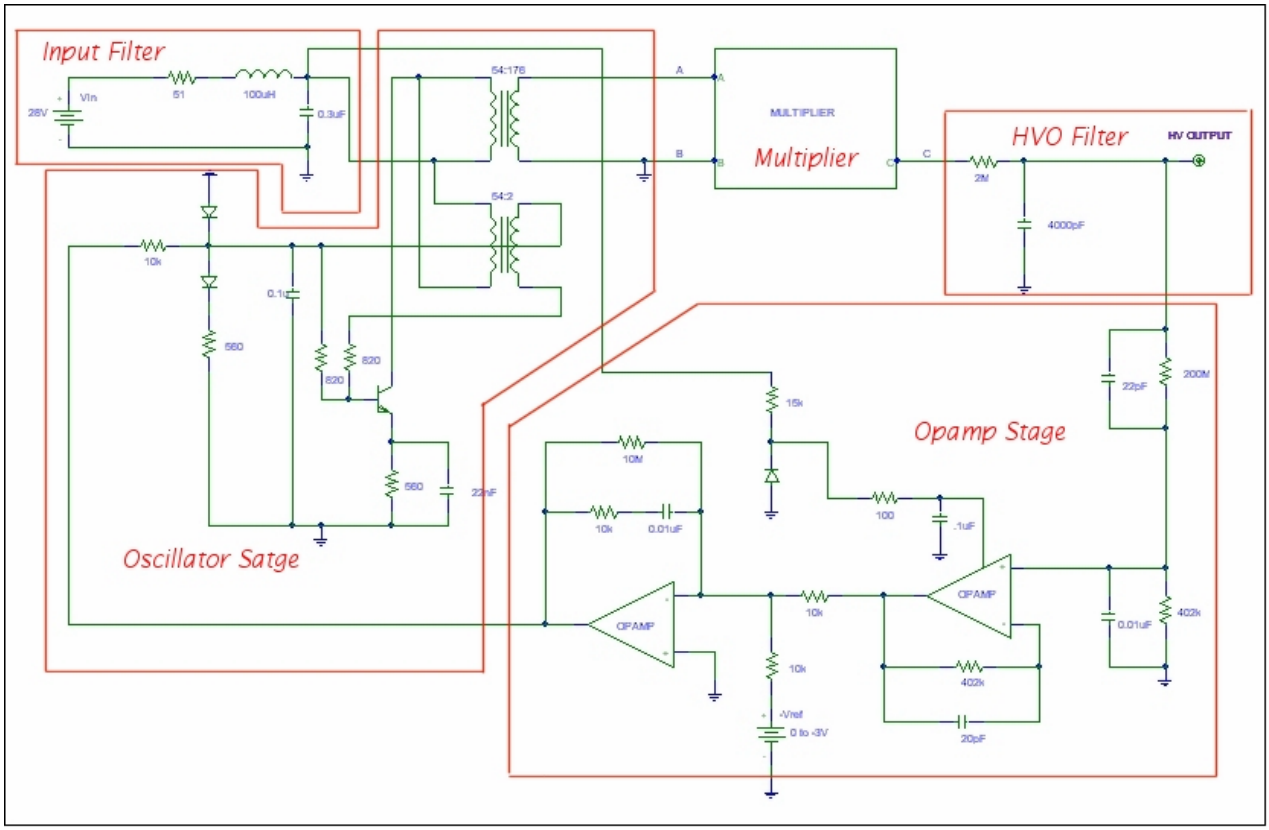


Figure 37. HVBS Schematic

HVBS Design Parameter	Specification
Output current	< 60uA
Load and line regulation	1.0%.
Output ripple	< 2mv.
Power consumption with max. Load	450mw.
Oscillator frequency	> 100khz, no synchronization required.
Dc isolation (+28 return to high voltage return.	>120ohms.

10.4.4 Low Voltage Power

The low voltage power supplies used to supply the filtered +28V and regulated +3.3V to the ACD are located outside the ACD subsystem. The low voltage power supply characteristics are defined in the LAT Dataflow Subsystem Specification – ACD-TEM (AEM) Interface, LAT-SS-00363-Dx.

10.4.5 Photomultiplier Tubes

The photomultiplier tubes baselined for the ACD will be Hamamatsu model R4443 tubes. These tubes are head-on, 15 mm diameter, 10-dynode, bi-alkali photocathode, 1250 V maximum bias tubes with gain adjusted to ~400,000.

10.4.6 Photomultiplier Tube Biasing Circuitry

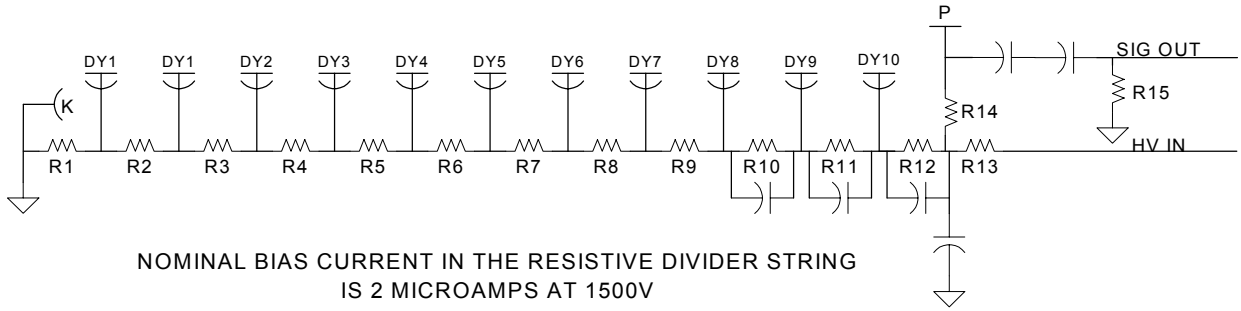
Each PMT requires a series of resistors and capacitors to properly bias the tube. The nominal bias string current is 2 μA at 1500 V. The nominal average current at the anode of the phototube (gain = 400,000) is calculated for a 1 kHz rate as

$$I = \frac{\partial Q}{\partial t} = (10\,pe)(1.602\times10^{-19}\,C/pe)(4\times10^{5}\,gain)(10^{3}\,Hz) = 640\,pA$$

The bias string current is purposely set high to allow for a possible larger number of photoelectrons (x5) and uneven gain degradation within a group of 18 PMT's, which would require higher gain for the stronger PMT's.

For a phototube with 10 dynodes, anode (P), and grounded photocathode (K), the biasing circuitry is shown in Figure 38.

In this configuration, resistor values of approximately 40 MΩ are appropriate for the dynodes. The high voltage rated (3000V) capacitors are approximately 680 pF. The current limiting resistor for the HVBS is approximately 40 MΩ and will provide a 135 volt drop and a nominal 2 μA. LAT-SS-00352-D10, section 5.11.1 - 5.11.3] The capacitor from resistor R13 to ground is a high voltage bias filter and meets the requirement of LAT-SS-00352-D10, section 5.11.4. In the diagram above, the resistor designated as R15 has a value of approximately 1MΩ, as per LAT-SS-00352-D10, section 5.11.5. Additionally, resistor R14 has a value of 1 MΩ, as per LAT-SS-00352-D10, section 5.11.6. The capacitors bypassing R10, R11, and R12 meet the requirement of LAT-SS-00352-D10, section 5.11.7.



PMT BIASING CIRCUITRY

Figure 38. PMT Biasing Circuitry

10.4.7 Electronics Mass

Electronics board mass is estimated using 1.25 gm/cm^2. The mass of an ACD front-end electronics processing board will not exceed 600 grams. The mass of the enclosure is not included in this estimate. The total mass of the ACD electronics will not exceed 25 kilograms, excluding the external wiring harnessing to the AEM, as per LAT-SS-00352-D10, section 5.17.

10.4.8 Electronics Enclosures

The ACD electronics will be fully enclosed in conductive housings. These housings will provide protection for the electronics and act as faraday cages for radiative emissions and susceptibility. These enclosures will be plated with a non-oxidizing, conductive passivation. The ACD electronics enclosures will provide a minimum of 0.05" of aluminum (or equivalent) for protection from micrometeoroids and space debris, and for the reduction of the total dose of ionizing radiation.

10.4.9 EMI/EMC Specification

Electromagnetic interference characteristics will adhere to MIL-STD-461/462. The EMI/EMC specifications will meet or exceed limits set forth in the Conducted Emissions (CE03) test, Radiated Emissions (RE02) test, Conducted Susceptibility (CS02, CS03) tests, Radiated Susceptibility (RS03) test, and the Magnetic Properties test.

10.4.10 System Grounding

The ACD system grounding is designed in accordance with the "ACD Grounding and Shielding Plan", LAT-TD-00435.

11 ACD SUBSYSTEM INTERFACE DESCRIPTION

The ACD mechanical and thermal interface to the LAT Grid is through an 8-point mount (4 corner mounts and 4 BEA center mounts), shown in Figure 15, Figure 16 and Figure 17 (Section 10.2.1 Base Electronics Assembly). The ACD electrical interface to the AEM is through 24 identical cables that connect into the AEM, see Figure 32. The cables are divided between the primary (A-side) and secondary (B-side) AEM's.

11.1 Mechanical and Thermal Interface Control

The detailed specification of the ACD mechanical and thermal interface to the Grid is contained in LAT-DS-0-241-Dx, LAT Mechanical Systems – ACD to Grid Interface Control.

11.2 Electrical Interface Control

The detailed specification of the ACD electrical interface to the AEM is contained in LAT-SS-00363-Dx, LAT Dataflow Subsystem Specification – ACD-TEM (AEM) Interface.

12 ACD SAFETY AND MISSION ASSURANCE

The ACD Safety and Mission Assurance Program will be conducted in accordance with LAT-MD-00039-01, "LAT Performance Assurance Implementation Plan" (PAIP). Additionally, ACD S&MA activities at GSFC will be conducted in accordance with the GSFC ACD-QA-8001, "ACD Quality Plan." The ACD S&MA Program will be coordinated by the GSFC ACD/GLAST Systems Assurance Manager (SAM) who will coordinate the ACD S&MA Program with the LAT Performance and Safety Assurance (P&SA) Manager. Selected highlights of the ACD S&MA Program are listed below.

12.1 Reliability

The reliability requirements listed in Chapter 8 of the LAT PAIP govern the ACD reliability program and the corresponding analysis performed for the ACD. The primary analyses/tasks include the Failure Mode Effect Analysis (FMEA), the Critical Items List (CIL), comparative numerical reliability assessments, and the limited-life items list that are described below in more detail. Other analyses, including the parts stress and trend data, also are required but are not thoroughly discussed below. As the design and development process continues, more specific information regarding the part stress data analysis and test data trend results will be generated and documented for review. (See Paragraph 12.2.1 for additional information on the parts stress analysis.)

From an overall perspective, the reliability program is integrated with the design process. The program interacts effectively with other project disciplines including systems engineering, hardware design, and parts engineering. The high reliability requirements are achieved by optimizing design, reliability, and cost considerations so mission and project objectives are met. The reliability program was started early in the design process to identify potential problems or "bottle-necks" and to help guide decisions impacting design and reliability considerations.

12.1.1 FMEA & CIL

Both the Failure Mode Effect Analysis and Critical Items List activity are focused on assessing failure modes (beginning with components and interfaces) for their effects at the local, subsystem, and mission levels of analysis. Details relating to the subject analysis can be found in ACD-RPT-12001, "FMEA & CIL."

In summary, the FMEA did not identify any single point failure items whose failure modes could result in the loss of one or more mission objectives. Some cases where the failure of identical or equivalent redundant hardware could result in the loss of one or more mission objectives were identified and are summarized in Table 16.

12.1.2 Comparative Numerical Reliability Assessments

An iterative comparative numerical assessment process is being used by GSFC to optimize the ACD reliability design and cost. First, preliminary reliability targets are allocated to each of the ACD components from the top-level 0.96 ACD target assigned by SLAC. Second, each component design is analyzed to determine if and how its corresponding reliability target allocation can be achieved. Third, the ACD team examines the level of effort and relative costs associated with improving the

reliability of required components in order to achieve the current allocation of component reliability targets. Fourth, based on this information, the team decides if new reliability target allocations will be assigned to each component so that the overall ACD 0.96 can still be achieved while further reducing cost. This iterative process continues until the ACD design is optimized in terms of both cost and reliability. Additional effort will be required prior to CDR to update the reliability allocations and tradeoffs as design progress continues.

Table 16. FMEA 2R Severity Classification Summary

2R SEVERITY CLASSIFICATION – COMPONENT, FAILURE MODE AND MISSION EFFECT	**FMEA REPORT, FAILURE MODE ID.**
Component – Scintillator Tile; **Failure Mode** – No light generation/ Outside light exposure; **Mission Effect –** Loss of DAQ Filtering Efficiency (when 2 or more tiles fail)	**5.01, 5.02**
Component – High Voltage Bias Supply; **Failure Mode** – No power; **Mission Effect –** Loss of DAQ Filtering Efficiency (when active redundant HVBS within the board pair fails)	**6.01**
Component – Digital ASIC; **Failure Mode –** No output; **Mission Effect –** Loss of DAQ Filtering Efficiency (when active redundant ASIC within the board pair fails)	**9.01**
Component – ACD to AEM Connection; **Failure Mode –** No output; **Mission Effect –** Loss of DAQ Filtering Efficiency (when 2 of 2 connections for a board pair fails)	**11.01**
Component – Micrometeoroid Shield; **Failure Mode –** Light leakage in tile; **Mission Effect –** Loss of DAQ Filtering Efficiency (when 2 penetrations or tile failures occur)	**12.01**

Figure 39 illustrates the most current reliability apportionment performed including corresponding allocations for each of the major ACD component. Figure 40 is an example of a trade-off analysis performed to optimize the HVBS design. Eight HVBS design configurations were analyzed with option "A" selected as the current baseline. Option A consists of 1 power supply per board and 2 actively redundant power supplies per board pair which support 18 Tile-to-AEM channels. The following list defines the different HVBS configuration that were analyzed and are shown in Figure 40.

A - 1 P/S per board, 0 stand-by (1 active P/Ss per 18 PMT's)
B - 2 P/S per board, 1 stand-by (1 active P/Ss per 18 PMT's)
C - 3 P/S per board, 2 stand-by (1 active P/Ss per 18 PMT's)
D - 2 P/S per board, 0 stand-by (2 active P/Ss per 18 PMT's)
E - 4 P/S per board, 2 stand-by (2 active P/Ss per 18 PMT's)
F - 6 P/S per board, 4 stand-by (2 active P/Ss per 18 PMT's)

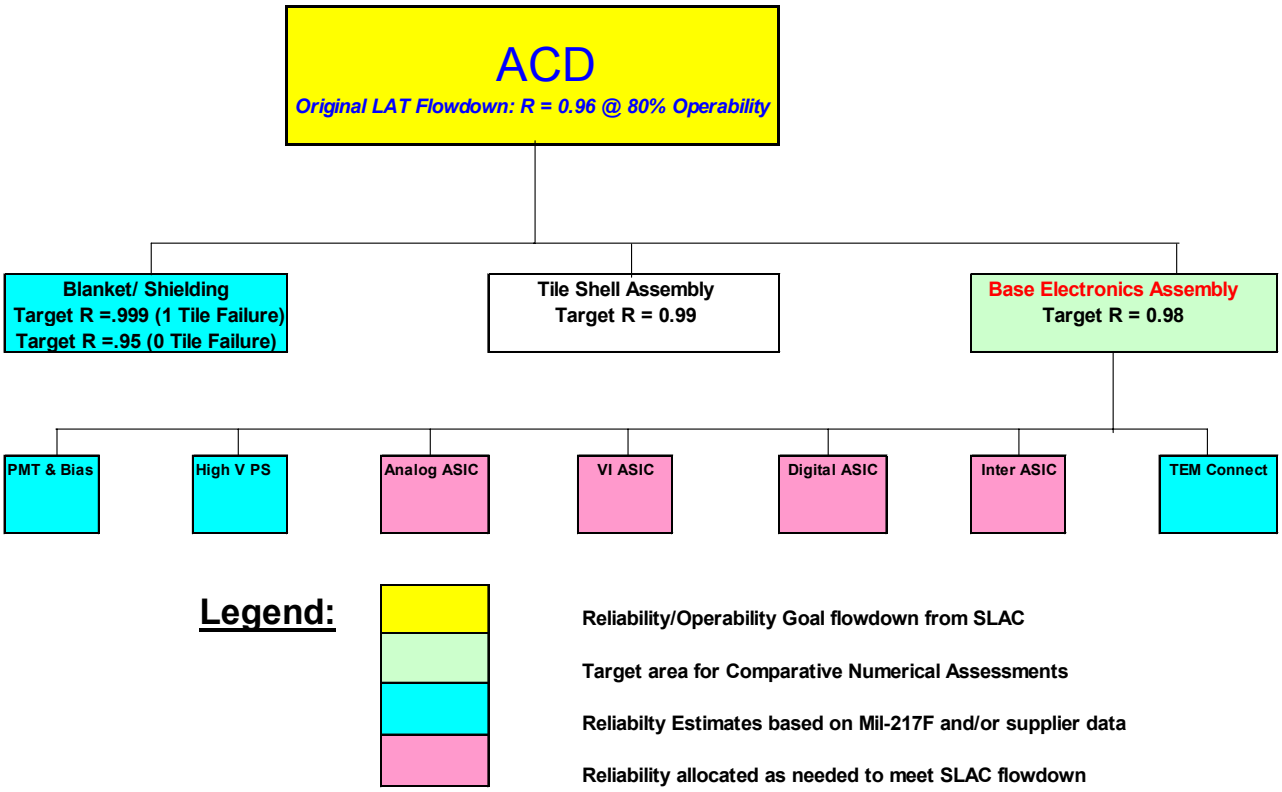


Figure 39. Reliability Allocation and Apportionment

12.1.3 Limited-Life Analysis

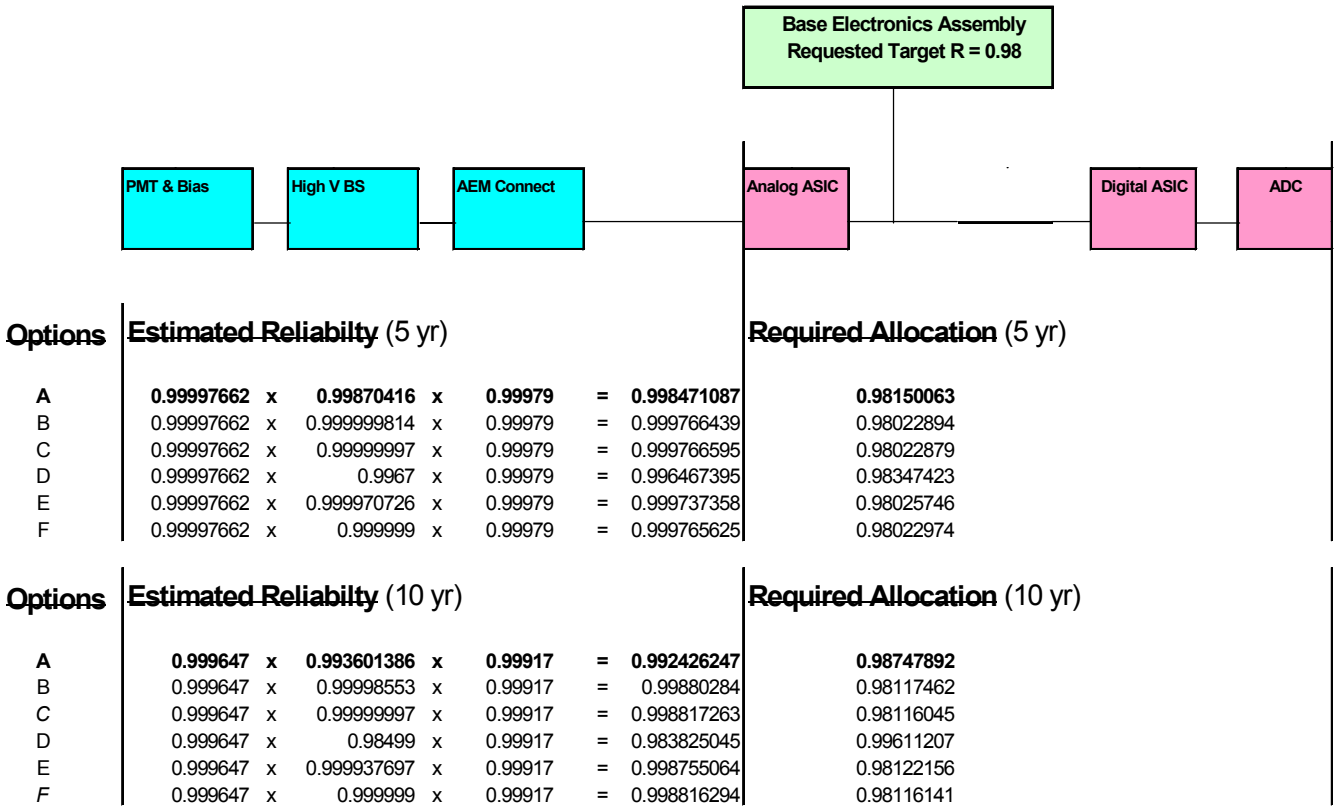
The limited-life analysis of the ACD is intended to identify all potential items with a useful life period that may be less than that required for the overall mission. The useful life period is initiated when an item is initially subjected to stresses that can degrade its life. For the PDR, a conservative approach is being taken by identifying all known items that may potentially have a limited life. As system design, integration, and testing continues; more information will be known about the potential limited-life items and further determinations will be made to establish which items should or should not be included in the corresponding limited-life list. Details relating to the subject analysis can be found in ACD-RPT-1250, "Limited-Life Items List."

12.2 Parts and Materials

12.2.1 Parts

The "LAT EEE Parts Program Control Plan" (PPCP), LAT-MD-00099-002, describes the LAT ACD electrical, electronic, and electromechanical (EEE) parts program. It summarizes the techniques and methods through which the EEE parts program will achieve maximum part reliability. This EEE parts program ensures that all parts used in the ACD design are of the highest available level of

reliability consistent with their functional requirements as well as program cost and schedule constraints.



Options	Estimated Reliabilty (5 yr)									Required Allocation (5 yr)
A	**0.99997662**	**x**	**0.99870416**	**x**	**0.99979**	**=**	**0.998471087**			**0.98150063**
B	0.99997662	x	0.999999814	x	0.99979	=	0.999766439			0.98022894
C	0.99997662	x	0.99999997	x	0.99979	=	0.999766595			0.98022879
D	0.99997662	x	0.9967	x	0.99979	=	0.996467395			0.98347423
E	0.99997662	x	0.999970726	x	0.99979	=	0.999737358			0.98025746
F	0.99997662	x	0.999999	x	0.99979	=	0.999765625			0.98022974

Options	Estimated Reliabilty (10 yr)									Required Allocation (10 yr)
A	**0.999647**	**x**	**0.993601386**	**x**	**0.99917**	**=**	**0.992426247**			**0.98747892**
B	0.999647	x	0.99998553	x	0.99917	=	0.99880284			0.98117462
C	0.999647	x	0.99999997	x	0.99917	=	0.998817263			0.98116045
D	0.999647	x	0.98499	x	0.99917	=	0.983825045			0.99611207
E	0.999647	x	0.999937697	x	0.99917	=	0.998755064			0.98122156
F	0.999647	x	0.999999	x	0.99917	=	0.998816294			0.98116141

Figure 40. Power Supply Reliability Tradeoff Study

ACD designs will incorporate GSFC-311-INST-001 Level 2 parts, minimizing the number of part type combinations and minimizing duplicate specifications and duplicate procurements actions. This GSFC document describes the selection, screening, and monitoring of EEE parts used in the hardware being built by subcontractors and vendors. The purpose of the EEE PPCP is to define criteria for selecting, screening, and qualifying ACD EEE parts.

In accordance with the LAT PAIP and EEE Parts Plan, the LAT Parts Control Board has the primary responsibility for conducting the parts and materials program for ACD flight parts. All LAT Parts Control Board functions will apply to the ACD hardware including:

- Controlling the management, selection, and standardization of LAT/ACD parts and materials
- Generating and maintaining the LAT/ACD Program Approved Parts List (PAPL) which, as the only source of approved parts for project flight hardware, may contain parts not actually in flight hardware design
- Ensuring that every part on the LAT/ACD PAPL meets the requirements of the LAT Program
- Dispositioning nonconforming parts, revolving part problems, and approving all LAT/ACD parts

The requirements of the LAT PPCP will be flowed down to ACD subcontractors and vendors. Each subcontractor and vendor will be evaluated for LAT PPCP compliance. All noncompliances to these requirements will be documented and dispositioned in Parts Control Board minutes.

ACD EEE parts will be approved for listing on the LAT/ACD PAPL before initiation of procurement activities. The final PAPL will be converted into the LAT/ACD Parts Identification List (PIL) that will list all parts included in the ACD flight hardware design. EEE parts used in ACD flight hardware will be selected in the order of preference as listed in the LAT-MD-00099-002, Section 6.0. All EEE parts will meet the radiation hardness requirements of the LAT Program including Total Ionizing Dose (TID), Single-Event Upset (SEU), and Single-Event Latch-up (SEL). All ACD EEE parts will be derated in accordance with the guidelines of the NASA Parts Selection List (NPSL) and the GSFC Preferred Parts List (PPL) 21 that are listed on the NASA Electronic Parts and Packaging Program website, <http://nepp.nasa.gov>.

All ACD electrical circuits will be analyzed to determine the maximum stress on each part when all applied voltages or currents are maximized and when all variations of other parts in the circuit are set to that combination of minimum and maximum values that produce worst-case maximum stress. The part stress analysis will verify that the derating requirements are met and documented on ACD schematics.

12.2.2 Materials

All parts and materials required for the manufacture and assembly of ACD hardware will be processed through receiving and inspection per the LAT PAIP; the "LAT Mechanical Parts Plan," SLAC LAT-SS-00107-1; and the "ACD Quality Plan," GSFC ACD-QA-8001. In accordance with these plans, traceability of individual parts or components or lots of parts/components will be accomplished using pertinent information about each lot material including flight or non-flight status, manufacturer, serial numbers, date codes, lot numbers, or other information. Quality assurance personnel, as required by the cited controlling plans, will segregate any material determined to be non-conforming for formal review by the LAT Parts Control Board. Acceptable material will be packaged and stored in a secured, environmentally controlled, segregated storage area following manufacturer recommendations. Materials that have a limited shelf life will be identified as specified in the above-cited plans.

12.3 Quality Control and Work Order Authorization (WOA)

12.3.1 Quality Control

The ACD Quality Assurance (QA) Program will cover ground and flight hardware and software. It will be conducted in accordance with the LAT PAIP. Additionally, ACD Safety and Mission Assurance activities at GSFC will adhere to the requirements and procedures mandated by GSFC's ISO 9001 system and/or described in the following GSFC documents:

a. GSFC ACD-QA-8001, "ACD Quality Plan"

b. GPG-5340.3, "Preparation and Handling of Alerts and Safe Alerts"

c. GSFC-GPG-5330.1, "Product Processing, Inspection and Test"

d. 302-PG-1410.2.1, "Goddard Non-Conformance Reporting and Corrective Action System Configuration Control Board (CCB)"

e. GPG-8621.1, "Mishap, Incident, and Close Call Investigation"

QA sign-off will be required for work order release or revision. QA will be responsible for verifying that needed inspection points and inspection instructions are provided. These identified points will be reflected through work order operation call out and supporting routing text. The QA Program for the flight hardware will not only include the standard inspection support but also such activities as operator/inspector training/certification, fabrication data records, Alert support, traceability, defect control documentation records, audits, and process controls.

12.3.2 Work Order Authorization (WOA)

In accordance with GSFC-GPG-5330.1, all ACD work performed at GSFC will be recorded on an approved WOA. This work will include, but not be limited to, box/component integration, functional testing, troubleshooting, environmental tests, and transporting/moving ACD hardware. WOA's will be initiated by Subsystem Leads and/or the I&T Manager or his/her designated representative. The WOA will specify the hardware items involved in the task, provide a brief description of the work to be performed, list the required documents, call out any hazards, and provide for the necessary approval signatures. Although the WOA form allows for short procedure steps to be included as part of the document in lieu of a separate formal procedure document, any attached procedures must be approved by the ACD I&T Manager, cognizant engineers, and QA. WOA's themselves must be approved by the appropriate engineers according to GSFC-GPG-5330.1. The WOA forms will be maintained by the ACD QA representative, including the log-in and sign-off of the work as completed.

12.4 Safety

The ACD Safety Program will be conducted in accordance with the "LAT System Safety Program Plan" (SSPP), LAT-MD-00078-01. The ACD safety team will develop documentation covering ACD safety issues as well as overall ACD-related information supporting the LAT System Safety Program. ACD safety activities will include:

- Defining the physical and functional characteristics of the ACD by employing the information available (e.g., design documents and operating procedures) and relating the interaction between people, procedures, equipment, and the environment
- Identifying all hazards related to all aspects of the ACD and determining their causes
- Assessing ACD-related hazards to determine their severity and probability and to recommend means for their elimination or control

- Implementing corrective measures to eliminate or control the individual hazards or accept their corresponding risks

- Conducting follow-up analyses to determine the effectiveness of preventive measures, address new or unexpected hazards, and issue additional recommendations if necessary

An ACD Preliminary Hazard Analysis, a detailed ACD subsystem description, and hazard descriptions for the ACD have been provided to the LAT System Safety Engineer as a part of this process. The ACD safety team will update the Preliminary Hazard Analysis as required.

12.5 Contamination Control

The ACD contamination control program will be conducted in accordance with the LAT PAIP, the LAT Contamination Control Plan, and the ACD Contamination Control Plan. The ACD subsystem will be fully integrated in a Class 100,000 HEPA filtered cleanroom facility that is in full accordance with these documents and FED-STD 209. External surface cleanliness levels will not exceed Level 750B per MIL-STD 1246 or 2 percent obscuration prior to inaccessibility of a surface. All internal surfaces will be vented away from star tracker and thermal control surfaces to minimize on-orbit deposition. The outgassing rate will be verified during component or system level vacuum testing.

All materials used in the cleanroom processing areas will be approved by contamination control and compatible with the above requirements. Garments will be 100% polyester with ESD grid, no Tyvek. Vinyl (e.g., PVC), rubber, or other high outgassing materials are prohibited from the cleanroom at all times. Gloves will be powder free CR100 latex, nitrile Chemsoft CE, or equivalent. Bagging film will be Llumalloy or equivalent approved material.

The ACD PMT's are sensitive to Helium. The ACD environment must be monitored for excess of normal levels of Helium. Provisions will be made for bagging and purging the ACD.

13 ACD ASSEMBLY, INTEGRATION AND TEST

The following sections provide a top-level flow for the assembly, integration and test of the ACD. The "LAT ACD Assembly, Integration, and Test", LAT-TD-00430, provides the detailed plans for the ACD.

13.1 Key Mechanical Components Assembly Flow

The only mechanical sub-assemblies that require a significant amount of assembly are the composite shell assembly, base frame, Tile Detector Assemblies, and Micrometeoroid Shield/Thermal Blanket. A brief description of the assembly sequence for each of these items follows.

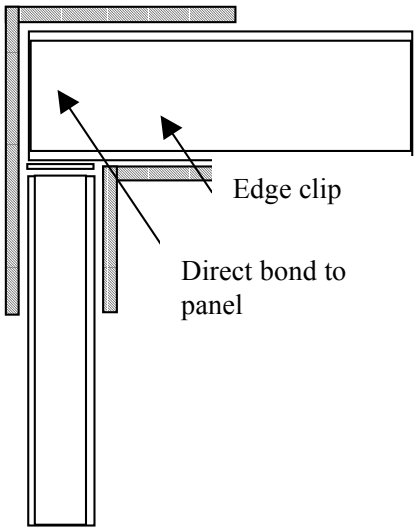


Figure 41. Typical Corner Joint

13.1.1 Composite Shell Assembly

- Fabricate honeycomb panels per specified design. Edges are filled with lightweight filler and trimmed to correct size.
- Fabricate inner and outer edge clips per specified design.
- Fabricate machined titanium inserts and flexures.
- Install (dry fit) the titanium inserts in the side panels.
- Build up the side panels on a template, which is on a surface table. Bolt the titanium inserts to the template. The template simulates the location of the flexure positions. Perform a dry fit check of the top panel.
- After final alignment verification, perform panel-to-panel bond for side panels. Bond edge clips, which join the side panels together and bond the titanium inserts in the honeycomb panels.
- Bond the top panel to the edge panels and bond on the outer edge clips.
- Turn the shell over, remove the template, and install the top inner edge clips.

13.1.2 Base Frame

- Machine Corner Fittings, Event Backplanes, and Channels.
- Install channels into the corner fittings.
- Using a template that simulates the LAT Grid corners, align the corner fittings.
- Verify that the center mount points on the channels are located properly.
- Install fasteners that attach the channels to the corner fittings (8 places).
- Install Event Backplanes and Closeout covers.

13.1.3 Tile Detector Assemblies

- Machine scintillator of specified thickness (10 mm +/-0.15 mm) to specified size.
- Machine grooves in the scintillator as specified.
- Polish the edges of the scintillator. This step may not be required if the edges are diamond milled.
- Anneal the scintillator using a temperature of 80^{o}C for three hours followed by a cool down to room temperature over an 8-hour period.
- For bent scintillators, bend to specified shape by using a warm temperature bending process

- Cut waveshifting fibers to specified lengths.
- Diamond mill one end of each fiber perpendicular to the fiber axis and vapor deposit aluminum on the milled ends of the fibers.
- To protect the aluminized surface, coat the aluminized fiber ends with a thin layer of Bicron BC-600 (or equivalent).
- Glue mirrored end of waveshifting fibers into grooved scintillator using Bicron BC-600 (or equivalent). The fiber ends shall be flush with the scintillator edge within 0.10 mm.
- Install and glue transmitting end of waveshifting fibers into GSFC supplied connector.
- Cut and polish (or diamond mill) the fibers and connector face perpendicular to the fiber axis.
- Anneal the scintillator and wave shifting fiber assembly using a temperature of 80^{o}C for three hours followed by a cool down to room temperature over an 8-hour period. A form will be required to hold the fibers in the correct position.
- Wrap tile with two layers of white Tetratex using GSFC specified tape or adhesive.
- Wrap tile and fibers with two layers of black Tedlar using GSFC specified tape or adhesive.
- Performance baseline test on the TDA.

13.1.4 Micrometeoroid Shield/Thermal Blanket

- Fabricate a template for the Micrometeoroid Shield/Thermal Blanket
- Cut the rough sizes for the MS/TB material
- Lay up the layers as specified by MS/TB design (i.e. Kevlar innermost layer, foam, Nextel, foam, Nextel, foam, ….., thermal blanket layers).
- Install mounting holes in the MS/TB.
- Ground and vent the MS/TB as required.

13.2 Key Electrical Components Assembly Flow

The only electrical sub-assemblies which require a significant amount of assembly are the FREE circuit card assembly, and HVBS. A brief description of the assembly sequence for each of these items follows.

This section describes the process to manufacture, produce and test the flight unit front-end electronics (FREE) circuit cards, the flight unit high voltage bias supply (HVBS), and the PMT biasing resistor network for the GLAST ACD. The FREE circuit cards are also known as the Event Processor.

13.2.1 FREE Circuit Card Assembly

- Fabricate and deliver to GSFC one development unit FREE circuit card
- Test separately the digital ASIC, analog ASIC and analog-to-digital converter (ADC)
- Populate the PCB at GSFC with all of the electrical components and some portion of non-flight photomultiplier tubes (PMT)

- Functionally test development unit FREE circuit card. The FREE circuit card test setup includes a PMT simulator for each PMT, that is programmable via software interface. Each FREE circuit card interfaces with an engineering model AEM for a ground test.
- Fabricate and deliver to GSFC four (4) engineering unit EU FREE circuit cards
- Populate at GSFC EU FREE circuit card PCBs. PMTs will be non-flight.
- Functionally test EU FREE circuit cards.
- Verification tests performed on EU FREE circuit card. Verification tests adhere to the tests specified by the GSFC General Environmental Verification Specification (GEVS) document.
- Functionally test EU FREE circuit cards.
- Manufacture and deliver to GSFC 14 FREE PCBs (12 flight unit, 2 spares) with coupons.
- Assemble and populate the 12 flight unit (FU) FREE circuit cards.
- Assemble and populate 2 spares FREE circuit cards
- Functionally test FU FREE circuit cards and spares
- Verification tests performed on 12 FU FREE circuit cards
- Functionally test FU FREE circuit cards
- Quality assurance inspection 12 FU FREE circuit cards.
- Conformal coat 12 FU FREE circuit cards.
- Integrate and test on the base frame assembly FU FREE circuit cards.

13.2.2 HVBS

- Purchase ICs and discrete components
- Fabricate and deliver to GSFC HVBS development unit (DU) circuit card PCB.
- Populate PCB with components.
- Fabricate and deliver to GSFC four fully assembled and populated engineering unit (EU) HVBS circuit cards.
- Functionally test EU HVBS circuit cards.
- Fabricate and deliver to GSFC 14 fully populated HVBS PCBs.
- Functionally test HVBS circuit cards
- HVBS circuit cards quality assurance inspection
- HVBS conformal coating.
- Integrate and test, on the base frame assembly, HVBS circuit cards.

13.2.3 PMT Biasing Resistor Network

- Fabricate resistor network PCBs
- Populate PCBs
- Solder onto PMTs
- Test PMTs

13.3 Integration and Test

13.3.1 ACD Instrument Development

Integration and test of the ACD will be done at GSFC. Instrument level I&T will be dealt with as it pertains to the instrument module I&T program at GSFC. A fully qualified ACD system will be delivered to the LAT instrument at SLAC. The I&T process will direct and assist ACD assembly and test, including characterization and environmental verification, see figure

Figure 42.

ACD system level integration begins when the flight mechanical support structure is delivered to I&T. Subsystem components of ACD are subject to protoflight or acceptance level structural, thermal, and EMC tests prior to ACD system integration. ACD system I&T sequence consists of a combination of performance and environmental testing used to verify the requirements set forth in the ACD verification documents. Integration of instruments will be done in conjunction with systematic testing of all system both functional and operational.

Three levels of testing shall be implemented: Engineering model (EM), Calibration Module, and Flight Module (FM). EM testing shall be performed on a small version of ACD – two strips of tiles and associated electronics. Acceptance testing shall be performed on Flight Unit. Calibration/characterization shall be performed under verified test procedures. The calibration program has three main functions: Test, Measurement, and Validate overall performance described in the "LAT ACD Assembly, Integration, and Test", LAT-TD-00430.

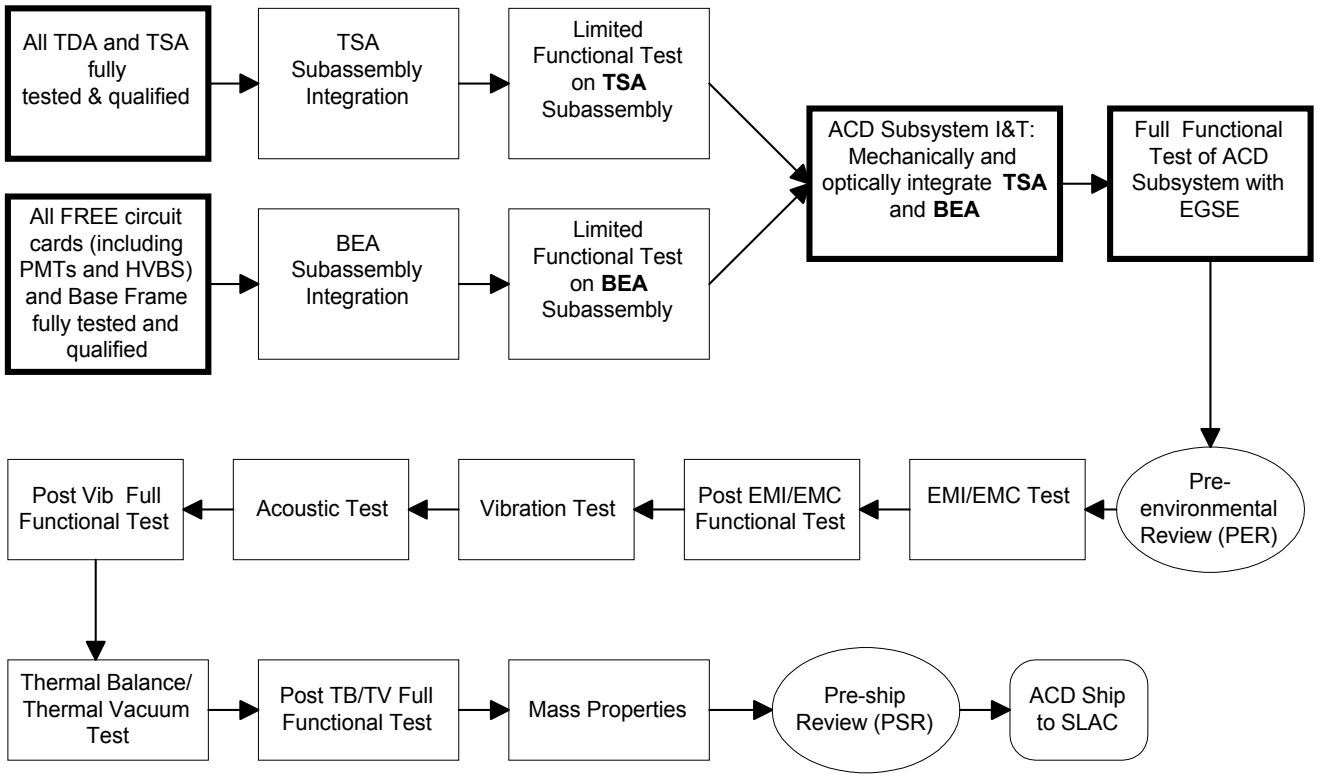


Figure 42. ACD Subsystem Integration and Test Flow

13.3.2 Environmental Tests

All ACD environmental tests shall be conducted at GSFC facilities. The exact levels and duration, the order of the tests, as well as any customizations to these tests, are described in "LAT ACD Assembly, Integration, and Test", LAT-TD-00430. Environmental tests list below are not necessary performed in the listed order. Unless specified, the tests are only performed on the ACD Flight Unit.

- Electromagnetic Compatibility (EMC)/ Electromagnetic Interference (EMI)
- Acoustic testing
- Vibration (vibration & shock) on both the EM and FM
- Thermal Vacuum (Thermal Balance, Thermal Cycling, Thermal Cal and/or Characterization)
- Mass Properties

13.3.3 ACD Support of LAT Instrument I&T

ACD shall be subjected to workmanship qualification, structural, and thermal prior to delivery for LAT I&T. Testing of ACD during LAT I&T will replicate and confirm functional tests that have already been done at subsystem level. The LAT Science Instrument I&T activities will be supported by ACD personnel, but it is currently budgeted for only three months support at SLAC when ACD is delivered. Any additional support will require additional funding. The following outlines those major portions of the I&T effort and involvement in ACD development program:

- Limited involvement during the integration & testing of ACD/LAT instrument at SLAC.
- Support aliveness, short and long form functional testing of ACD/LAT instrument and spacecraft at SLAC.
- Assist in calibration and characterization of instrument and observatory, writing and revising procedures and scripts for I&T related activities, and conducting instrument tests on ACD.

13.3.4 Mission I&T Support

Currently, there is no budget for ACD I&T team to support GLAST Mission I&T, except for consultation.

13.4 Ground Support Equipment

13.4.1 Mechanical Ground Support Equipment (MGSE)

The requirements for the ACD MGSE can be found in ACD-REQ-7002. There are six main pieces (or groups) of MGSE: the BEA dolly, TSA dolly, ACD multi-purpose lift sling, ACD multi-purpose test fixture, ACD templates, and ACD mass simulators. The following is a brief description of each piece of MGSE.

- BEA dolly: The BEA dolly has to support and transport the BEA during the integration and testing of the BEA. It will also be used as the ACD instrument dolly.

- TSA dolly: The TSA dolly will support and transport the TSA during its integration and testing. It will have the same basic design as the BEA dolly, however the attachment points will different from the BEA dolly.

- ACD Multi-Purpose Lift Sling (MPLS): The ACD MPLS will be used to lift the ACD Instrument, BEA, and TSA. If the ACD MPLS can not be used at SLAC because of limited crane hook height, an additional special lift sling will be required.

- ACD Multi-Purpose Test Fixture: This test fixture will be a simulation of the LAT Grid. Therefore it will provide the same mounting points as the LAT Grid. It will be used for vibration and thermal/vacuum testing of the ACD. For the thermal vacuum test a combination of heaters and temperature-controlled tubes will be used to control the temperature of the fixture. This will allow the fixture to simulate the operating temperature of the LAT Grid.

- ACD templates: Templates will be required to position and install the flexure inserts on the composite shell and to locate the TDA's on the composite shell. The same template that is used to install the flexure inserts in the composite shell can also be used to locate and drill the interface holes in the base frame.

- ACD mass simulators: Mass simulators for the TDA's, Event boards, and MS/TB will be required for qualification testing of the flight structure. In addition to these mass simulators, a mass simulator of the ACD instrument will be required to test the shipping container isolation system.

13.4.2 Electronics Ground Support Equipment (EGSE)

There are four main pieces (or groups) of EGSE: AEM's, Event Simulator, HVBS Test Fixture and ASIC test stations. The following is a brief description of each piece of EGSE.

- Five AEM's are needed from the LAT team for FREE circuit card development and I&T. The AEM's should include three NT workstations for using the AEM's.

- Event Simulator for FREE circuit cards. This unit will simulate the input of the 18 PMT's for the FREE circuit card, allowing timing, coincidence, and spectroscopy tests to be performed on the electronics. This unit is a custom-designed circuit board assembly, a computer (& software), and laboratory test equipment, such as pulse generators, multimeters, and oscilloscopes. This is need prior to functional testing of the FREE circuit cards.

- High Voltage Bias Supply Test Fixture. This GSE is required to test the flight HVBS prior to integration with the BEA. This is needed prior to vacuum testing the HVBS.

- ASIC Test Stations (2). We will require a test station for the evaluation of the analog ASIC and a test station for the evaluation of the digital ASIC. This will be a combination of a custom-designed circuit board with a computer and COTS lab equipment. This is needed for the screening of the ASICs.

14 ACD KEY MILESTONES AND SCHEDULE

14.1 Key Level III and Level IV Milestones

Level III Key Milestones - interfaces to other subsystems

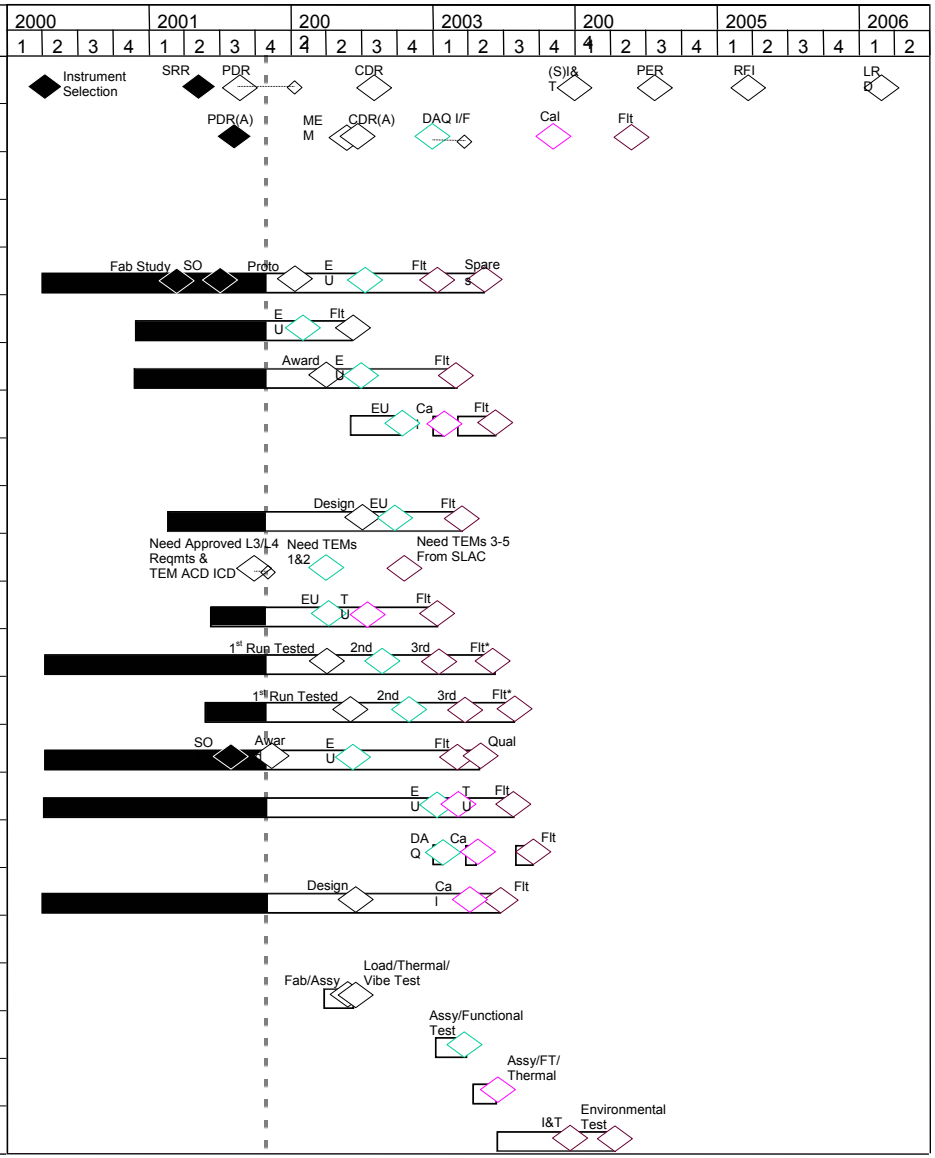
Prototype ACD Electronics Module received	3/15/02
First EGSE system received	3/15/02
Deliver prototype high voltage bias supply	6/03/02
Deliver prototype test/screening board with ASIC for electronics interface testing	7/01/02
Deliver calibration unit description	1/03/03
Fit test of ACD BEA with grid	5/08/03
Deliver ACD calibration unit components	10/31/03
Deliver tested flight unit ACD	4/26/04

Selected Level IV Key Milestones - Internal ACD Development Process

First qual unit photomultiplier tubes received	3/01/02
First run analog ASICs received	3/07/02
Test of first digital ASICs complete	6/12/02
ETU TDA's tested	7/02/02
Flight Tile Detector Assemblies received	9/19/02
Flight high voltage bias supplies complete	1/14/03
Flight Shell complete	2/07/03
Flight Tile Detector Assembly testing complete	3/17/03
Flight base frame complete	3/19/03
Flight tile shell assembly integration/test complete	8/25/03
Flight base electronics integration/test complete	10/09/03
Flight Unit ACD environmental tests complete	3/30/04

14.2 Schedule

ID	Task Description
1	LAT Instrument Milestones
2	Anti-Coincidence Detector Milestones
3	
4	Tile Shell Assembly (TSA)
5	Tile Detector Assembly (TDA)
6	Fiber Extension Cables
7	Shell Assembly
8	TSA Assembly/Test
9	Base Electronics Assembly (BEA)
10	Base Frame Assembly
11	Front End Electronics (FREE)
12	High Voltage Power Supplies
13	Analog ASIC
14	Digital ASIC
15	Photo-multiplier Tube (PMT)
16	FREE PWA
17	BEA Assembly/Test
18	Micrometeoroid Shield/Thermal Blanket Assy
19	ACD Assembly, Integration & Test
20	Mechanical Engineering Model (MEM)
21	DAQ I/F Test Unit
22	Calibration Unit
23	Flight Unit



* Note: Flt Run ASIC's (If Necessary)

Rev 5 – 10/31/01