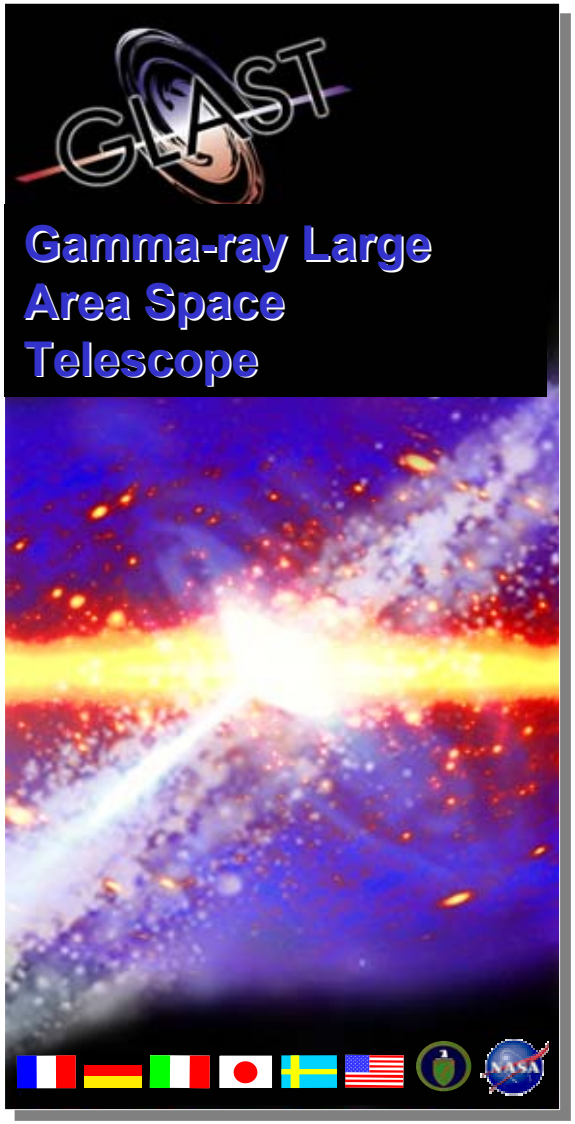


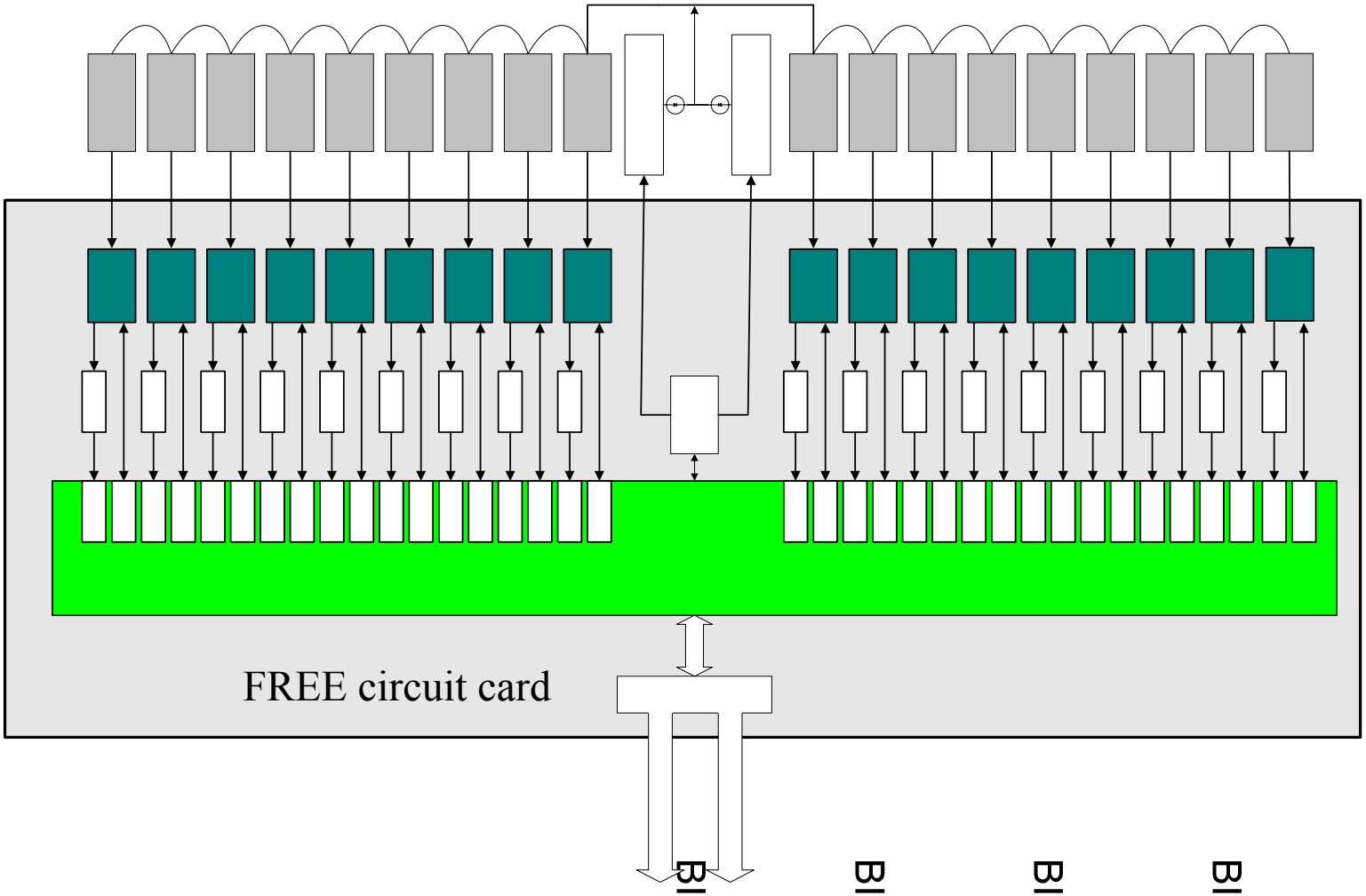
GLAST Large Area Telescope:

AntiCoincidence Detector (ACD)
Electrical Subsystem Review

ACD Electrical Subsystem - Overview

- 194 Independent electrical channels
- Six primary and six secondary Front-End Electronics (FREE) circuit cards
- One High Voltage Bias Supply (HVBS) per FREE circuit card. Request to change to two HVBS
- Up to 18 Photomultiplier Tube (PMTs) per FREE circuit card
- One resistor network per PMT

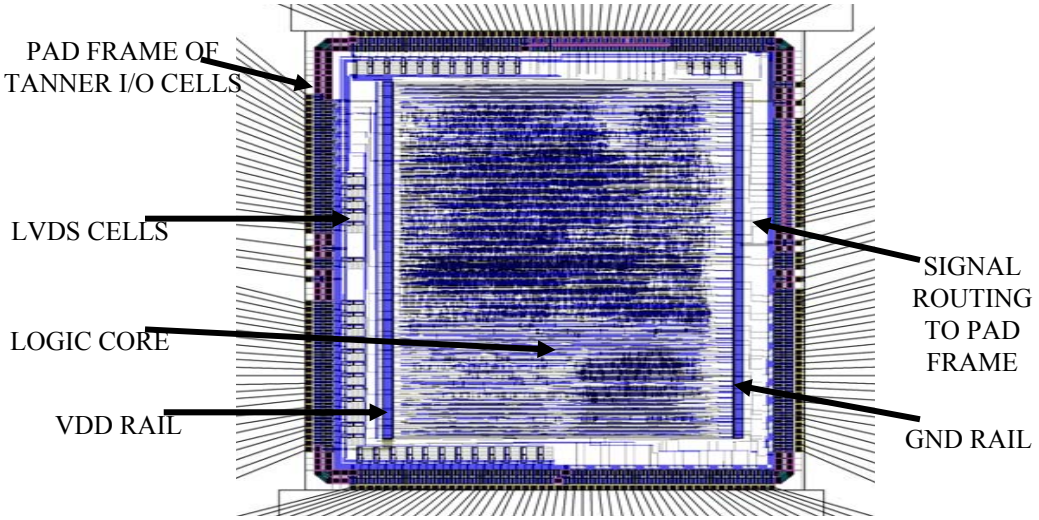
ACD Electrical Subsystem - Block diagram



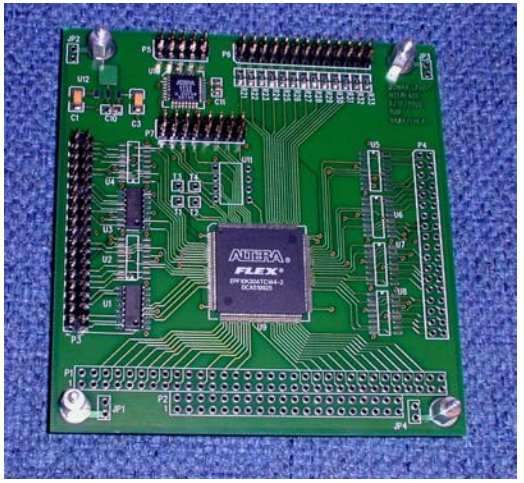
ACD Electrical Subsystem – Component Status

Components	Function	Status
HVBS	Requires +28 V supply; Outputs 0 V to 1500 V	Designed and ready for fabrication; Awaiting electronics packaging design completion
GAFE	Receives PMT signal output; Generates VETO signals Track and Holds PMT signal pulse height	1st generation in testing; 2nd generation at the foundry
GARC	Processes all commands from ACD Electronics Module (AEM) Transmits all ACD data to AEM Provides commands and control to the GAFE and HVBS	1st generation design completely emulated in an FPGA 1st generation at the foundry

GARC Development



GARC Layout



Front End Electronics (FREE) emulator. FPGA implementation of GARC

GARC test board

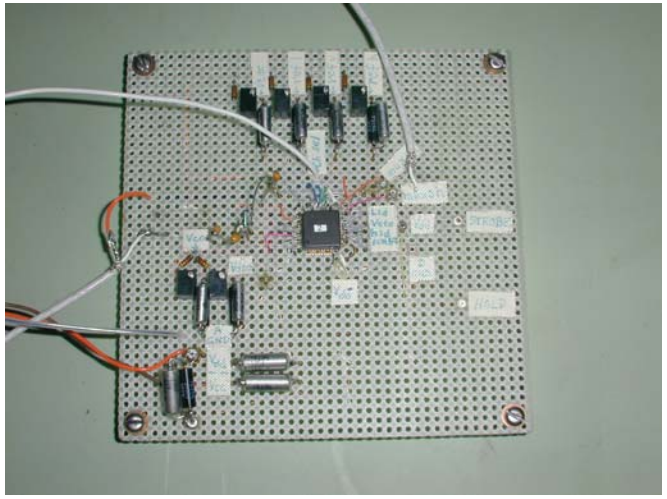
Held design review at GSFC in July ’02 – no serious issues

First generation is due August ‘02.

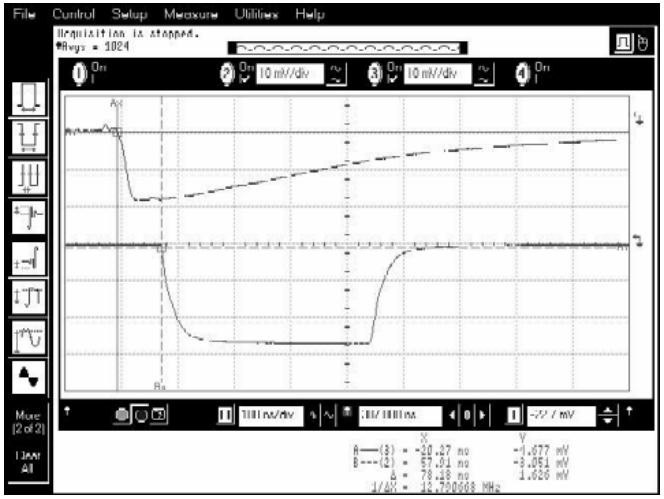
FPGA implementation was tested.

FREE FPGA emulator board is successfully communicating with the AEM at SLAC and GSFC

GAFE Development



Preliminary test set-up for ACD first-generation analog ASIC (GAFE)



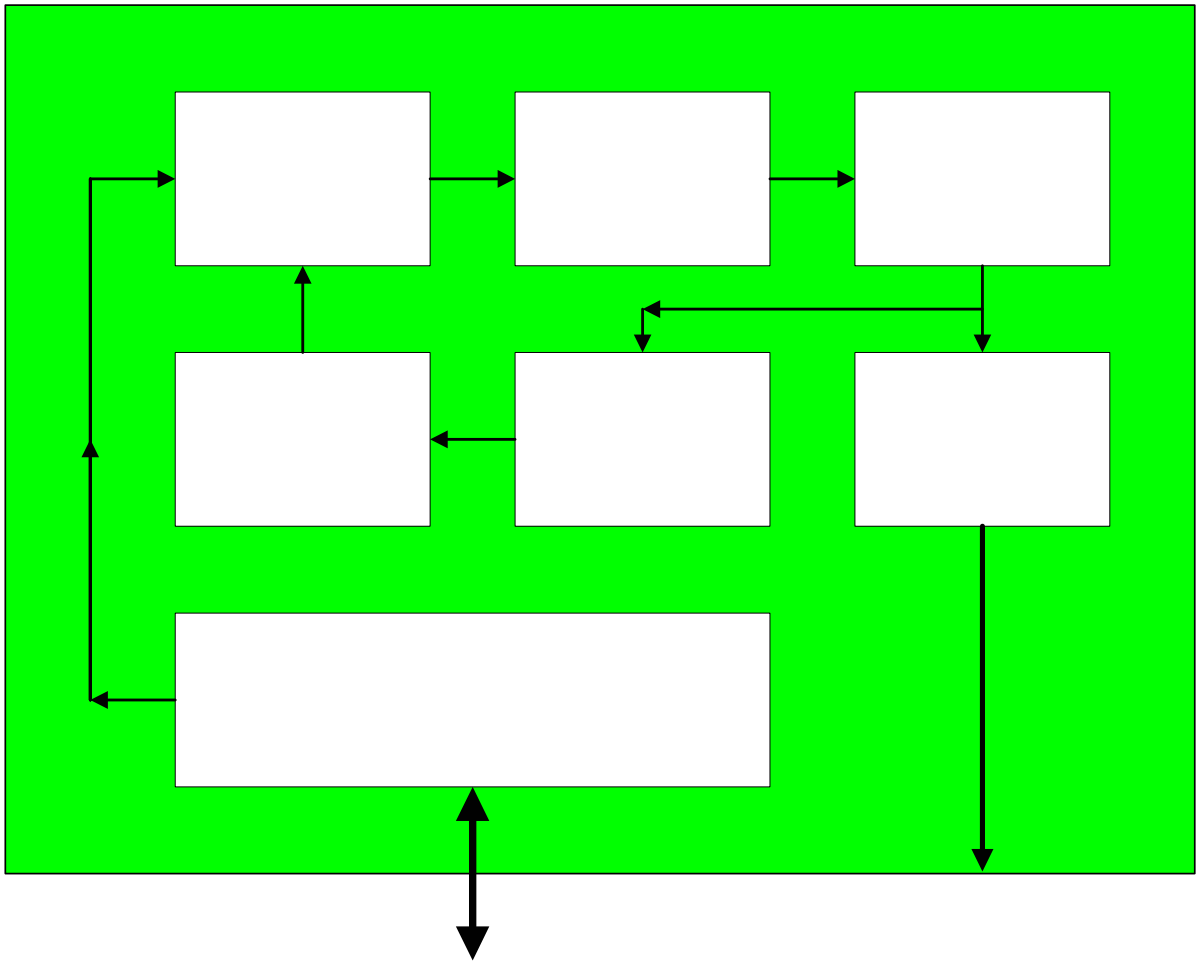
VETO output from a 1 MIP signal input to the GAFE.

Held design review at GSFC in July ’02 – no serious issues

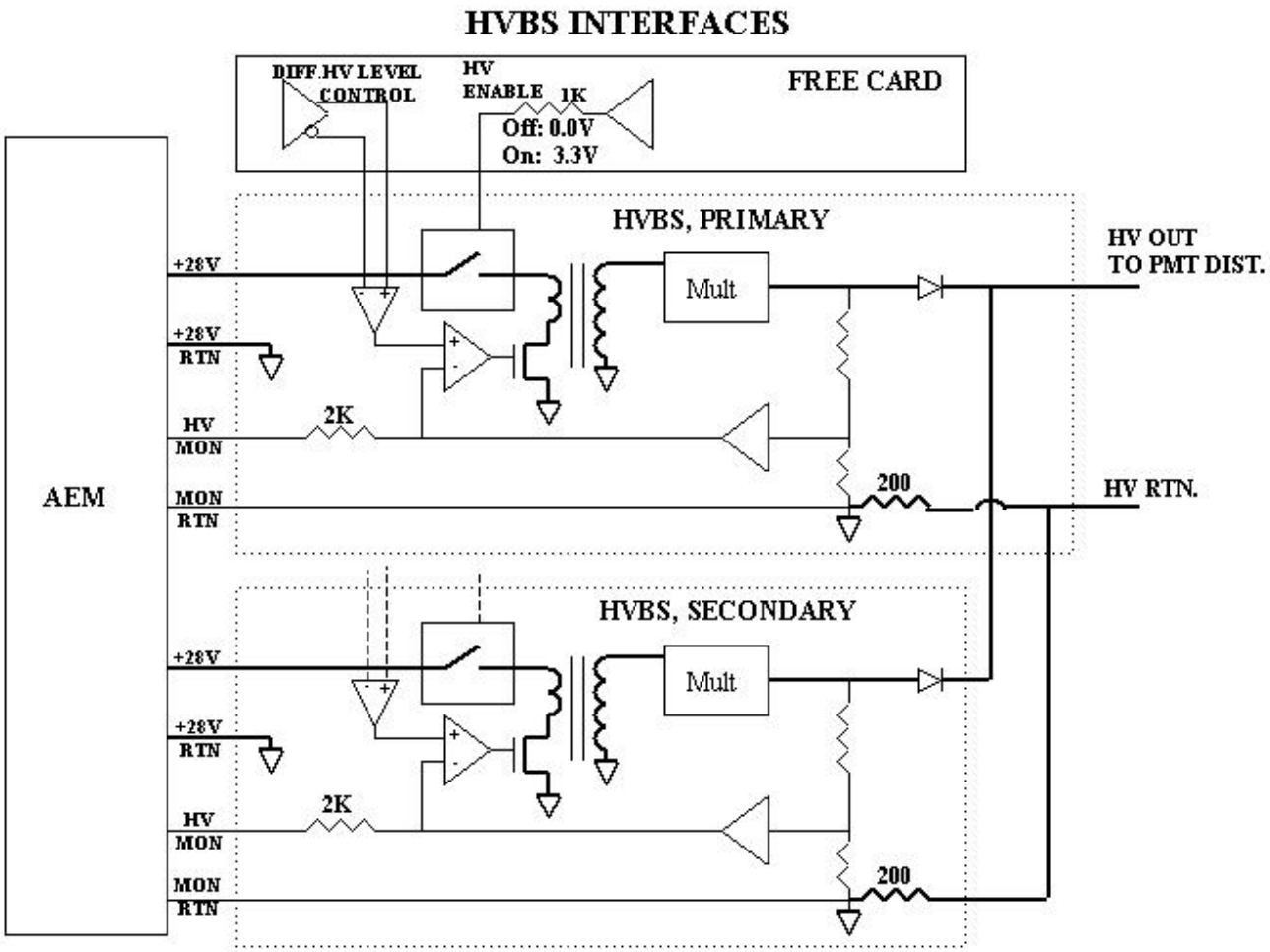
First generation: VETO and noise measurements of the analog section meet specifications. Some problems in the digital section and in the low-gain PHA linearity (secondary function)

Second generation is due in August ‘02.

High Voltage Bias Supplies



HVBS Interfaces



Electrical Subsystem – Schedule

Components	Completion Date
HVBS	
• Development Unit Testing	8/26/02
• Engineering Unit testing	1/21/03
• Flight Unit ready for I&T	7/14/03
GAFE	
• 1st Generation fabrication	10/26/01
• 2nd Generation fabrication	5/13/02
• 3rd Generation fabrication	9/23/02
• Flight unit fabrication	3/03/03
GARC	
• 1st Generation fabrication	5/13/02
• 2nd generation fabrication	9/23/02
• Flight unit fabrication	3/03/03

Components	Completion Date
Resistor Network	
• Engineering units testing	7/08/02
• Flight units ready for I&T	7/30/03
PMT subassembly	
• Engineering unit testing	8/12/02
• Flight units ready for I&T	10/09/03
FREE Circuit Card	
• Development Unit Testing	11/06/02
• Engineering Unit testing	4/24/03
• Flight Unit ready for I&T	12/01/03
Float	15 weeks

- **End of Presentation**

ASIC Design Review - GARC

Issues/recommendations	Status
Power trace width might not meet process specs	G. Haller checked with Agilent and it is OK.
State machine design could be susceptible to SEU. Encode using One-hot or Triple Modular Redundancy (TMR)	Current design is acceptable because the SEU rate is negligible.
LVDS drivers are more sensitive to latch-up because of the higher current. Radiation test should be performed	All ASICs will undergo radiation testing

ASIC Design Review - GAFE

Issues/ Recommendations	Status
Resistors are constructed in N-wells. Use poly resistors for better performance.	Being investigated (need more ASIC area)
High-value resistors that are used for charge splitting should be reduced	Being investigated
Investigate the system level noise	Current noise spec is 5x less than 0.1 MIP threshold (400 μV). Measured shaping amp output is 1.3 mV.
Pulse height analysis accuracy will vary with temperature, signal level and power	Thermal cycling. Measured 6% to 6.5% variation of gain over temperature range.