Peer Review of the ACD Subsystem in Preparation for the LAT Instrument PDR

July 26, 2001

ACD Science, Management & Engineering Team
Goddard Space Flight Center

Peer Review Agenda

• Introduction and Overview	Ormes/Larsen	9:00 - 9:45
• Detector Design	Moiseev	9:45 - 10:45
• Break		10:45 - 11:00
• Mechanical/Thermal Design	Johnson	11:00 - Noon
• Electronics Design	Sheppard	1:00 - 2:00
• Safety & Mission Assurance	Huber	2:00 - 2:30
• Subsystem Integration & Test	Lindsay	2:30 - 2:45
Calibration & Operation	Larsen	2:45 - 2:50
• Status & Schedule	Larsen	2:50 - 3:10
• Discussion & Action Items	All	As required

Large Area Telescope (LAT) Design Overview

Instrument

16 towers ⇒ modularity

height/width = 0.4 ⇒ large field-of-view

Tracker

Si-strip detectors: 228 μm pitch, total of 8.8 x 10^5 ch.

Calorimeter

hodoscopic CsI crystal array

⇒ cosmic-ray rejection

⇒ shower leakage correction

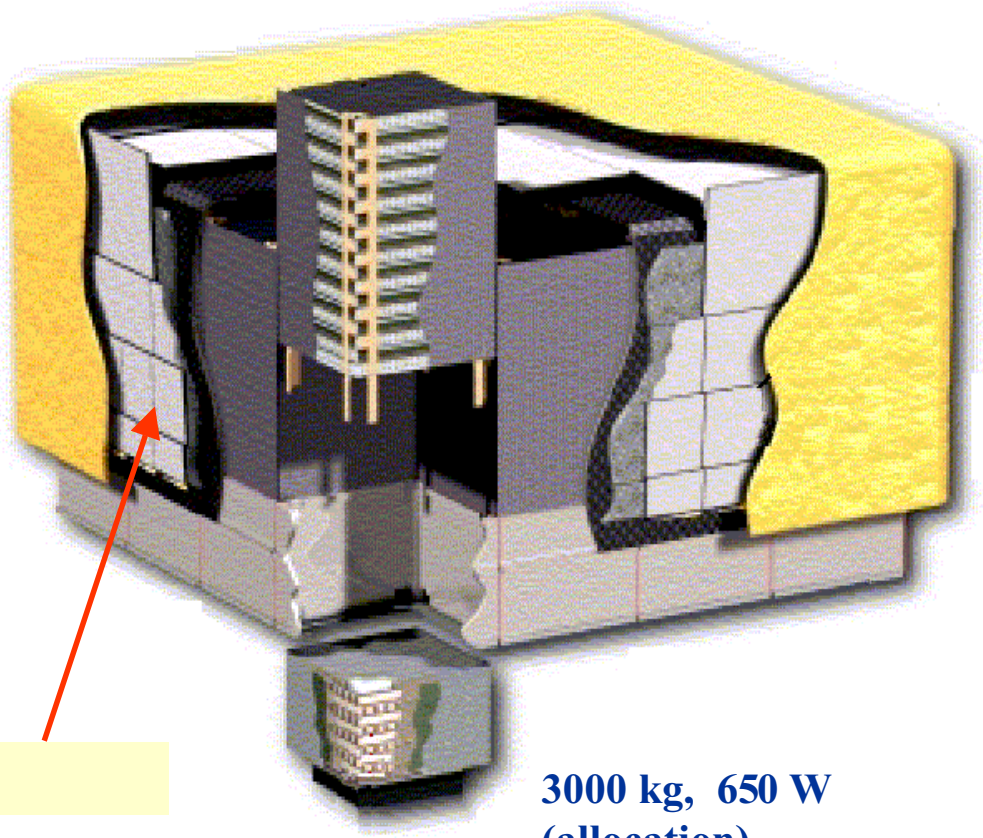
$X_{Tkr + Cal}$ = 10 X_0 ⇒ shower max contained < 100 GeV

Anticoincidence Detector

segmented plastic scintillator

⇒ minimize self-veto

> 0.9997 efficiency & redundant readout



3000 kg, 650 W (allocation)

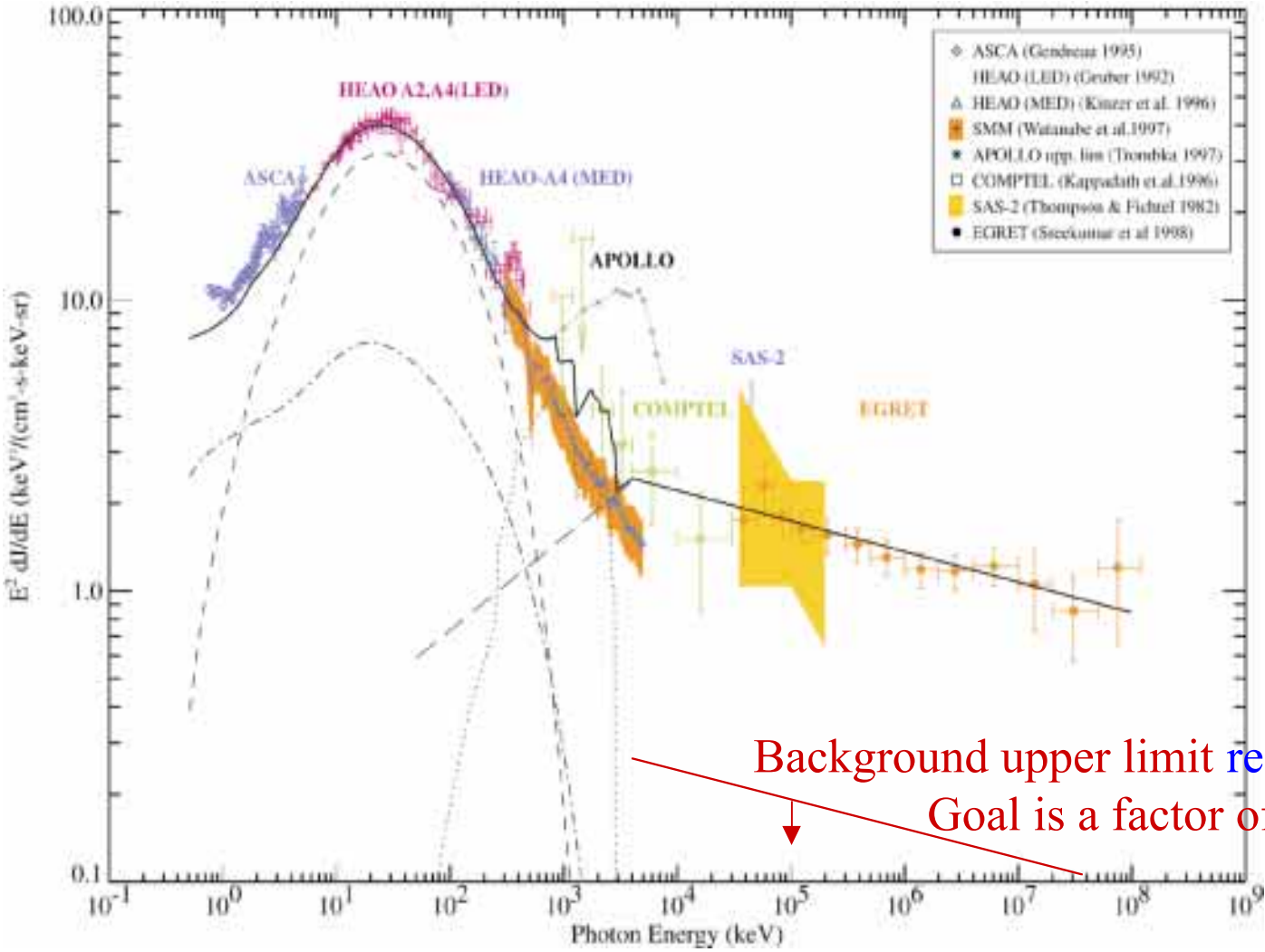
1.75 m × 1.75 m × 1.0 m

20 MeV – 300 GeV

ACD: The First Line of Defense Against Background

- The purpose of the ACD is to detect incident cosmic ray charged particles that outnumber cosmic gamma rays by more than 5 orders of magnitude. Signals from the ACD can be used as a trigger veto or can be used later in the data analysis. The optimal use of ACD is topic dependant.
  - High latitude extra-galactic diffuse studies and gamma-ray line searches require very low background and long integration times.
  - Studies of bright time-variable sources may not be background limited.
- EGRET coverage at high energy was limited by backsplash. This is the first time a segmented anticoincidence detector will have been built for space flight.
  - Self-veto and hence ACD segmentation affects both projected effective area A_p and geometry factor $A\Omega$, "G"
- A flexible system design will help make GLAST a powerful next generation instrument.

Cosmic Diffuse Background

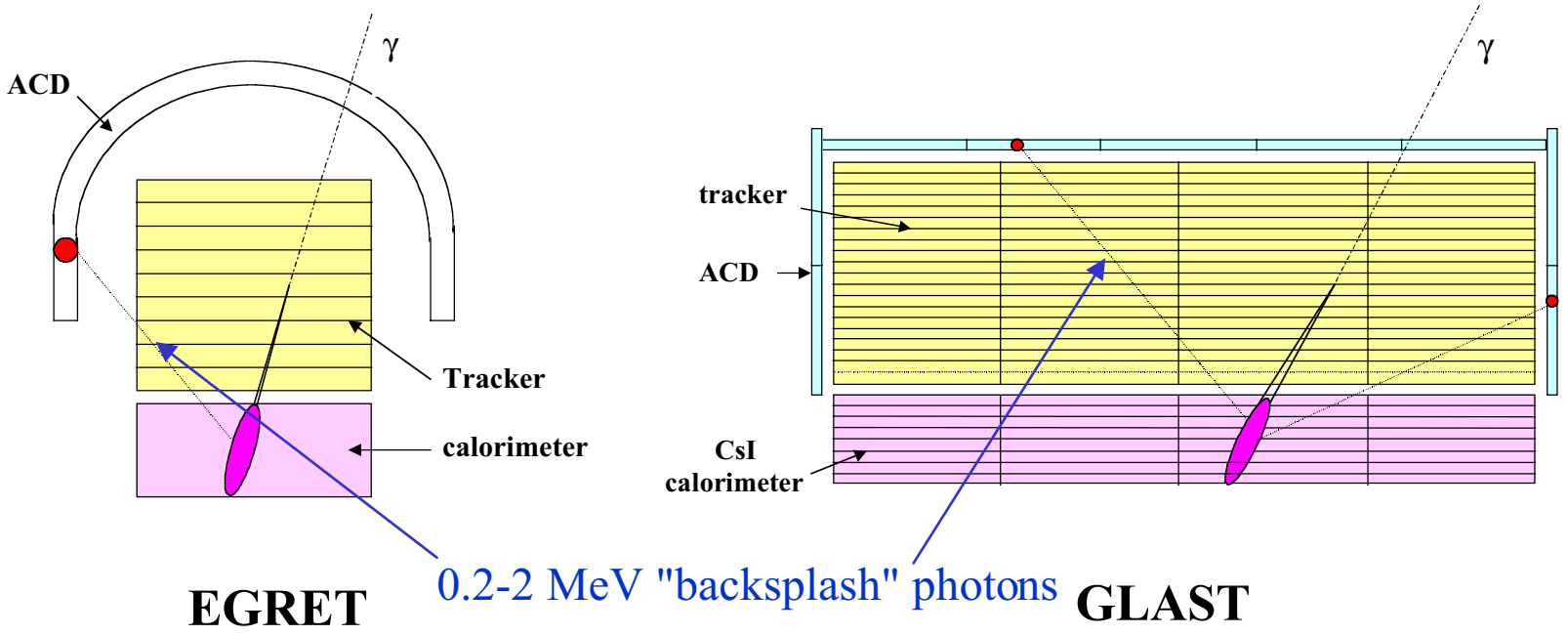


Approach: Divide and Conquer

Backsplash reduced the EGRET effective area by 50% at 10 GeV compared to 1 GeV.

GLAST will be studying photons to above 300 GeV.

Anticoincidence Detector for GLAST is subdivided into smaller tiles to avoid the efficiency degradation at high energy.



LAT Science Requirements Related to the ACD

From the Science Requirements Document (433-SRD-0001)

- LAT shall have a background rejection capability such that the contamination of the observed high latitude diffuse flux (assumed to be 1.5 x 10^{-5} cm^{-2} s^{-1} sr^{-1}) in any decade of energy (>100 MeV) is less than 10% (goal of 1%).
  - This implies the LAT must be capable of identifying and removing background with a rejection efficiency of 0.99999 with a goal of 0.999999. It applies to the more abundant protons.
    - Pattern recognition in the calorimeter and tracker are powerful in rejecting protons.
    - Electrons drive the ACD efficiency requirements.
- LAT shall have broad energy response from 20 MeV to at least 300 GeV. LAT shall have an energy range goal of 10 MeV to 500 GeV. LAT shall have an energy range minimum of 30 MeV to 100 GeV.
  - Implications for the ACD: backsplash at high energies cannot adversely impact the LAT performance.

Electron (e^-) backgrounds

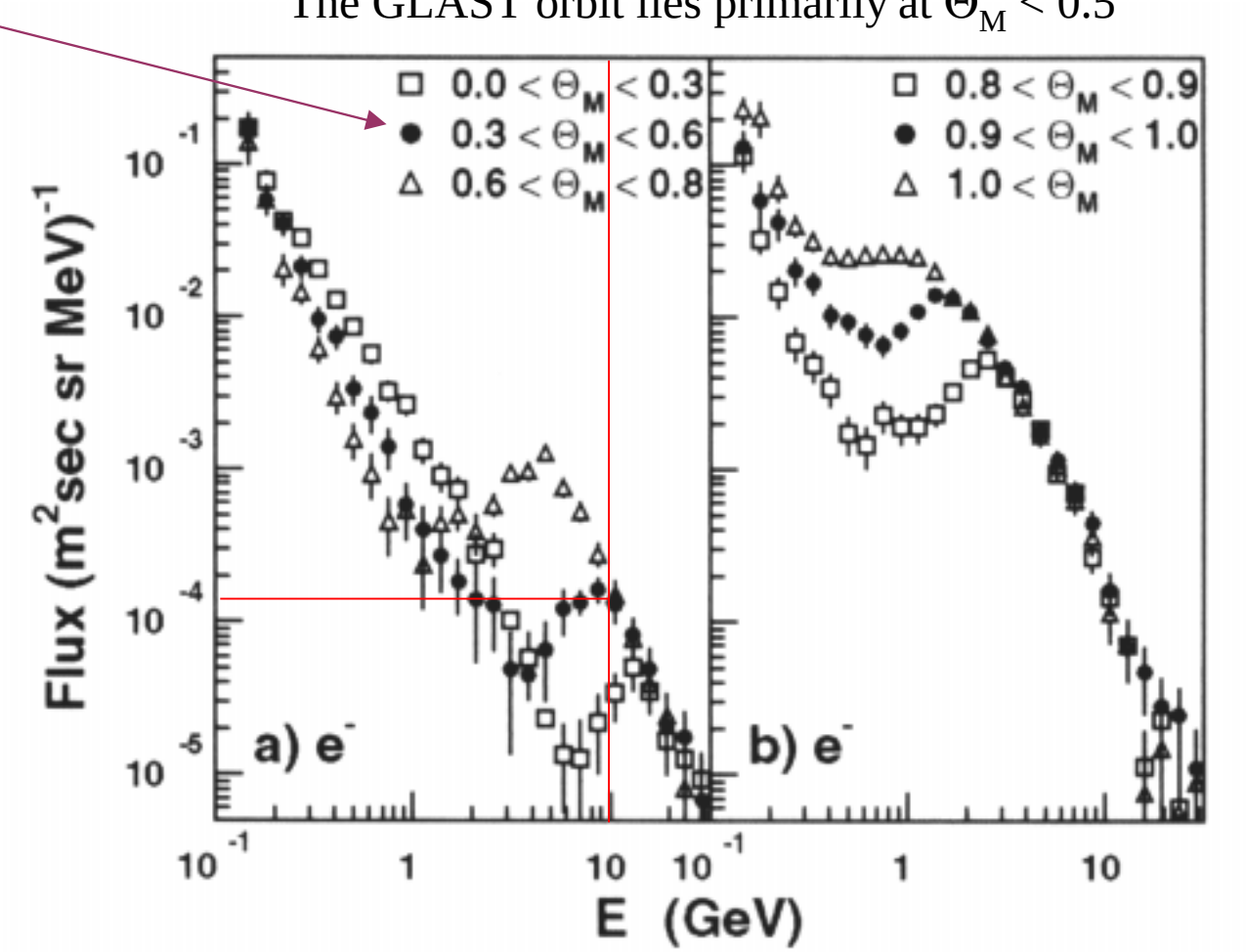
These guys!!

The GLAST orbit lies primarily at $\Theta_M < 0.5$

At latitudes < 28° degrees, galactic cosmic ray electrons are the most problematic background!

AMS has made an accurate measurement of this component.

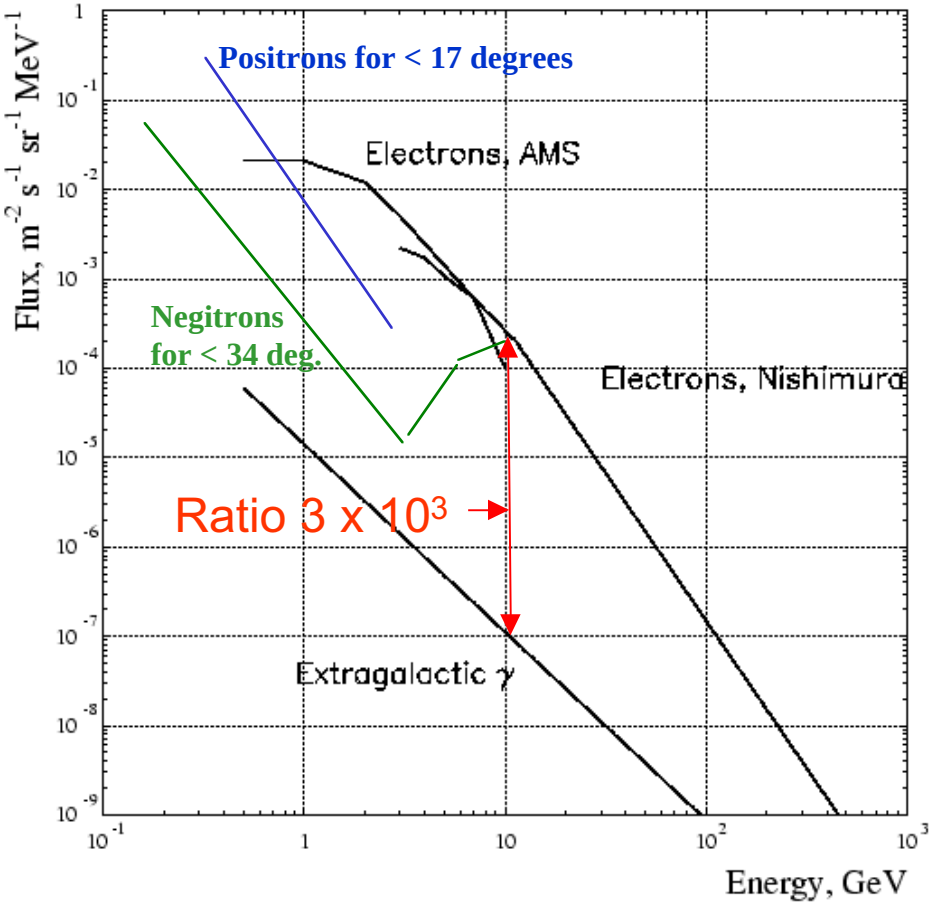
1.4×10^{-4} electrons per (m^2 sr s MeV) at 10 GeV



Alcaraz et al. 2000, Phys. Lett. B **484**, 10

ACD Efficiency Requirement

- Cosmic ray electrons of 10 GeV drive the background rejection requirement
  - Assumes no help from the calorimeter
- Recent measurements with AMS agree with those from Nishimura
  - Positrons at few 100 MeV near the equator might also be a problem
- Requirement is 10% below the extragalactic diffuse γ-ray flux
- Remove 1-10 GeV electrons
  - Flux ratio 3 x 10^3
- Requirement: 1.- 3.x10^{-5} = 0.99997
  - Goal: 1.-3.x10^{-6} =0.999997
- Outermost Tracker layer: 0.9
  - ACD efficiency: 0.9997



To reach our goal we need another factor of 10 from pattern recognition.

ACD Science Requirements

Driving requirements

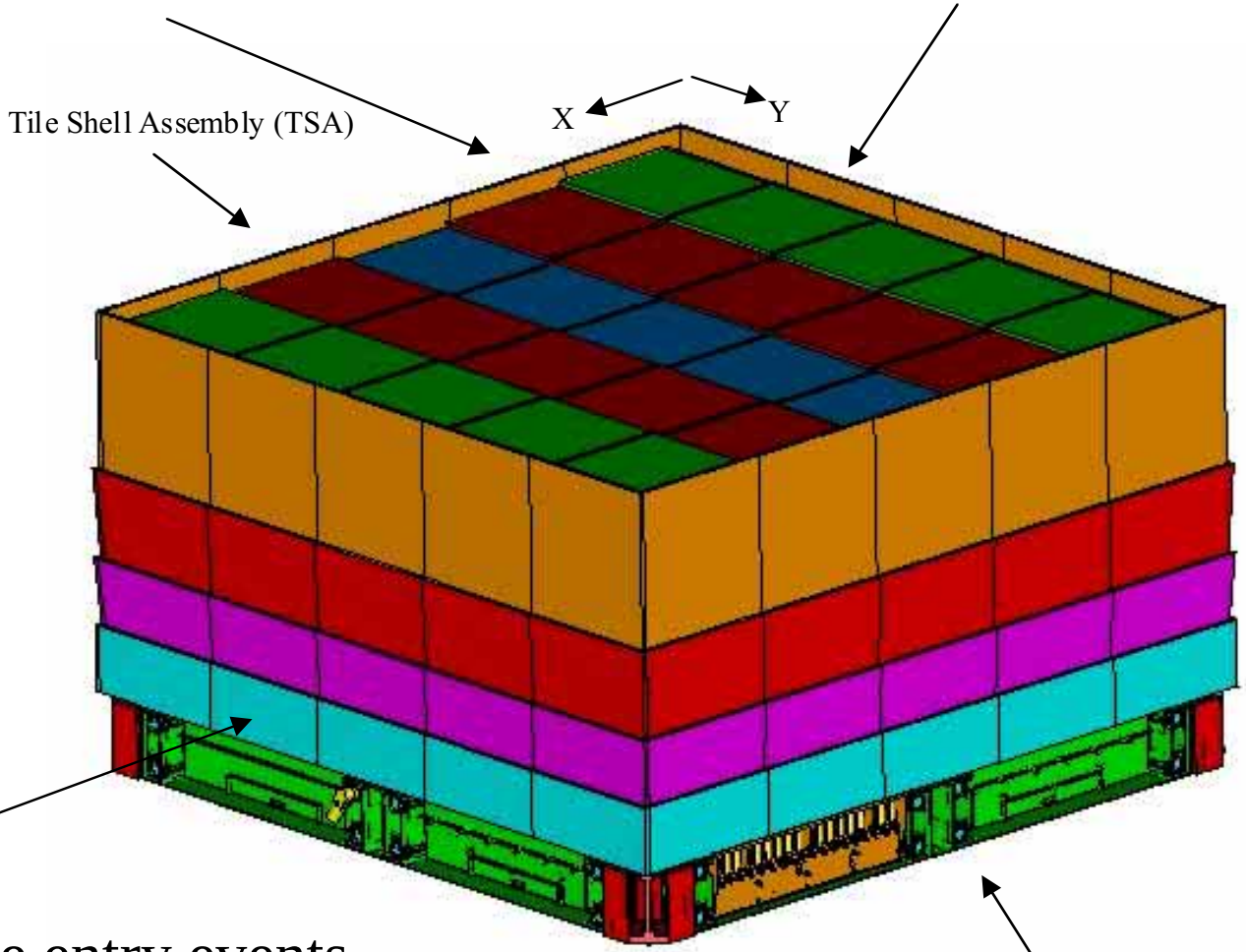
- Detect charged particles hitting the top and sides of the LAT, down to the top of the calorimeter, with a detection efficiency of 0.9997.
  - Combined with the tracker and calorimeter data, this efficiency results in a net LAT particle rejection efficiency of 0.99999 (miss 1 in 10^5) as stated in the Science Requirements Document.
- Reject no more than 20% of otherwise-accepted gamma-rays due to self-veto caused by backsplash for all energies up to 300 GeV.
  - We determine segmentation at 300 GeV, the worst case.
  - Meeting goal (500 GeV) would require 50% more tiles 2/3 present size.

Secondary

- Absorb less than 6% of the incident high-energy gamma radiation, in order to maintain the required LAT effective area.
- Provide a signal identifying heavy cosmic rays (carbon or heavier), for the purpose of calorimeter calibration.

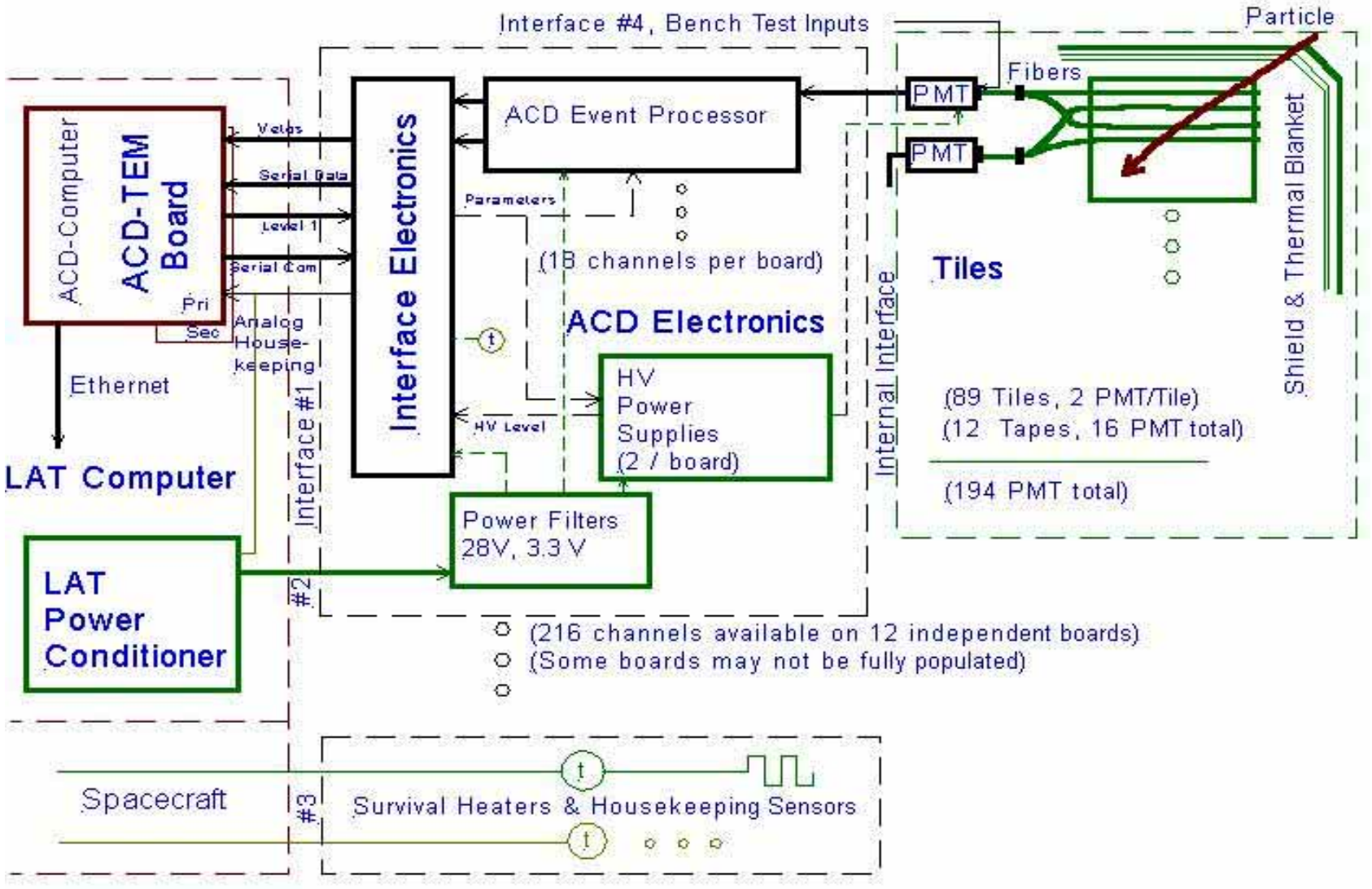
Design

Lip to "hide" thermal blanket and micro-meteorite shield



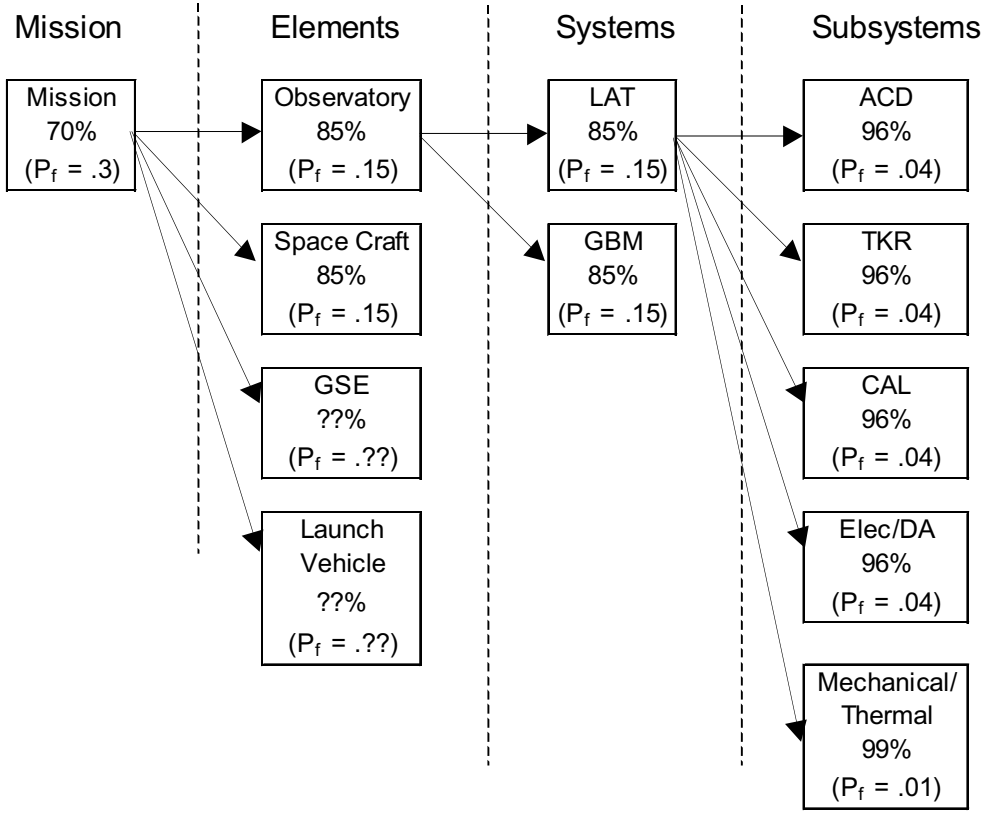
Segmentation for side entry events

ACD Block Diagram



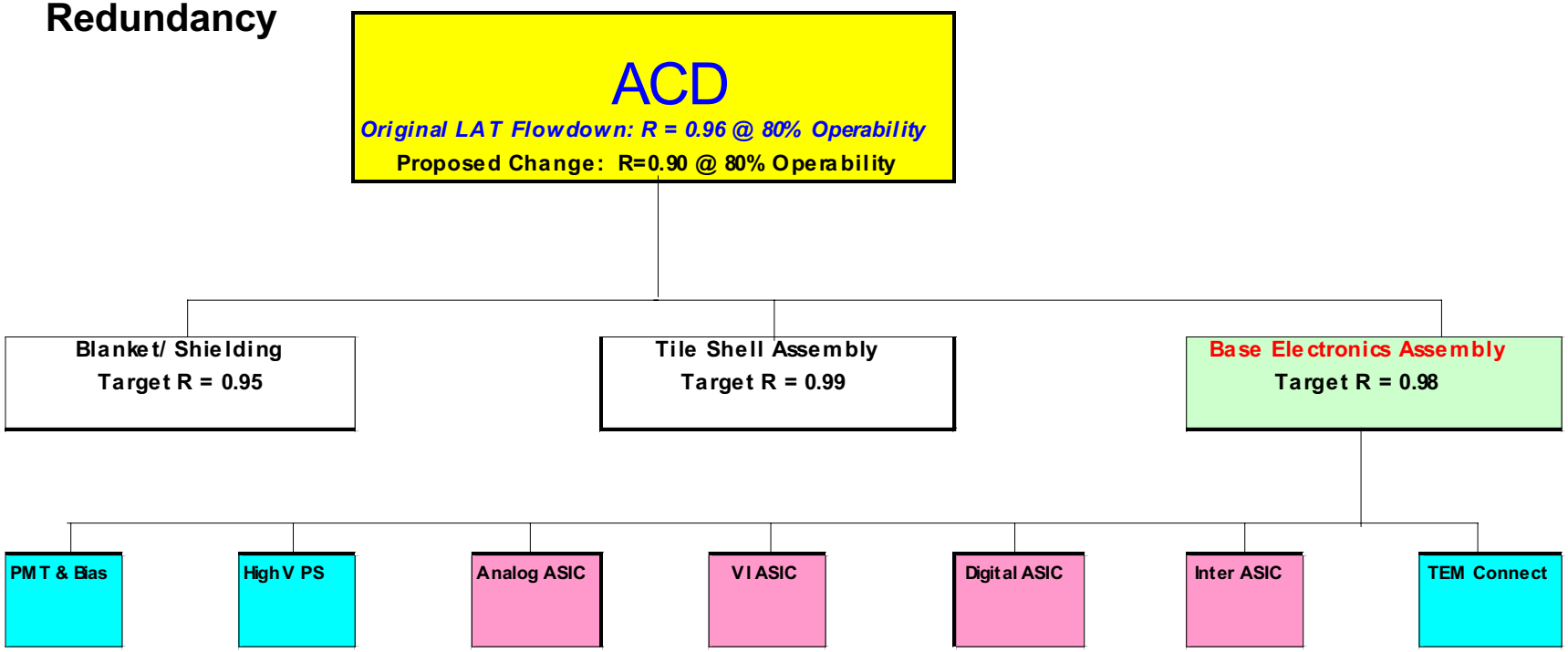
Redundancy

Reliability Allocation

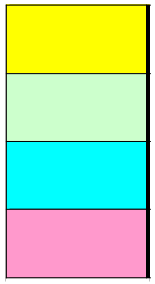


Reliability - is defined as the probability of successfully meeting mission objectives at end of life. P_f is probability of failure.

Redundancy



Legend:



Reliability/Operability Goal flowdown from SLAC

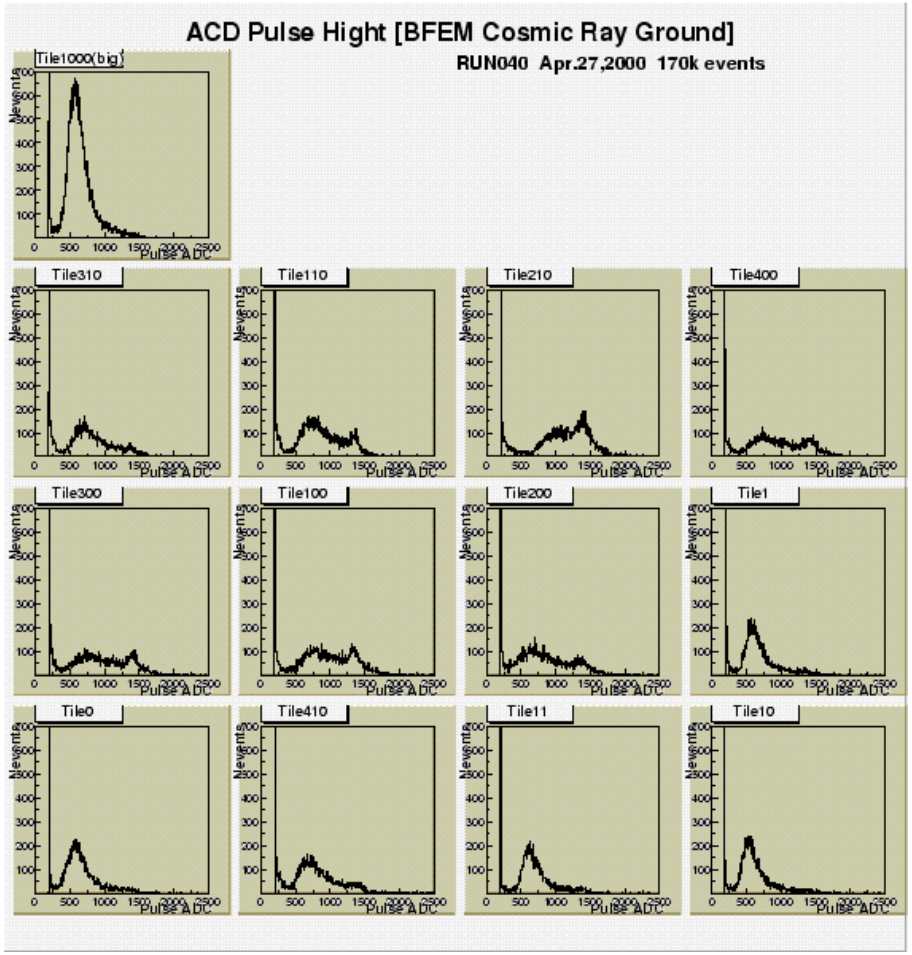
Target area for Comparative Numerical Assessments

Reliabilty Estimates based on Mil-217F and supplier data

Reliability allocated as needed to meet SLAC flowdown

Balloon Flight Engineering Model (BFEM)

It works. May it protect us from the dreaded *background*



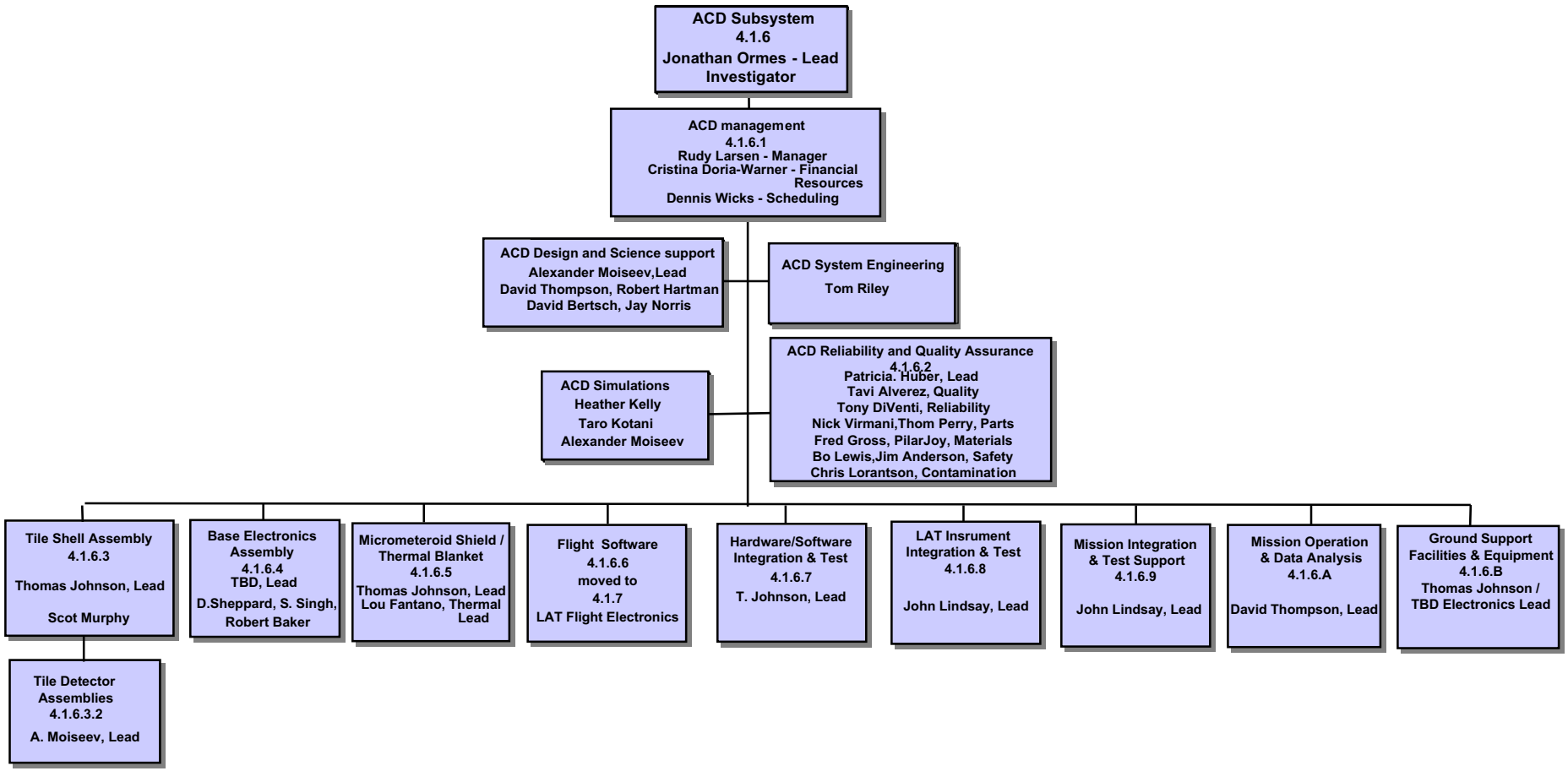
Studies planned before PDR

- **R&D Testing: Identify optimum design in terms of tile efficiency and light collection and map the response (light yield, efficiency) of a fiber/tile configuration in detail.**
  - **Determine testing methodology and construct test configuration -complete**
  - **Determine optimum fiber spacing in tile -complete**
  - **Determine optimum groove depth -complete**
  - **Determine tile thickness effects on light yield (linear with thickness?)**
  - **Determine edge effects -complete-no measureable effect**
  - **Determine tile uniformity**
  - **Determine effects of fiber end treatments (Al'ized ends)**
  - **Determine fiber length effects -complete, using low attenuation light transmission fibers**
  - **Determine MIP light yield, # of PE's, and PMT gain requirements -complete**
- **Production Testing: Develop and implement test procedure and fixture to verify performance of every tile.**
  - **Experience derived from R&D Testing will determine testing methodology and requirements**
- **Milestones:**
  - **Remaining R&D Testing Completed: September 1**
  - **Production Test Plan Completed: September 1**

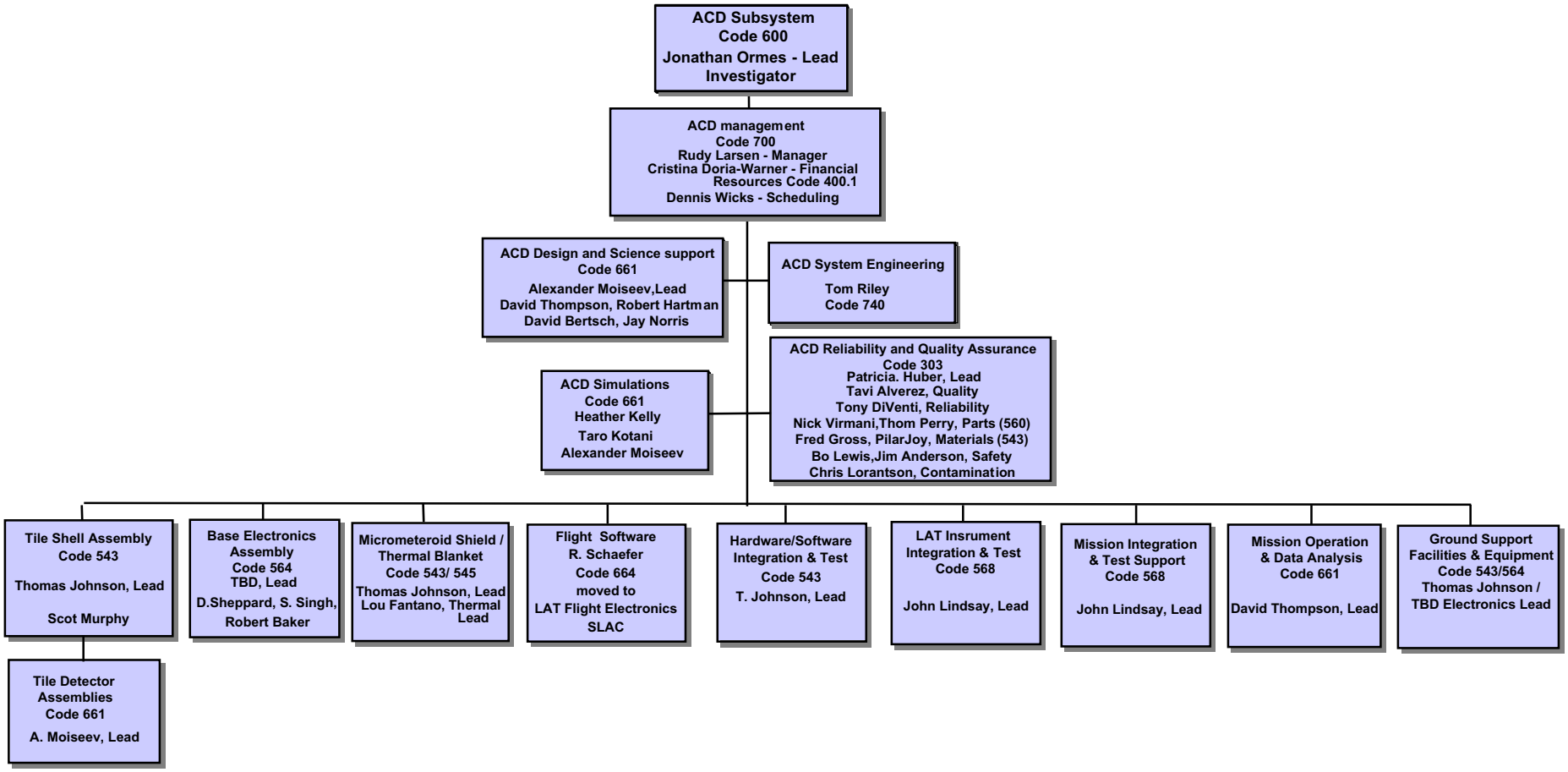
Issues and Concerns

- **Reliability requirement**
  - Blanket penetration can be reduced by making it thicker at the cost of additional background and mass.
  - Revised electrical design and interface leads to large number of interconnections. Connector reliability is under study.
  - Poor understanding of total system performance due to an ACD tile failure (especially for side entry).
- **Unvalidated system performance of background rejection**
  - Electron rejection power not yet adequately simulated. Needed to obtain effective area after electron cuts.
  - Is the coverage of the ACD adequate against albedo from the Earth, esp. low E proton, positron and electron albedo.
- **Level 4 requirements documentation is incomplete**
  - Electronics interfaces need further definition
  - Detector design optimization studies just completed

ACD Work Breakdown Structure



ACD Organization Chart (Backup)



Code
302 - Systems Reliability and Safety Office
303 - Assurance Management Office

Code
400.1 - STAAC Business Management Office

Code
543 - Mechanical Engineering Branch
545 - Thermal Engineering Branch
564 - Microelectronics and Signal Processing Branch
568 - Flight Systems Integration and Test Branch

Code
600 - Space Sciences Directorate
661 - Gamma Ray and Cosmic Ray Astronomy
663 - Instrument Development
664 - Data Management & Programming

Code
700.1 - Systems Technology, And Advanced Concepts Directorate
740 - Flight Instrument Division

ACD Resource Allocations

Title	Allocation	Estimate	Comment
Mass	205 Kg (without Electronics under the grid) 34 Kg (electronics under the grid) _____ Total 239 Kg.	228.4 (including electronics on the ACD) 16 Kg (cable on the ACD only) Total 244.5 Kg.	Resolve discrepancies for distribution of cabling and electronics
Power	37 Watts	<37 Watts	High Voltage Power Supply design will set exact consumption
Size		Meets internal Requirements	Details in Mechanical Section
		Meets External Requirements	

ACD Requirements Flowdown

Level III

5.2 Detection of Charged Particles
5.3 Detection Efficiency
5.4 Adjustable Threshold on Detecting Charged Particle
5.5 Instrument Coverage
5.6 Mean Thickness
5.7 False VETO due to Backsplash
5.8 False VETO due to Electrical Noise
5.9 High-Threshold Detection
5.10 Adjustable High-Threshold
5.11 VETO Signal & Trigger Primitives
5.12 ACD Performance Monitoring

5.13 Reliability - Electronics
5.14 Reliability - Tiles
5.15 Reliability – System

5.16 Commands

5.17 Power Consumption

5.18 Mass
5.19 Center of Gravity
5.20 Environmental
5.21 Physical Size

5.22.1 Thermal Blanket/ Micrometeoroid Shield
5.22.2 Micrometeoroid Protection

Areal Mass Density

Level IV - Electrical

Charged Particle Detection
Threshold on VETO Detection of Charged Particles
False VETO due to Electrical Noise
High-Threshold Detection
Adjustable High-Threshold
Level 1 Trigger Acknowledge
Performance Monitoring and Calibration
High Voltage Bias Supply Requirements
PMT Bias Chain Requirements
Radiation Tolerance
Electrical Reliability
Commands and Commanding interface
Output Data Formats
Power Consumption
Electronics Mass and Mass of cables
Environmental Requirements and Test plans

Number of Photoelectrons per tube per MIP
Adjustment of Threshold
PMT gain, charge output per MIP
Trigger Primitives

Derived - Mechanical

Mass budget
Inside Dimensions
Outside Dimensions
Fundamental Frequencies
Support for Tiles
Support for Fibers
Location of Grid
Thickness
Loads

PMT Size
Tile Sizes, & Segmentation & Location
Gap Restrictions & Locations
Mechanical Engineering Unit
Mechanical Reliability

Software Interface

ACD Level 3 Spec and Verification

Req't #	Title	Summary	Verif. Method
5.2	Detection of Charged Particles	The ACD shall detect energy deposits with energies of above an adjustable threshold nominally at 0.3 MIP (minimum ionizing particle) and produce VETO signals.	T
5.3	Adjustable Threshold on Detecting Charged Particle	The threshold for VETO detection of charged particles shall be adjustable from 0.1 to 0.6 MIP, with a step size of $\leq$0.05 MIP.	T
5.4	Detection Efficiency	detection efficiency for minimum ionizing particles shall be at least 0.9997 over the entire area of the ACD (except for the bottom tiles on each side, for which the efficiency shall be at least TBD).	T, A
5.5	Instrument Coverage	The ACD shall cover the top and sides of the LAT tracker down to the top of the CsI.	I
5.6	Mean Thickness	The ACD, support structure, and micrometeorite shield shall have a mean thickness less than 0.04 radiation lengths.	A
5.7	False VETO due to Backsplash	The ACD shall be segmented so that no more than 20% of otherwise-accepted gamma-ray events at 300 GeV shall be rejected by false VETOES due to calorimeter backsplash.	A
5.8	False VETO due to Electrical Noise	The false VETO signal rate due to noise shall result in a rejection of no more than 1% of triggered gamma rays.	A
5.9	High-Threshold Detection	The ACD shall detect highly-ionizing particles (carbon-nitrogen-oxygen or heavier nuclei, denoted High-Threshold) depositing energy greater than 25 times a MIP and shall provide a signal to the ACD TEM. The eighteen (18) High-Threshold fast signals generated on a single electronics board will be OR'ed to produce a single signal for transmission to the TEM(s).	A
5.10	Adjustable High-Threshold	The High-Threshold shall be adjustable from 20 to 30 MIP in steps of $\leq$1 MIP.	A
5.11.1	Fast VETO Signal	For each PMT, a fast VETO signal shall be generated when the its VETO threshold is exceeded.	D
5.11.2	Fast VETO Signal Latency	The fast VETO signal latency shall be $150 \leq t_{latent} \leq 600$ nsec from the time of particle passage. The time jitter in the VETO pulses shall be $\leq$200 ns relative to particle passage.	T
5.11.3	Logic VETO Signal	A map of the tiles that produce VETO signals shall be generated for each Level 1 Trigger Acknowledge.	D

T- Test A - Analysis I - Inspection D - Design

ACD Level 3 Spec and Verification (2)

Req't #	Title	Summary	Verif. Method
5.11.4	Logic VETO Signal Latency	The map of VETO signals shall be available less than 100nsec after receipt of a Level 1 Trigger Acknowledge.	T
5.11.5	Logic VETO Signal Timing	The logic VETO map shall represent the triggering of all ACD discriminators at the time of the particle passage ($\pm$300 ns TBD) causing the Level 1 Trigger Acknowledge.	T
5.11.6	Fast VETO Signal Width	The fast VETO output signal shall be longer than the time for baseline recovery to within 0.05 MIP of original baseline to prevent "change of threshold" for following VETOs.	T
5.11.7	Fast VETO Recovery Time for Large Signals	For a signal equivalent to 1000 MIP's, the fast VETO signal shall be no longer than 10 microseconds.	D
5.11.8	High-Threshold Signal Latency	A highly-ionizing particle hitting the top or upper side row of tiles of the ACD shall produce a High-Threshold fast signal that will be delivered to the hardware trigger logic with latency of no more than the latency defined for fast VETO in specification 5.11.2	A
5.11.9	ACD Trigger Primitives	. The VETO signals caused by the individual PMT's will be transmitted to the ACDTEM's, where they will be OR'ed together (for each tile or ribbon), and used by the the TEM's to generate trigger primitives.	T
5.12	ACD Performance Monitoring	The ACD electronics shall collect and transmit sufficient pulse height, and temperature information to monitor the status and performance of the ACD system and maintain its calibration to 5%. The ACD TEM's will generate and transmit count rates for ACD signals. A low-threshold signal will allow zero suppression of the pulse height data transmission to the data acquisition system. ACD voltages and currents will be monitored on the LAT side of the interface.	D
5.12.1	Low-Threshold Signal	The ACD shall detect energy deposits above an adjustable threshold nominally at 0.1 MIP and produce Low-Threshold signals.	D
5.12.2	Low-Threshold Adjustability	The Low-Threshold shall be adjustable from 0.05 to 0.3 MIP, with a step size of $\leq$0.05 MIP.	D

T- Test A - Analysis I - Inspection D - Design

ACD Level 3 Spec and Verification (3)

Req't #	Title	Summary	Verif. Method
5.12.3	Signal Content	When a Level 1 Trigger Acknowledge is received, the ACD electronics shall collect and transmit sufficient information to determine thepulse height up to 1000MIP with the following precision: for a pulse below 10 MIP, precision of <0.02 MIP or 5%, whichever is larger; for a pulse above 10 MIP, precision of <1 MIP or 2%, whichever is larger.	D
5.12.4	Pulse Digitization	Upon a Level 1 Trigger Acknowledge, all tile and ribbon pulses shall be digitized.	
5.12.5	Pulse Height Measurement Latency	The pulse height measurements shall be completed within (TBD) microseconds after a Level 1 trigger is received.	
5.13	Reliability - Electronics	No single failure in the ACD electronics shall result in the loss of signal from more than one detector element (tile or ribbon)..	A
5.14	Reliability - Tiles	The loss of any one detector element (tile or ribbon) shall not result in the loss of any other element.	A
5.15	Reliability - System	The probability of the loss of both VETO signals from any scintillator tile shall be less than 1%/year (TBR). The probability of the loss of both VETO signals from any scintillator ribbon shall be less than 5%/year (TBD).	A
5.16.1	Detector On/Off Commands	The ACD shall implement commands to allow each group of 18 PMT's to be separately powered on and off.	T
5.16.2	Detector Gain Commands	The ACD shall implement commands to allow the gain of each group of 18 PMT's to be separately adjusted.	T
5.16.3	Electronics On/Off Commands	The ACD shall implement commands to allow each redundant set of electronics to be separately powered on and off.	T, D
5.16.4	VETO Threshold Commands	The ACD shall implement commands to set the VETO threshold for each PMT.	T, D
5.16.5	High-Threshold Commands	The ACD shall implement commands to set the High-Threshold for each PMT.	T, D
5.16.6	ACD Monitoring Commands	The ACD shall implement commands to allow the Instrument Operator to adjust the monitoring functions of the ACD electronics, including the Low-Threshold for each PMT.	T, A
5.16.7	Low-Gain Mode Commands	The ACD shall implement commands to switch the ACD PMT's into and out of low-gain mode for high counting rate conditions.	T

T- Test A - Analysis I - Inspection D - Design

ACD Level 3 Spec and Verification (4)

Req't #	Title	Summary	Verif. Method
5.17	Power Consumption	The ACD total electronics power consumption shall not exceed 37 W.	D, A
5.18	Mass	The total mass of the ACD and micrometeoroid shield shall not exceed 205 kg.	D
5.19	Center of Gravity	The center of gravity of the ACD and micrometeoroid shield shall be located within 400 mm of the top of the mechanical grid structure.	T
5.20	Environmental	The ACD shall meet the structural and thermal environment requirements defined in its ICD.	T, D, A
5.21	Physical Size	The dimensions of the ACD plus the micrometeoroid shield shall conform to the requirements in its ICD.	D
5.22.1	Thermal Blanket/ Micrometeoroid Shield Areal Mass Density	The thermal blanket/micrometeoroid shield shall have mass per unit area <0.32 g/cm^2 in order to minimize secondary gamma-ray production by undetected cosmic ray interactions.	D, A
5.22.2	Micrometeoroid Protection	The thermal blanket/micrometeoroid shield shall minimize the probability that micrometeoroids and space debris will penetrate and create a light path to the ACD scintillators. The mean rate of such penetrations over the entire shield shall be less than 0.01/Year	A
5.22.3	Thermal Control	The thermal blanket/micrometeoroid shield shall have thermal properties (absorptance, reflectance, and transmittance) as required to maintain the temperatures described in its ICD.	A
5.23	Performance Life	The ACD shall maintain the specified performance for a minimum of five years in orbit.	A
5.24	Operation in High Rate Conditions	The ACD photomultiplier bias supplies shall switch into a low-gain mode to protect the phototubes in very high intensity particle conditions (> 10 kHz in an individual tile) such as the South Atlantic Anomaly. The ACD requires a source(s) of the SAA entry and exit signals from elsewhere, either the LAT DAQ or the Spacecraft.	A
5.24.1	Notification of Mode Change	The ACD shall identify times when it switches into low-gain mode for high counting rate conditions.	D, T
5.24.2	Tile Linear Response	The scintillator tiles in the ACD shall have linear (non-saturated) response for MIP rates up to 3 kHz.	D, T

T- Test A - Analysis I - Inspection D - Design

ACD Flight Interfaces

- Electronic
  - Data & Commands
  - Power
  - Spacecraft Housekeeping
- Mechanical
  - Mount
  - Internal Clearance
  - External Clearance
- Thermal / Environmental
  - Shield / Thermal Blanket

Grounding and Cable Harness

- Primary Ground in Spacecraft Power System
- ACD connection through LAT Power Conditioner
  - All ACD cards are independent
  - 100 ohm isolation resistors between board grounds
- Internal ACD Cable Harness
  - 2 cables per ACD Electronics Card: 24 total
  - Very simple, redundant design
  - Separate Spacecraft analog Housekeeping Cable
  - Primary and Secondary systems segregated
- External ACD Cable Harness
  - 24 cables to ACD-TEM's
  - Power Cable

ACD Documentation Status (1)

	GLAST Peer Review/PDR Documentation Status Report					
	Internal Doc # LAT	Title	Responsible Person	% Complete	% Complete Last Report	ECD
01	ACD-PDR-11002	LAT ACD Subsystem Preliminary Design Presentation	Laren			
02	LAT-SS-00016-D7	LAT ACD Subsystem Specification - Level III	J. Ormes	Draft		
03	ACD-SPEC-3001	Subsystem Specification - Level IV	T. Riley	Preliminary		
04	ACD-ICD-9001	Subsystem Specifications and Interface Requirements - Level IV	T. Riley	60%		
05	ACD-ICD-9002	Interface Requirements	T. Riley	Preliminary		
06	ACD-PDR-11001	GLAST ACD Mechanical Design, PDR Design Review Document	T. Johnson			
07		Conceptual Design of the LAT ACD Electronics Readout System	D. Sheppard			
08	ACD-SPEC-3002	ACD Front-End Readout ASIC Specification	Singh			
09	ACD-SPEC-3003	ACD Grounding and Shielding Plan	T. Riley			
10	ACD-ICD-9003	ACD Electrical Interface Specification	Hoiler/Sheppard			
11	ACD-ICD-9004	LAT ACD Interface Control Specification				
12		LAT ACD Reliability Analysis - SAMPLE	T. Diventi			
13		ACD Failure Mode Effect Analysis Table	D. Sheppard			
14	ACD-TEST-1001	LAT ACD Test Plan	J. Lidsey			
15	ACD-MPML-10001	LAT ACD Mechanical Parts and Materials List	T. Johnson			
16	ACD-EPML-10002	LAT ACD Electronics Parts List	D. Sheppard			
17		ACD Dimensions and Masses	Johnson/Riley			
18	GEVS-SE Rev A	General Environmental Verification Specification for STS & ELV Payloads, Subsystems, and Components	A. Moiseev			
19	ACD-TEST-1002	Beam Test of Gamma-ray Large Area Space Telescope Components	A. Moiseev			
20		Single-Event Latchup Characteristics of Three Commercial CMOS Processes	Singh			
21	LAT-SS-00010	LAT Instrument Performance Specification	Thurston/Davis			
22		GLAST Large Area Telescope, Flight Investigation: An Astro-Partical Physics Partnership Exploring the High-Energy Universe	LAT Project			
23	GSFC 433-SRD-0001	GLAST Science Requirements Document	GLAST Project			Complete

ACD Documentation Status (2)

24	LAT-GE-00009	LAT Science Requirements Document - Level II Specification	Ritz/Thurston			
25	GSFC 433-IRD-0001	GLAST Science Instrument - Spacecraft Interface Requirements Document	GLAST Project			Complete
26	LAT-SS-00047	LAT Mechanical Performance Specification	M. Norby, SLAC			
27	GSFC 433-MAR-0001	Mission Assurance Requirements (MAR) for Gamma-Ray Large Area Telescope(GLAST) Large Area Telescope(LAT)	GLAST Project			Complete
28	GSFC 433-RQMT-0005	GLAST EMI Requirements Document	GLAST Project	Draft		
29	LAT-MD-00099	LAT EEE Parts Program Control Plan	N. Virmani			
30	LAT-CR-00082	QA Provisions for the GLAST LAT SSD	Virmani/Sadruzinski/Ohsugi	Draft		
31	LAT-MD-00033	LAT Work Breakdown Structure	T. Boyson/LAT Project	Draft		
32	ACD-REQ-7001	Anti-Coincidence Detector Requirements and Implications for the GLAST Trigger and Rates	J. Ormes			
33		Readout for the Anticoincidence Detector				
34		ACD Segmentation Trade Study	Moiseev/Ormes			
35	ACD-CM-6001	ACD Configuration Management Plan	J. Anders	10%		

ACD Subsystem Deliverables

ACD Deliverables to LAT

DAQ I/F Test Unit	28 February, 2003
Engineering Model	3 February, 2004
Calibration Unit	3 February, 2004
Flight Unit	26 April, 2004

LAT Deliverables to ACD

TEM Boards

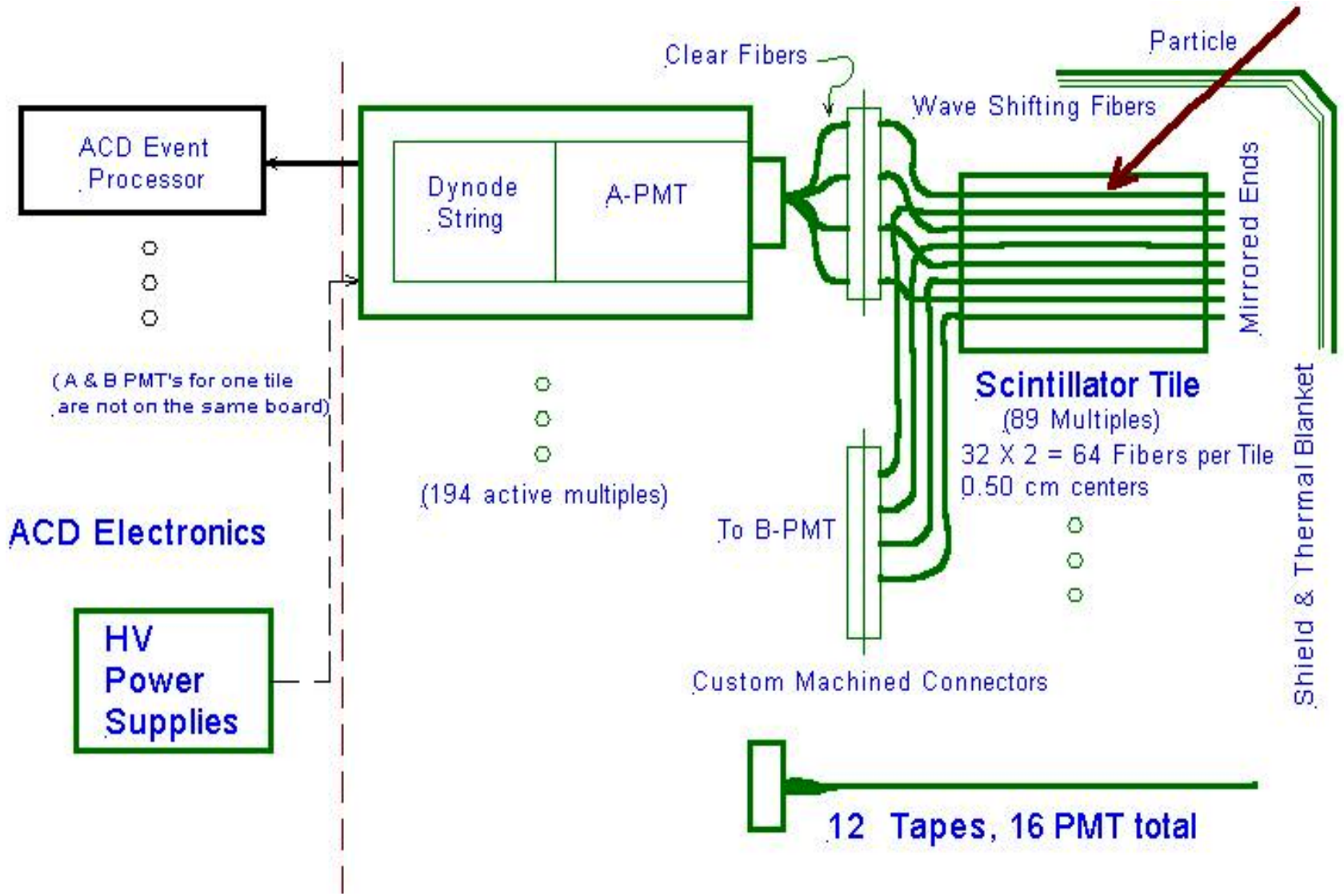
ACD Subsystem Design

ACD Detector Design - Alexander Moiseev

ACD Mechanical Design - Thomas Johnson

ACD Electronics Design - David Sheppard

Block Diagram: Tiles



Detector Design

Task: design the system to meet the SRD and ACD Level III requirements. Provide the scientific proof and support to the design

Outline

I. Requirements and outline

- Efficiency and Light Yield
- Backsplash and self-veto
- Tile design approach

II. Trade Studies and Implementation

- Segmentation
- Hermeticity
- Tile design
- Efficiency
- PMT choice
- Prototyping
- Issues and Summary

Detector Design
Required Efficiency

ACD Level III,
5.4. Efficiency

I. Requirements and approaches

The ACD uses plastic scintillating detectors. They are the most reliable, inexpensive, well understood detector of charged particles, perfectly suited to the ACD task.

- The ACD efficiency requirement is 0.9997 over the whole area.
- This is equivalent to missing 3 events of 10,000. Two major factors can contribute to inefficiency
  - event crossing the detector can go undetected due to a fluctuation of the signal (Landau, Poisson, path length)
  - imperfect hermeticity of the system (cracks between detectors or leakage around ACD)

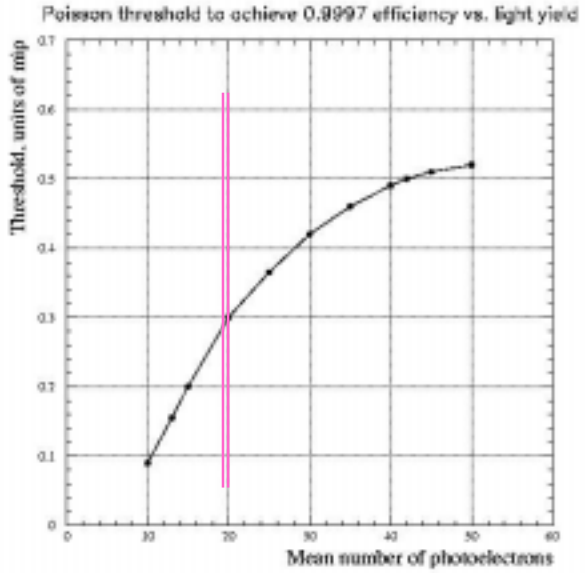
Detector Design
Required Light Yield

- The light, created by the charged particle crossing the plastic scintillator, is effected by Landau and path-length fluctuations

- The major, Poisson fluctuations occur at the step of conversion photons into photoelectrons (p.e.) in the photomultiplier tube (PMT) phocathode.

- The particle can go undetected if this signal falls below the threshold, set in the electronics discriminator.

- The number of photoelectrons $N_{p.e.}$ is the key parameter which determines the efficiency.



This figure demonstrates that ~ **20 p.e.** are needed to set a threshold to 30% of the *mip*

Detector Design
Self-veto

ACD Level III
5.7 False veto

- EGRET experienced 50% degradation in sensitive area at 10 GeV, compared to 1 GeV, due to false veto caused bybacksplash
- Backsplash is a small fraction of the cascade developed in the calorimeter by the primary high energy particle and emitted backward. It mainly consists of 100 KeV - few MeV photons that have attenuation lengths that allow them to escape from the CsI calorimeter
- Some of these photons undergo Compton scattering in the ACD and create false veto signals. These signals can veto good events otherwise being accepted.

The approach - SEGMENTATION - is to subdivide ACD into small segments (tiles) to minimize the efficiency degradation at high energy.

Detector Design
Tile design

Segmenting the ACD creates a problem: How to get the light out from the tiles?

LAT-SS-00016
5.4 Efficiency
5.6 Mean thickness
5.14, 5.15 Reliability

Requirements:

- minimize the amount of the inert material outside of ACD in the Field-of-View
- the total thickness of ACD should be less that 0.04 X_0
- no significant gaps (dead areas) between the tiles
- redundancy in readout
- loss of one tile shall not result in the loss of any other element
- 5 year lifetime

Detector Design
Tile design - approach

Tile Design:

- 1cm thick plastic scintillator (BC-408) tiles with wave-shifting fiber (WSF BCF-91A/MC) and PMT (Hamamatsu R4443, baseline) readout
- Fibers are embedded in grooves cut on the internal surface of the tile Two PMTs to read out each tile
- Each tile with fiber bundles has a separate light-tight housing
- Fiber spacing in the tile is of the order of 1 cm

Detector Design
Tile design - approach

This design provides:

- **minimum inert material (no heavy light guides etc.)**
- **minimum gaps between tiles**
- **uniform light collection**
- **resistance impacr ofaccidental puncture by micrometeoroids (with separate light-tight housing only one tile will fail if punctured)**
- **redundancy of PMTs**
- **robust design: low impact of individual fiber failure/damage**

Detector Design: Trade studies and implementation

Backsplash

The backsplash effect was measured in GLAST beam test in 1997 at SLAC and in 1999 at CERN. The collected data were combined and fitted by the expression:

$$P_{backsplash} = \overline{0.85 \leftrightarrow \frac{0.3}{E_{thr}} + 0.15 \sqrt{\leftarrow 10^{-3} \leftrightarrow \frac{A}{144} \leftrightarrow \frac{\overline{\quad 55}}{x+10}}^{2} \leftarrow E^{0.75}}$$

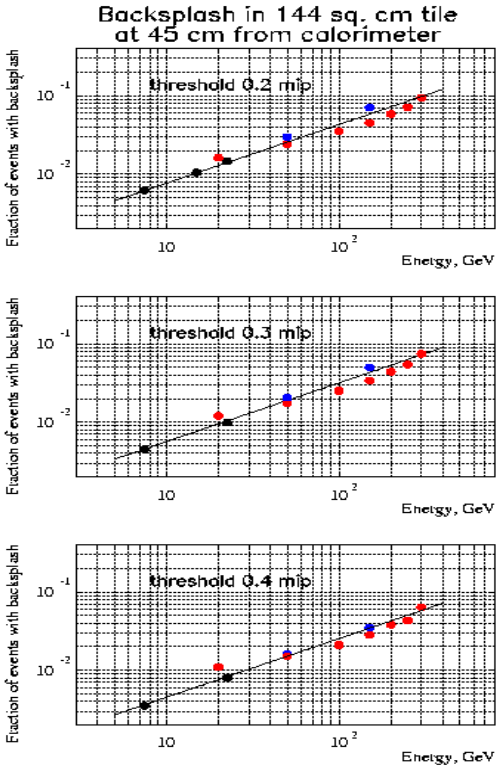
Where E is the energy of incident electron/photon in GeV

E_{thr} is the threshold value in units of *mip*

X is the distance from the top of calorimeter

A is area in cm^2

$P_{backsplash}$ is the probability that there was an energy deposition above E_{thr} in 1cm scintillator

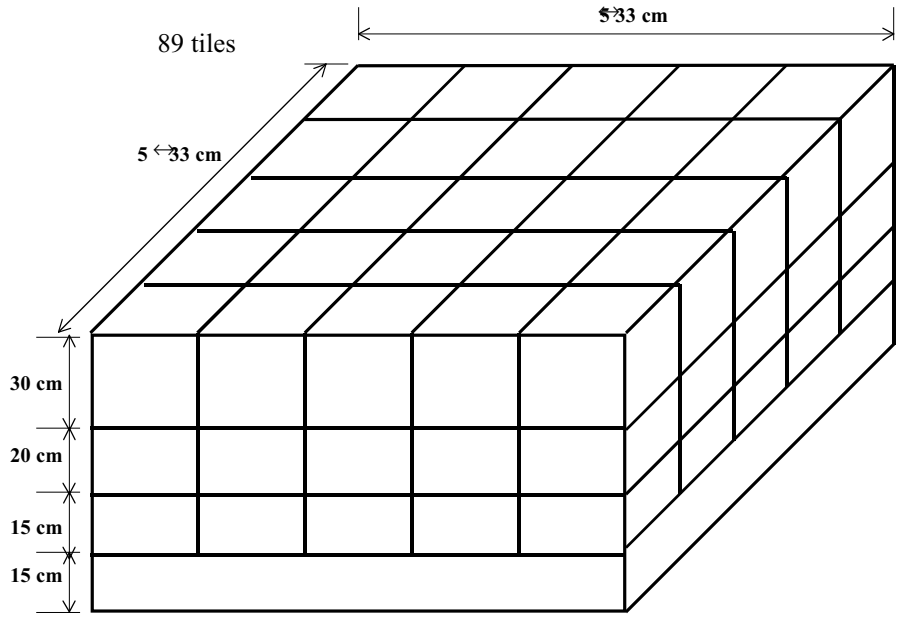


- **- 1997 SLAC**
- **- 1999 CERN/ICA**
- **- 1999 CERN/TTU**

Detector Design
Segmentation

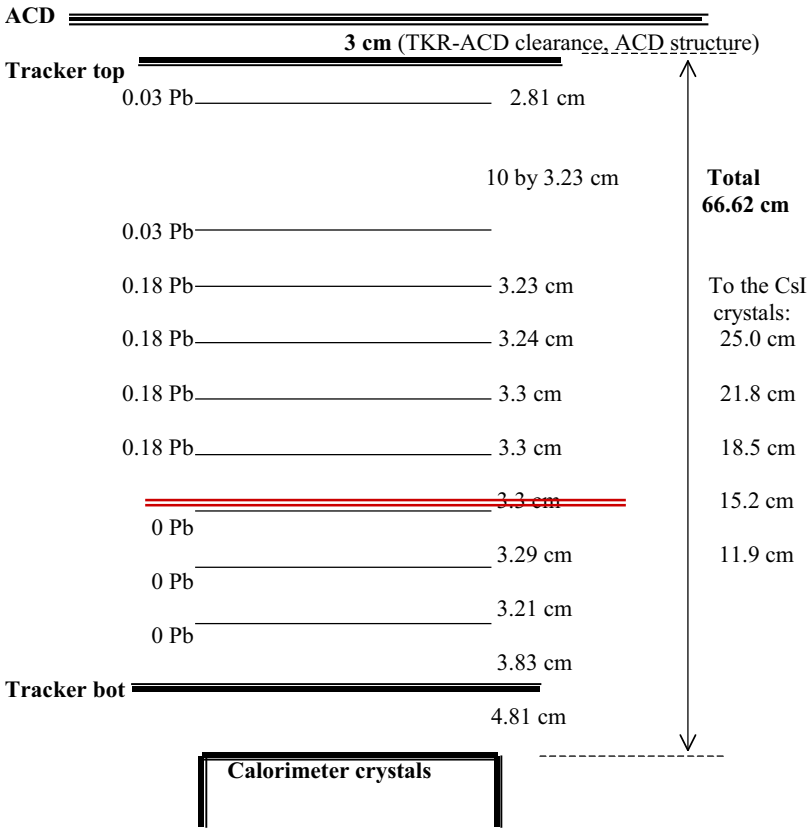
•Our simulations show lower backsplash than that predicted by the experimental formula. To be sure that we are not underestimating the effect we put fitted experimental formula into GEANT simulations

• ACD segmentation was optimized by evalulating the effective area and geometric factor degradation for high energy (300 GeV) photons.



Detector Design
Side Segmentation

- Taking into account a fact that the first tracker tray with the radiator is situated at >18cm from the calorimeter, we considered those events which enter the ACD side at least 15 cm from the ACD bottom (calorimeter top)
- With this approach we were able to reduce the number of tiles from 145 to 89, with only a few percent loss in effective area



Detector Design
Segmentation

Conclusion

As a result of the trade study the optimal side segmentation was chosen:

- **Final segmentation of active area: 3 rows of 5 tiles each**
- **Use of events entering through lower 15 cm of the ACD is questionable because there is no tracker layers with converters. There is only 1 or 2 tracker layers w/o converters to be crossed for the events which may produce high energy calorimeter trigger, but they are at large angles. The use of such events has not been simulated. Thus the bottom row is unsegmented.**
- **The reduced segmentation design for the ACD is proposed with 5 by 5 tiles on the top and 16 tiles in each side (89 tiles in total)**

Detector Design
Hermeticity

- **Cosmic ray particle leakage through the gaps in the tile layout represents a serious problem. It can severely effect the ACD efficiency.**
- **Butt tile joints should assume the gaps of order of 2mm (at room temperature) for the thermal expansion, and tile wrapping material.**

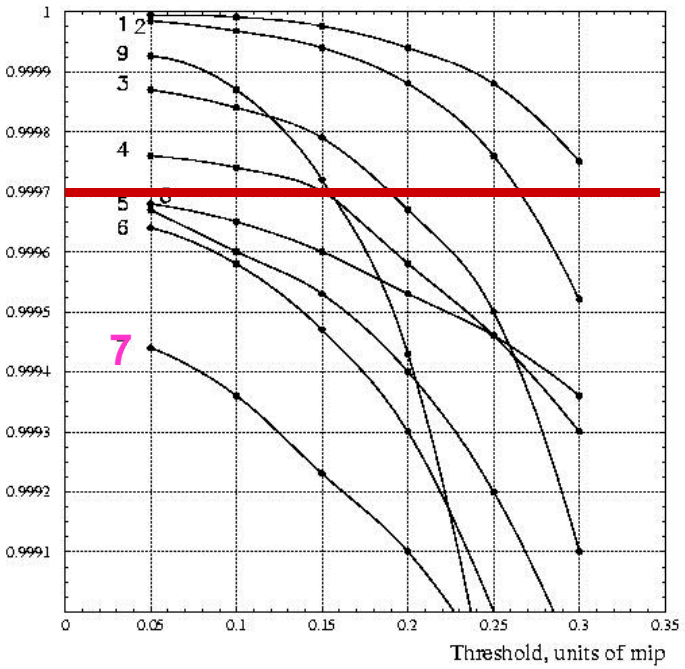
To quantify the effects, the detailed performance of the ACD assuming different gaps between the tiles, and given light yield was simulated.

Detector Design
Hermeticity: Simulations

Approach to the simulations:

- the whole ACD area is illuminated by isotropic flux of 1 GeV muons, uniformly distributed over the area, which perfectly imitate mips.
- Energy loss for each event, including Landau fluctuations, is determined by the path in the scintillator
- Assuming given number of photoelectrons for normal particle incidence, the number of p.e. is calculated proportionally for every event
- Gaussian fluctuation is applied to that number of p.e., providing the actual number of p.e. for each event. Gauss here is a conservative estimate for the Poisson
- Efficiency of detection is simulated as a number of events with the number of p.e. exceeding corresponding threshold (scaled to the single mip mean number of p.e.) divided by the total number of trials.

Detector Design
Hermeticity: Gap Simulations



Gaps are problematic!

Line 1 - no gaps, $N_{p.e.}$ = 20

Line 2 - no gaps, $N_{p.e.}$ = 17

Line 3 - 0.5 mm gaps, $N_{p.e.}$ = 17

Line 4 - 1mm gaps in one direction, and no gaps (overlap) in the other, $N_{p.e.}$ = 20

Line 5 - 1mm gaps, $N_{p.e.}$ = 20

Line 6 - 1mm gaps, $N_{p.e.}$ = 17

Line 7 - 2mm gaps in one direction, no gaps - in other, $N_{p.e.}$ = 20

Line 8 - 1mm gaps, no statistical fluctuation

Line 9 - normal incidence at one point, $N_{p.e.}$ = 17

Detector Design
Hermeticity: Effect of gaps

Simulations show that necessary gaps immediately bring us below the required efficiency

Solution: these gaps can be covered by **flexible ribbons**, made of scintillating fibers, to provide detection of particles which leak through the gaps

Design trade study - 3 designs have been considered:

- Option 1 - butt joints* in both directions, covered by the ribbons
- Option 2 - tiles overlap in one direction, and butt joints in the other with ribbons to seal these gaps
- Option 3 -tiles overlap in both directions

* Butt joints assume 2mm gaps for the wrapping and thermal expansion

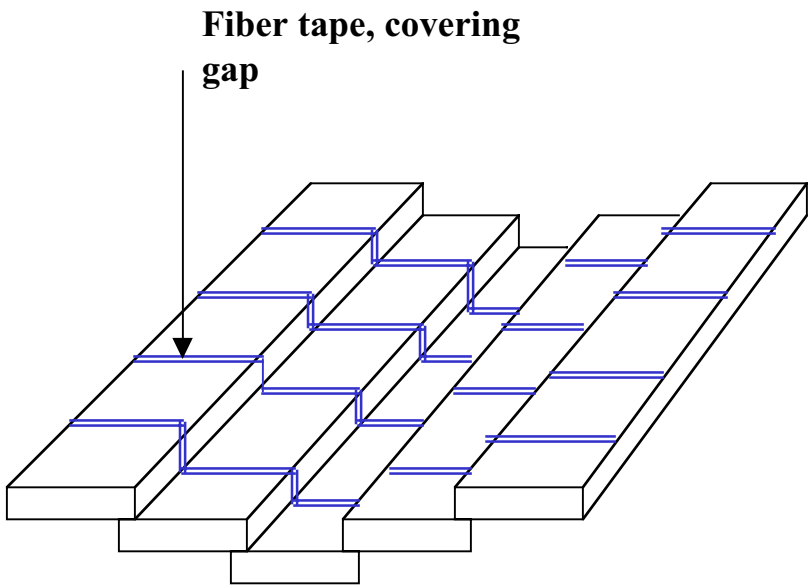
Detector Design

Hermeticity: Overlap and ribbons

Option 2 was chosen as a compromise between the mechanical complexity and required performance

Simulated Design.

- **all tiles are overlapped by 1cm in one direction, and have variable gaps in the other. The gaps are required to be ~ 3 mm (0.7mm for wrapping and 2mm for contraction from room temperature to -10C^{o}). These gaps are covered by 2mm thick scintillating fiber ribbons.**
- **the light yield from normal incidence *mip* was assumed to be 5.5 p.e., and the threshold for the detection was set to 2 p.e. Both these numbers are conservative.**



Detector Design
Hermeticity

1 - 20 p.e. in average from mip in the tile, 2 mm gaps between tiles, 8 mm wide fiber ribbons

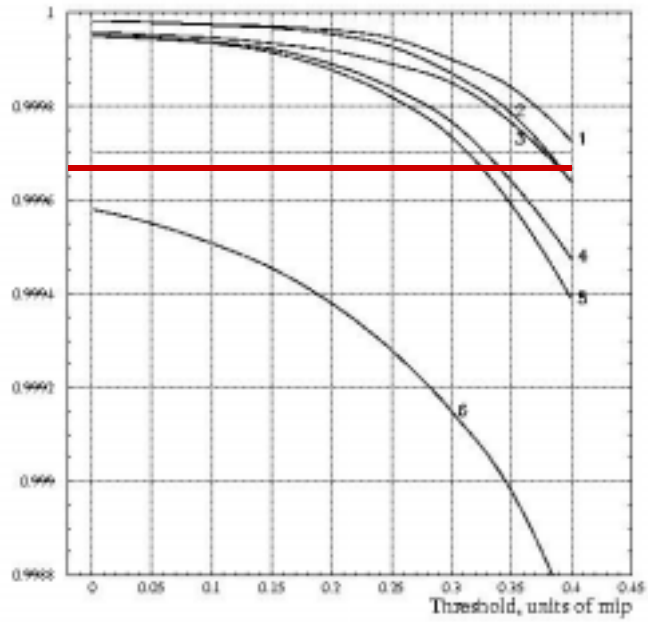
2 - 18 p.e., 2 mm gaps, 8 mm wide ribbons

3 - 20 p.e., 3 mm gaps, 8 mm wide ribbons

4 - 20 p.e., 3 mm gaps, 6 mm ribbons

5 - 18 p.e., 3 mm gaps, 6mm ribbons

6 - 20 p.e., 2 mm gaps, NO ribbons

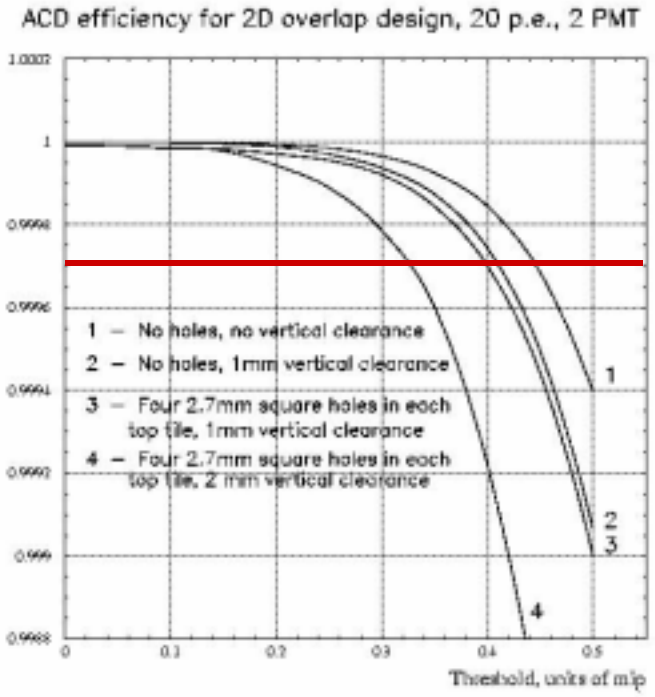


Conclusion: 8-10 mm wide fiber ribbons provide sufficient sealing of the gaps

Detector Design
Hermeticity: Holes

Effect of the holes in the tiles and vertical clearances between tiles

The holes are to attach the tile to the structure, and vertical clearance combines mechanical tolerance and wrapping.



Conclusion:

- **the holes do not effect much the hermeticity**
- **vertical clearance should be kept minimal, desirably under 1 mm**

Detector Design
Tile Design

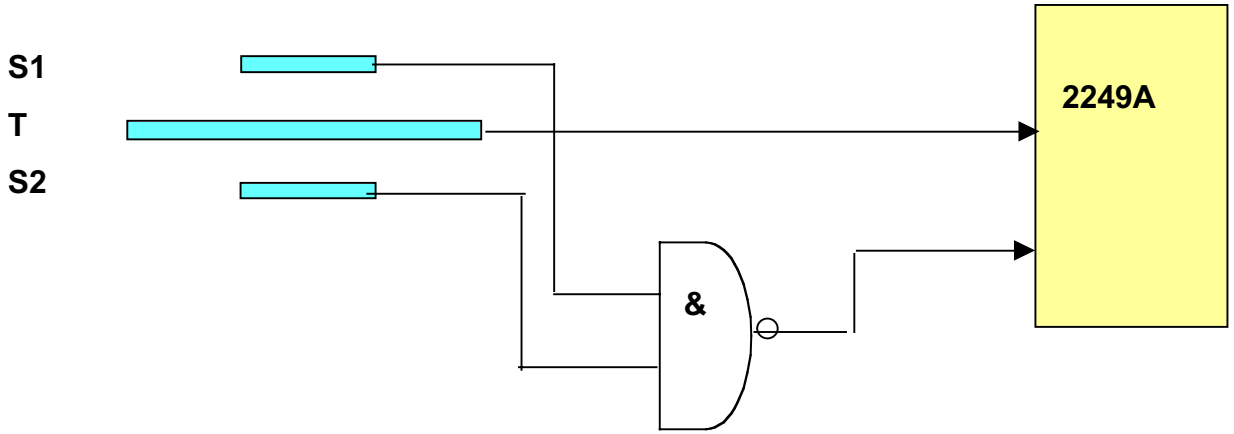
The tile design was carefully studied for the maximization of the light collection.

The parameters studied are the following:

- **fiber spacing effect**
- **effect of wrapping material - light reflection**
- **aluminization of the fiber ends**
- **fiber cladding**
- **scintillator manufacturer**
- **other different designs**

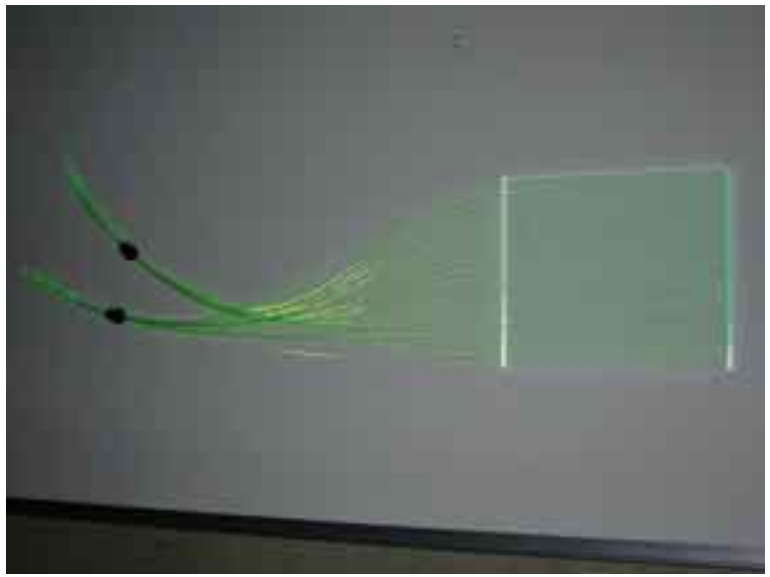
Detector Design
Tile Design

- To study the performance dependence on the tile design, a number of 10 cm by 10 cm tiles with the grooves were fabricated
- all runs were performed with the cosmic muons, and the same physical PMT was used
- tested sample T was placed between triggering scintillators S1 and S2; the pulse-height from T was analyzed by CAMAC 2246A gated by the coincidence from S1 and S2



Detector Design
Tile Design

Chosen tile design with maximum light yield, 40-50% higher than used before



- 1 cm thick plastic scintillator (BC-408 or ElJen 200)
- 5 mm spaced, 1.6 mm deep straight grooves
- 1mm diameter BCF-91A/MC wave-shifting multiclad fibers glued into grooves by BC-600 optical cement
- High light reflecting TETRATEC wrapping
- Aluminized fiber ends
- Clear 1.2mm diameter fibers BCF-98, connected to WSF near the tile, to bring the light to the PMT with minimal light loss

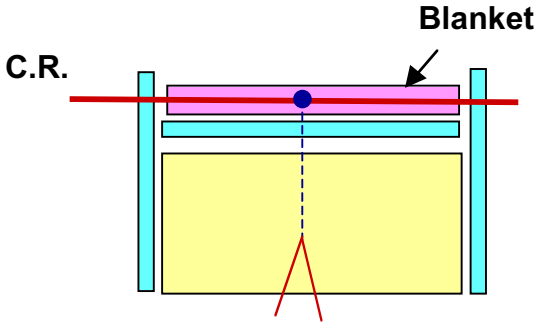
Detector Design
Tile Design

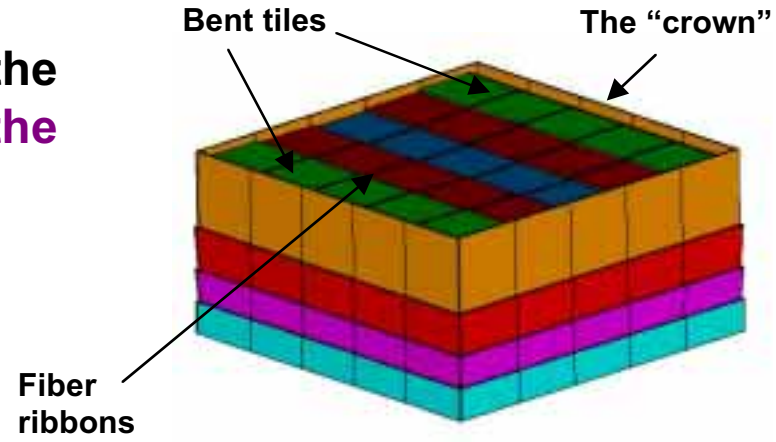
ACD Level III
5.5 Crown

The "Crown"

To protect the instrument against the background gammas, which can be produced by cosmic rays in the micrometeoroid and thermal blankets, the top row tiles are elevated above the top ACD surface, making up a "crown"

To provide for fiber routing over the ACD edges, the outer row tiles on the top are bent





Detector Design
Tile Design

Bent tiles

The bend radius is 4-5 cm

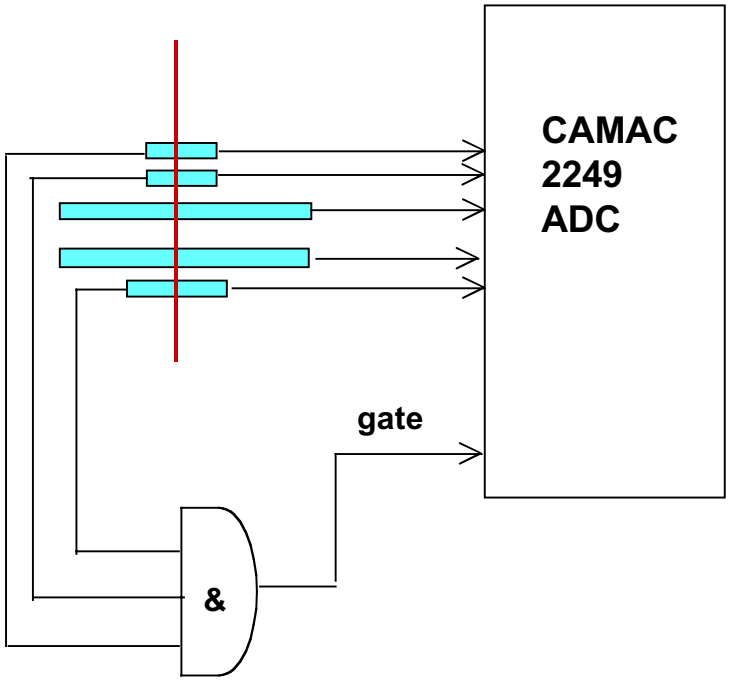
The problem is the gluing fibers in the grooves on the inside surface of the tile - they do not stay on the groove bottom, the glue spills out from the groove etc.

The solution is to make key-hole shaped grooves and to feed the fibers through from the edge - tested and found to work well

Detector Design
Tile Design

Efficiency

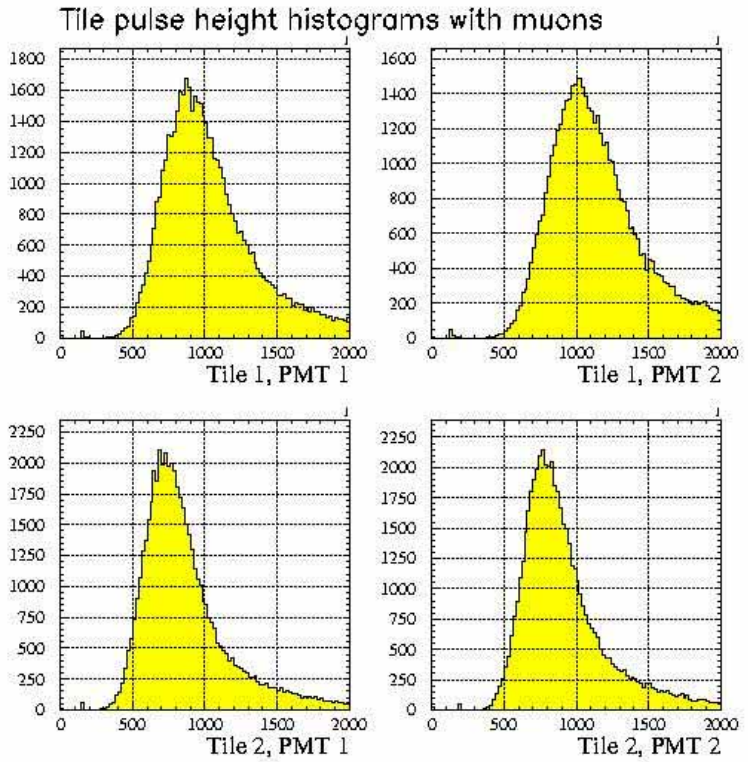
- Two flight tile prototypes were made to test their performance
- The design of these tiles was that found to be the best in our tile design trade study. Each tile has 2 fiber bundles, read out by separate PMT Hamamatsu R647 (non ruggedized version of flight baseline PMT)
- The efficiency for muons was measured



Detector Design
Tile Design

Efficiency

- Obtained pulse height histograms from all four PMTs are shown
- Characteristic shape of Landau distribution for muon energy loss is seen



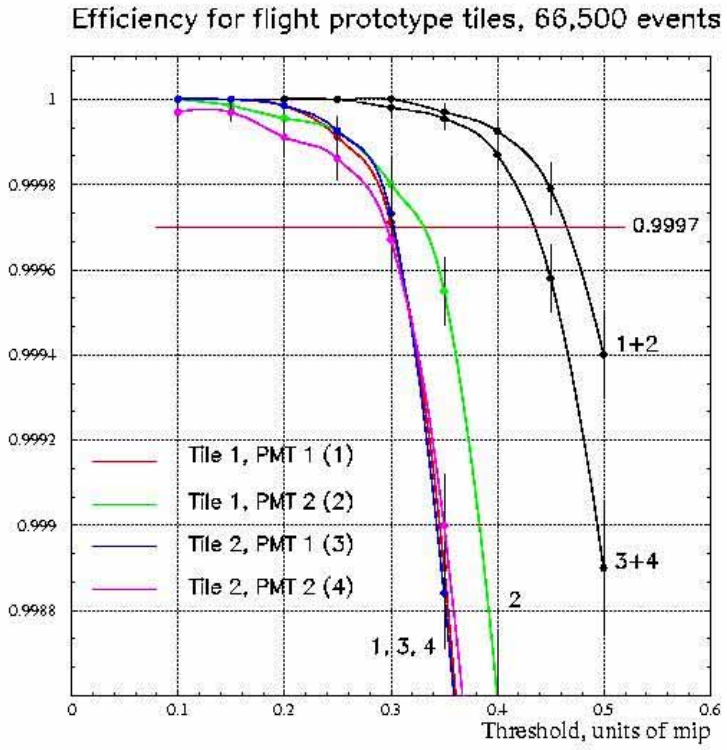
Detector Design
Tile Design

Efficiency

The efficiency measured in this experiment is shown in a figure for:

- single PMT (lines 1, 2, 3, and 4)

- both PMTs from one tile can be logically "ORed" as shown by lines "1+2" and "3+4"



Conclusion. Required efficiency of 0.9997 is achieved for thresholds $\leq$ 0.3 mip

Detector Design
Efficiency - Backsplash trade-off

Designing to minimize backsplash and maximize efficiency are competing requirements

- **backsplash reduction implies high threshold**
- **high efficiency implies a low threshold**

This leads to the requirement to carefully set the threshold in flight for high efficiency. This can be done by measuring the pulse height in the ACD tiles (PHA for every event is needed) and optimizing the threshold for backsplash in data analysis off-line. The thresholds can be set differently for different scientific goals.

- **Precise threshold setting requires the light collection uniformity of < 10% over the tile area (see efficiency curve)**

Detector Design
Tile Design

Conclusions

- the tile design is chosen with maximized light yield
- the flight tile prototype demonstrated the efficiency of > 0.9997 which meets the requirements
- in a case of performance degradation or the necessity to raise the threshold, both PMT in the tile can be ON and used in logical "OR". An increase in threshold could be needed to reduce the self-veto effect

Detector Design
PMT

Requirements:

- Head-on type PMT
- Bi-alkali photocathode (we need a sensitivity to 490 nm)
- Diameter less than 15.2 mm
- Length less than 80 mm (leads are not included)
- Flying lead connections
- Minimum gain at max HV shall be 2×10^6
- Cathode sensitivity greater than 90 μA/lumen at the maximum
- Projected gain degradation shall be less than 30% (1σ) after 50,000 hours of operation at a mean anode current of 30 ηA
- Ruggedized design, flight heritage is desirable
- 260 units are needed

Detector Design
PMT

PMT trade study

We found that possible choice of PMT to meet our requirements is limited to 3 candidates, all made by Hamamatsu

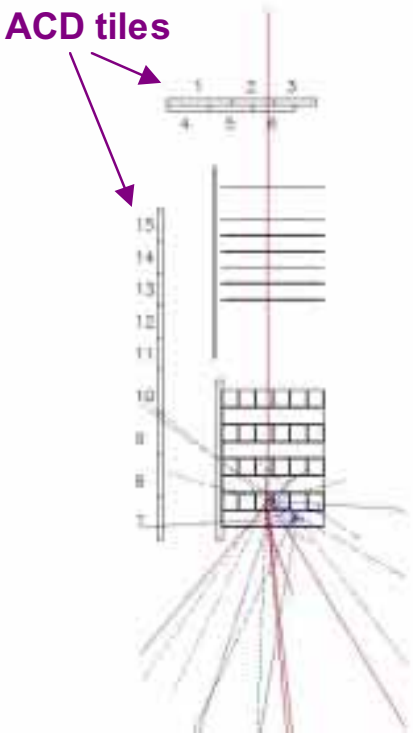
PMT type	Flight heritage	Ruggedness	Gain Degradation after 5 years	Cost	
R1635 10mm	STX	Exists in ruggedized version	25%	Medium-high (~ $1,500)	
R5611 19mm	No	Good	50%	Low	Rejected
R4443 15 mm	HEXTE, SOHO	Good	20%	Low-medium (~ $1,000)	

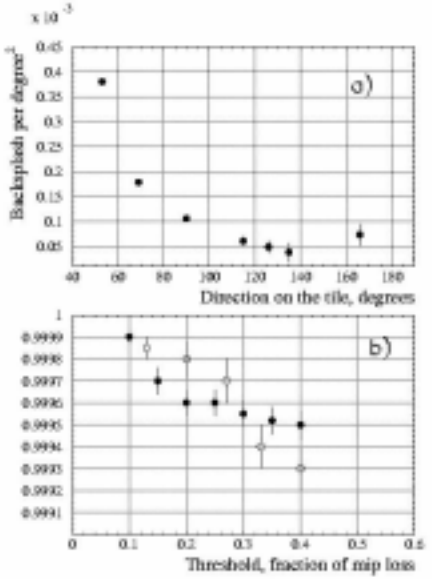
R4443 is chosen as a baseline

Detector Design
Prototyping

More than 45 different tile prototypes with WSF readout have been fabricated by us since 1997:

1. ACD prototype for 1997 beam test at SLAC (15 tiles with R647). This prototype was also tested at CERN in 1999. No one failure has been encountered. Obtained results were published in W.Atwood et al., NIM 2000, and were used in the backsplash analysis

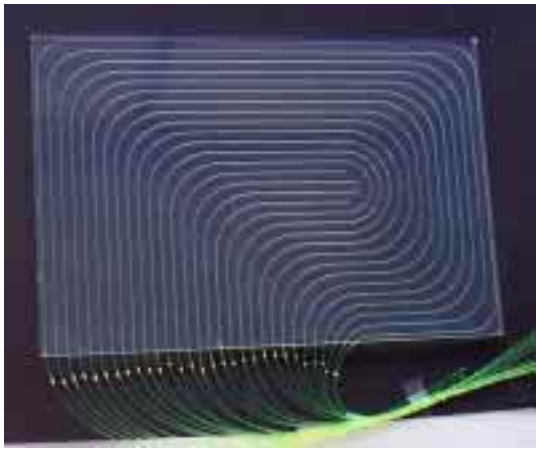




Results of SLAC'97 beam test

Detector Design
Prototyping

2. ACD prototype for BTEM and BFEM (13 tiles, including 4 bent, with R1635). This prototype was tested at SLAC in 1999-2000, and currently is at the final step of preparation for the balloon flight.

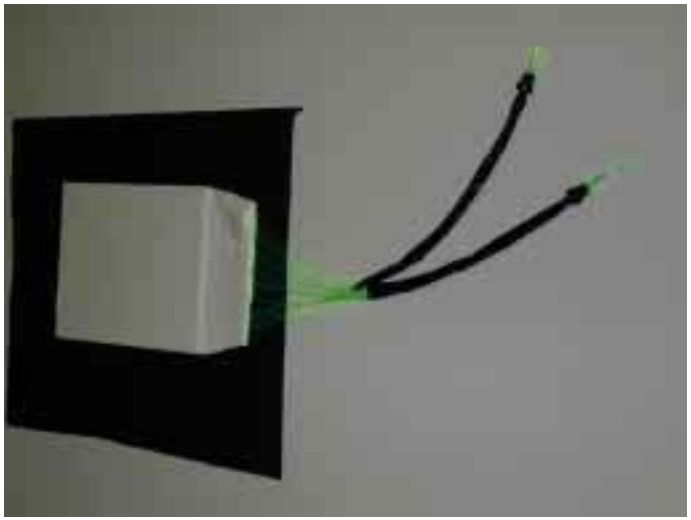


Detector Design
Prototyping

3. More than 15 different tiles were built and tested in the laboratory for the design trade study and for the performance verification

4. Fiber ribbon prototype was built and tested demonstrating at least 6 photoelectrons as required

5. 2 tiles were recently built to be a prototype of the flight unit. Currently they are being tested



ACD Detector Level IV Requirements

	Title	Summary	Verification
1	Self-veto not more than 20% at 300 GeV	ACD shall be divided into 89 scintillating tiles	I
2	Efficiency to single charged relativistic particles is 0.9997 over the whole area	2.1 Tiles shall be 1 cm thick, made of plastic scintillator	I
		2.2 Tiles shall be read out by wave-shifting fibers embedded in grooves with 5 mm spacing	I
		2.3 Wave-shifting fibers maybe coupled to fibers to reduce light attenuation	I
		2.4 Tiles shall be wrapped in TETRATEC light reflecting material	I
		2.5 The fiber ends shall be aluminized for the light reflection	I
		2.6 The tiles shall be overlapped in one direction to provide hermeticity	I
		2.7 The gaps in the other direction shall be covered by scintillating fiber ribbons to provide the hermeticity	I
		2.8 The total number of photoelectrons from each tile shall be at least 20	T
3	PMT Redundancy	Each tile shall be read out by 2 PMTs	I
4	Resistance to the puncture by micrometeoroid	Each tile two fiber bundles shall be separately light-tightened	I

T- Test I - Inspection

Detector Design Summary

Design is understood and complete

- Baseline PMT chosen
- Sizes determined
- Redundancy is robust against PMT failure (1 HXTE PMT of 25 of the same type failed after launch)
- Design has been shown to meet science requirements

Detector Design
Issues and Concerns

- More work is planned to measure carefully the light yield, including the deconvolution of Landau and statistical fluctuations
- The design of the bottom (the 4-th) ACD row, which currently is a single, long tile, shall be completed. We do not expect the problems here.
- Fiber ribbons to seal the gaps between tiles shall be prototyped and tested before PDR
- Validate system performance with electrons and protons on balloon flight, analysis to be completed by PDR
- Measure uniformity of the tile response

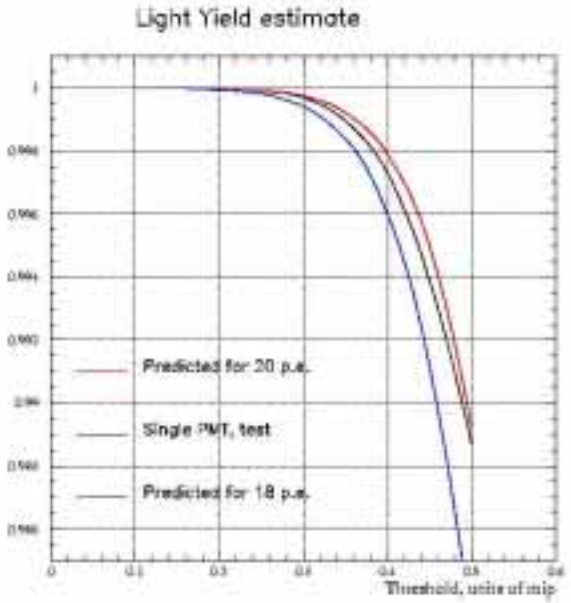
Detector Design
Conclusions

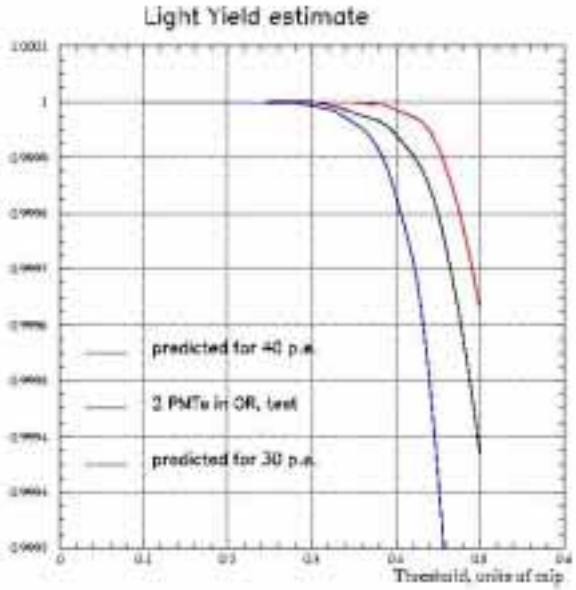
- **Practically all issues on the scientific proof of the design are answered positively to meet the requirements**
- **Experience has been established**
  - **over 45 tiles built to date**
  - **balloon unit established system level performance on muons on sea level**
- **Extensive simulations**
  - **effect of gaps**
  - **segmentation study, which include backsplash effect**

Back-up

Detector Design
Tile Design: Light Yield

The light yield was estimated by fitting experimental efficiency curves with that predicted by Poisson fluctuations for given number of p.e. The estimate for the single PMT is shown on the left, and for two PMTs in "OR" on the right





Back-up

Detector Design
Tile Segmentation Requirement

- Requirement flowdown
  - SRD does not specify the effective area we need at >60°
  - It does say for >60° incidence we require <6% (goal 3%) energy resolution.
    - Explanatory footnote: "Effective area for side incidence is 0.1 to 0.2 that of normal incidence for high resolution measurements."
  - This requires calorimeter depth of 17-18 radiation lengths
  - Selection: we must require at lease one tracker layer with "no- hit" be in the path of these events and the ACD must not be "hit" either.
- LAT team adopted

  Efficiency > 80% at 300 GeV relative to that at few GeV
- Segmentation is driven by the inverse square law.

Back-up

Detector Design
Segmentation

Effective Area

- Effective Area means pure area, reduced for the backsplash, calculated according to our formula for given distance between the ACD and the calorimeter entry points and crossed ACD tile area. Energy of 300 GeV and threshold of 0.3 mip are used
- Pure Area for the events (parallel flux, uniformly distributed over the area) entering GLAST through the ACD was calculated as following:

- for the top entry $S_{eff} = \frac{N_s}{N_\Sigma} \cdot S_{top} \cdot \cos(\Theta)$

- for the side entry $S_{eff} = \frac{N_s}{N_\Sigma} \cdot S_{row} \cdot \sin(\Theta) \cdot [\sin(\Phi) + \cos(\Phi)]$

where Θ and Φ are respectively zenith and azimuth angles,

N_Σ is the total number of events

N_S is the number of events which have a path in a calorimeter longer than 8.5 X_0 (face-to-face calorimeter thickness) or 15 X_0

S_{top} and S_{row} are the area of respectively the ACD top surface or the side tile row

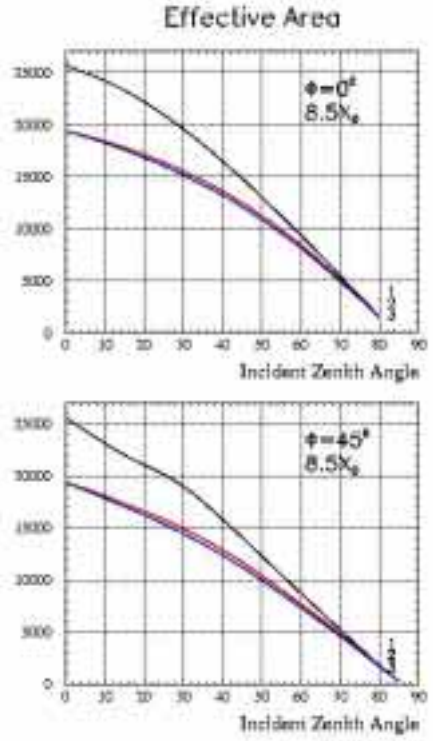
Detector Design
Segmentation

Back-up

Effective Area

Tile size effect on Effective area:

- all events are required to enter more than 15 cm above a calorimeter (4-th ACD row is not in use). Top entry is included
- Black line - pure area (no backsplash)
- Red line - baseline segmentation (145 tiles)
- Blue line - reduced segmentation (89 tiles)



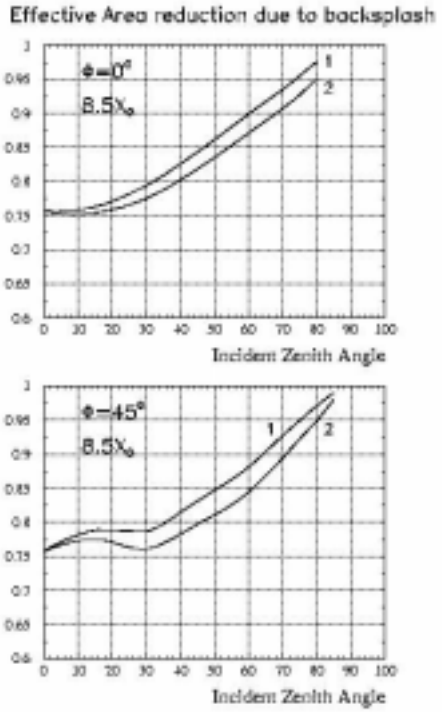
Back-up

Detector Design
Segmentation

Effective Area

Effective area reduction due to backsplash at 300 GeV:

- **Line 1 - baseline segmentation**
- **Line 2 - reduced segmentation**



Detector Design
Segmentation

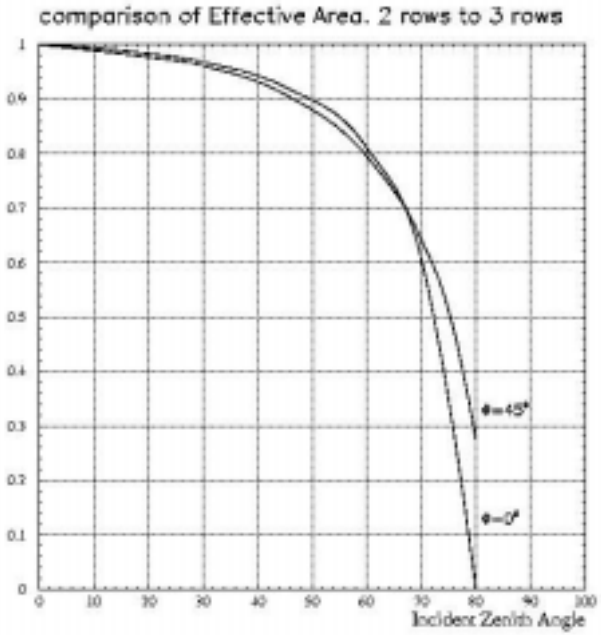
Back-up

Effective Area

Further tile number reduction:

- **Comparison of Effective Area - the ratio between (Top + 2 upper ACD rows, 30cm above calorimeter) to the (Top + 3 ACD rows with reduced segmentation in 3-rd row, 15cm above calorimeter). All events have paths in the calorimeter longer than 8.5 X_0**

This step would cause significant performance degradation



Back-up

Detector Design
Segmentation

Geometric Factor

- **Geometric Factor G (isotropic flux, uniformly distributed over the area) was calculated according to the expression:**

$$G(>X_0) = \frac{N_S(>X_0)}{N_\Sigma} \leftarrow \pi \leftarrow S$$

where $N_S(>X_0)$ is the number of events which have a path in a calorimeter longer than given number of X_0,

N_Σ is the total number of events

S is the area of considered segment (tile row or ACD top surface)

- **Effective geometry means reduced for the backsplash**

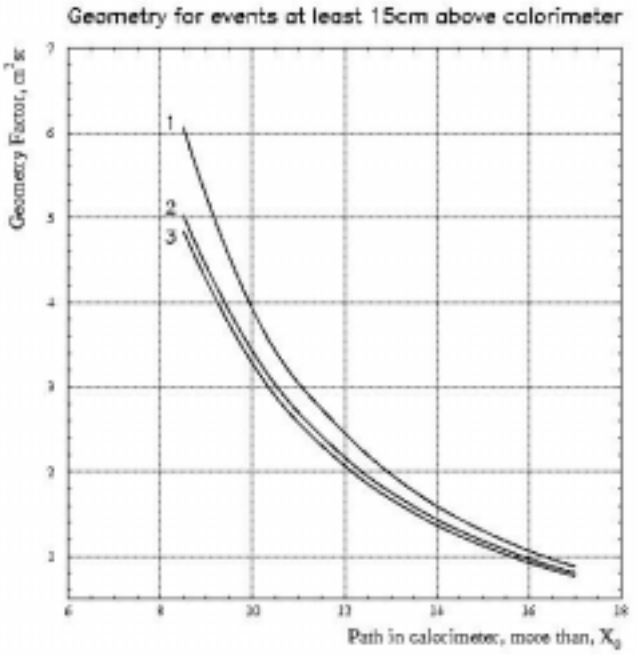
Back-up

Detector Design
Segmentation

Geometric Factor

Events are required to enter at least 15 cm above a calorimeter (3 ACD rows are in use), top and sides combined:

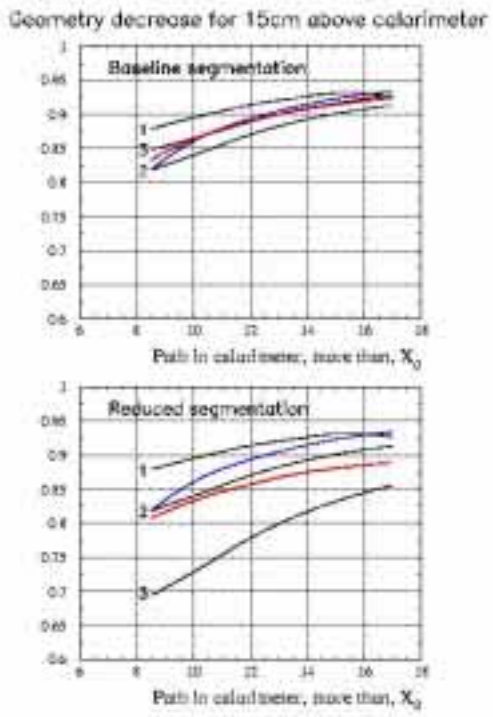
- **Line 1 - pure geometry**
- **Line 2 - effective geometry, baseline segmentation (145 tiles)**
- **Line 3 - effective geometry, reduced segmentation**



Back-up

Detector Design
Segmentation

Geometric Factor



- Events are required to enter at least 15cm above calorimeter
- Upper panel is for baseline segmentation, lower one - for the reduced segmentation
- Blue line - top entry only
- Red line - top and side entry together
- Lines 1 to 3 correspond to the tile row

Back-up

Detector Design

Tile Design - Trade study

1. Fiber Spacing Effect. All tiles are BICRON, TYVEK wrapped, multiclad fibers

Fiber Spacing	Relative Light Yield
2 cm	15.9
1 cm	18.1
0.5 cm	22.0
0.25 cm	20.2
Continuous	23.3

Back-up

Detector Design
Tile Design

2. Effect of Wrapping

Wrapping	Tile	Relative Light Yield
TYVEK	BICRON, 5mm fiber spacing, MC fibers	22.0
TETRATEC	- " -	24.5
Poliester	- " -	20.0
TYVEK	ElJen plastic, 10mm fiber spacing, single clad fibers	15.3
TETRATEC	- " -	17.2

10-12% of TETRATEC wrapping improvement over TYVEK is confirmed

Back-up

Detector Design
Tile Design

3. Aluminization of the fiber ends

Fiber Ends	Tile	Relative Light Yield
Razor cut	TYVEK, ElJen, 1cm SC fibers	14.1
Al, GSFC	- " -	15.3
Al, FNAL	- " -	?
Razor cut	TETRATEC, Bicron, 5mm MC fibers	24.5
Mylar	- " -	21.1

Back-up

Detector Design
Tile Design

4. Fiber Cladding. All tiles are ElJen, 1cm fiber spacing, TYVEK wrapped

Fibers	Relative Light Yield
Single Clad BCF-91A	14.1
Multiclad BCF-91A/MC	17.8

Multiclad fibers BCF-91A/MC will be used

Back-up

Detector Design
Tile Design

5. Scintillator manufacturer. All tiles are 1cm MC fiber spacing, TYVEK wrapped

Scintillator	Relative Light Yield
Bicron	18.1
ElJen	17.8

We found no significant difference between these manufacturers. The cost and scintillator sheet flatness are the issues.

Back-up

Detector Design
Tile Design

6. Other different designs - trade study

Tile	Tested Feature	Relative Light Yield
Bicron, TETRATEC	Light guides – clear fibers	5.5
Bicron, TYVEK	WSF glued to the tile edges	13.2
Bicron, TYVEK, 1cm MC fibers	2 fibers in one groove	19.0 (to compare with 18.1 for single fiber)
Bicron, TYVEK, 1cm MC fibers	WSF fibers are embedded inside the tile	11.0

No real competitors to the chosen design

Back-up

Detector Design
Tile Design

7. Use of half of fibers. The tiles are Bicron, 5mm MC fiber spacing, wrapped in TETRATEC

Number of readout fibers	Relative Light Yield
All fibers	24.5
Half fibers	11.9

Use of 2 PMTs reduces the light for each PMT by 50%

Mechanical Design
Thomas Johnson

Mechanical System

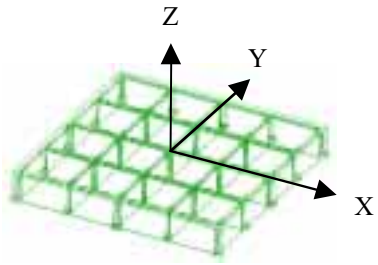
- **Outline**
  - Mechanical Team
  - Mechanical Requirements
  - Interfaces
  - Mechanical Design
    - Anticoincidence Detector (ACD)
      - Base Electronics Assembly (BEA)
      - Tile Shell Assembly (TSA)
      - Tile Detector Assemblies (TDA's)
  - Tile Detector Assembly Sequence
  - Micrometeorite Shield/Thermal Blanket
  - Mass Budget
  - Mechanical Analysis
  - Thermal Analysis
  - Mechanical Trade Studies
  - Mechanical Ground Support Equipment
  - Verification Matrix
  - Issues and Concerns
  - Summary

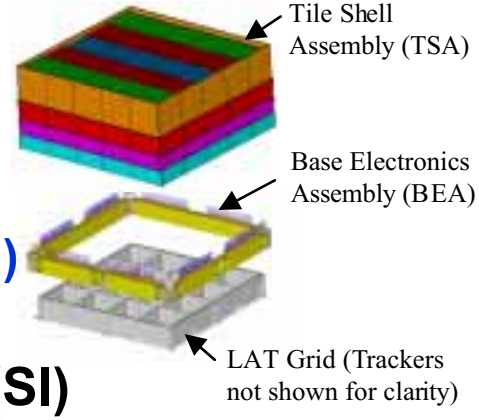
Mechanical Team

Tom Johnson	Mechanical Lead
Scott Murphy	Mechanical Engineer
Ian Walker	Mechanical Designer
Scott Gordon	Mechanical Analyst
Shelia Wall	Mechanical Analyst
Lou Fantano	Thermal Engineer
Carlton Peters	Thermal Engineer
Wes Alexander	Fabrication Engineer

Mechanical Requirements

- Mass Allocation: 205 kg (without reserve)
- X, Y, Z Coordinate System with the X-Y plane located on the top surface of the LAT Grid. 0,0,0 is located at the geometric center of the top surface of the LAT Grid
- Center of Gravity: x=y<5 mm (TBR), z<393 mm
- Volume (ACD & Shield): Ref. LAT-DS-00038-2)
  - Inside: LAT Grid: 1574 x 1574 x -204.7 (mm)
    LAT Tracker: 1515.5 x 1515.5 x 650 (mm)
  - Outside: 1796 x 1796 x 1015 (mm)
- System of Units: International System of Units (SI)
- Operational life on orbit: 5 years with a 10 year goal
- ACD shall cause interactions of less than 6% of the incident gamma radiation
- Vent all components to prevent damage due to Delta launch accent pressure profile





Mechanical Requirements (cont.)

ACD Design Limit Loads (G's)[1,2]		
	Event	
Direction	Liftoff/Transonic (Max Lateral)	MECO (Max Axial)
Thrust[3]	+3.25/-0.8	+6.6
Lateral	+4.0	+0.1

Notes:

(1) Defined from preliminary in-house GLAST CLA. Will be updated as additional CLA results become available.

(2) Thrust and lateral loads applied simultaneously for each event in all combinations.

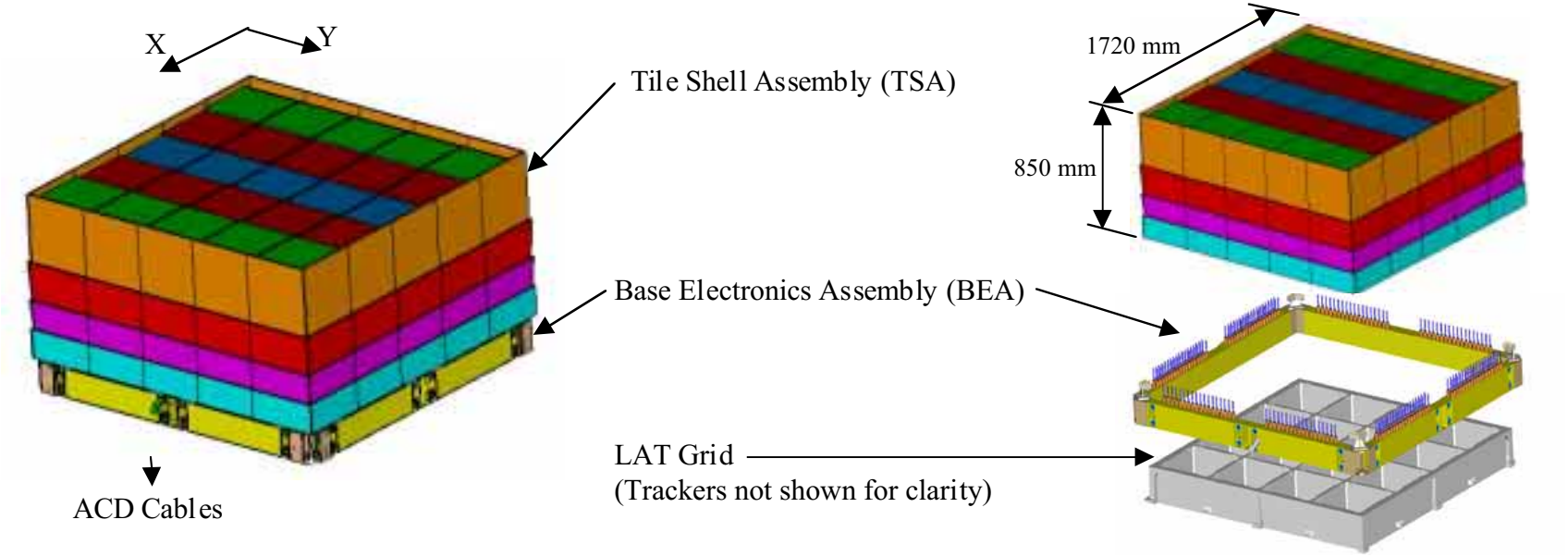
(3) Plus indicates compression load and minus indicated tension.

- **First Fundamental Frequency: Goal of >50 Hz**
- **Provide micrometeoroid protection for the tiles such that the mean rate of penetrations over the entire ACD area is < 0.01/year**
- **The thermal blanket/micrometeoroid shield shall have mass per unit area density <0.32 g/cm^2 in order to minimize secondary gamma-ray production by undetected cosmic ray interactions**
- **The ACD shall survive loads imposed by ground handling, transportation, environmental test, launch, and on-orbit**

Interfaces

- All interfaces to be controlled by LAT-DS-00241-1 LAT-ACD Subsystem Mechanical Interface Control Document
- Mechanical Interfaces
  - ACD Base Frame interfaces to the LAT Grid
  - 8 point interface - At 4 corners and center of each side
- Thermal Interfaces
  - Conductive heat transfer from base frame to Grid at bolted interface points
  - Radiative thermal interface between ACD inside surface and LAT Trackers and Grid

ACD Mechanical Design



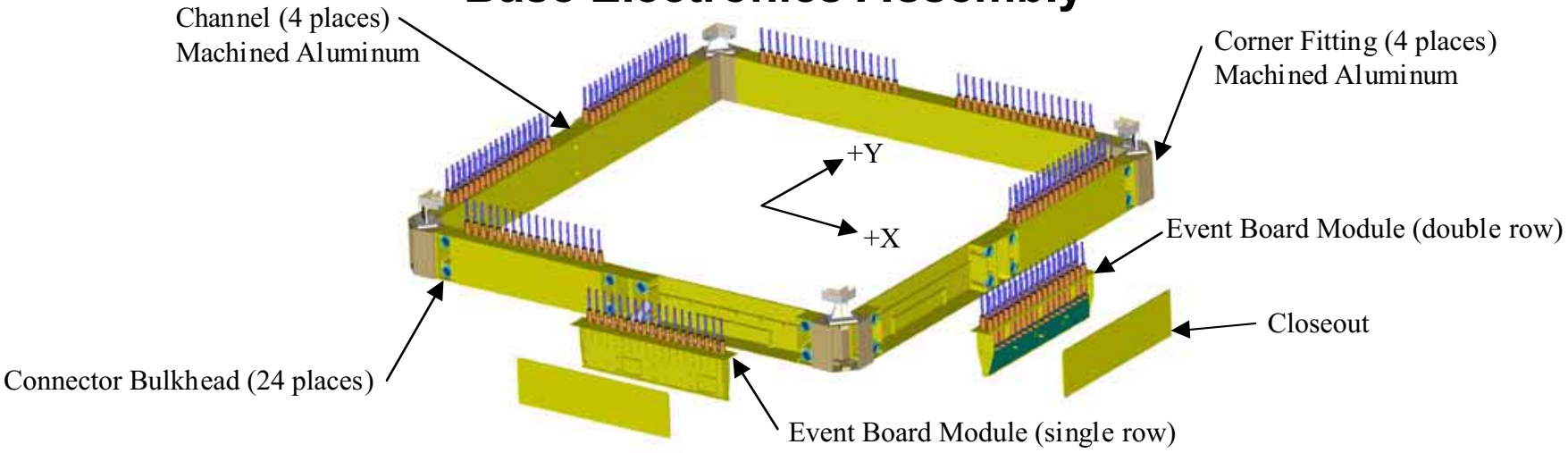
- **The ACD is comprised of two primary sub-assemblies. The Base Electronics Assembly (BEA) and the Tile Shell Assembly (TSA)**
- **Base Electronics Assembly**
  - **Mechanical Support Structure for the ACD**
    - **Supports Tile Shell Assembly**
    - **Houses ACD Electronics**
    - **Provides all Electrical and Mechanical interfaces to the LAT**
  - **The BEA Base Frame is constructed with machined aluminum components bolted and riveted together**

ACD Mechanical Design (cont.)

- Tile Shell Assembly
  - Supports the Tile Detector Assemblies and their associated fiber cables
  - Supports the Micrometeorite Shield/Thermal Blanket
  - Structural shell is constructed using composite honeycomb panels
- Calculated Center of Gravity: 0,0,332 mm
- Estimated mass: 228.4 kg
- Interface cables between LAT and ACD come down on the +X and -X sides (12 cables on each of the +/-X sides route to the TEM boxes on the bottom of the Grid)
- Advantages to ACD Mechanical design
  - Clean interface to the LAT
  - Easy to integrate
  - Allows TSA and BEA to be integrated and tested in parallel
  - No CTE mismatch between LAT and ACD

BEA Mechanical Design

Base Electronics Assembly



- **Mechanical Support Structure for ACD**
  - **Supports Tile Shell Assembly**
  - **Provides all Electrical and Mechanical Interfaces**
  - **Aluminum structure (bolted and riveted joints)**

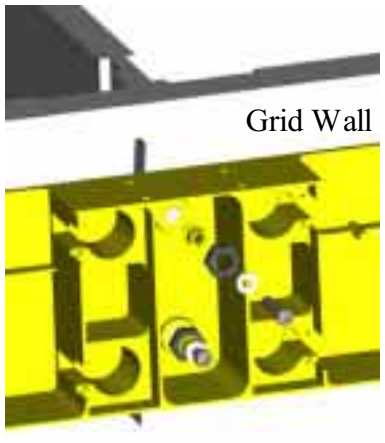
- **Electrical Housing and Interface for ACD**
  - **Houses and protects ACD electronics**
  - **LAT Cable Interfaces (bulkhead connectors)**
  - **Electrical shielding - Fully enclosed electronics for EMI**

BEA Mechanical Design (cont.)

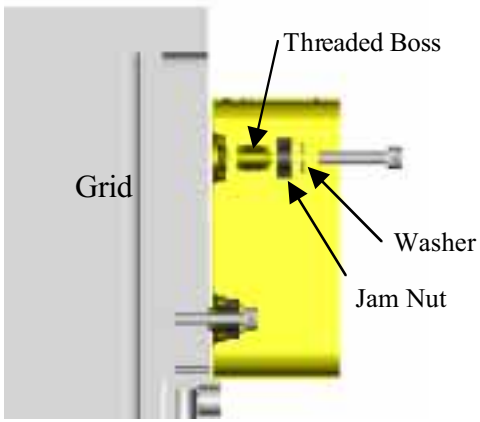
- **Mechanical Interface for the ACD to LAT**
  - **Provides 8 point mount to LAT Grid: 4 corners + 4 sides (center)**

Center Mount

Front View

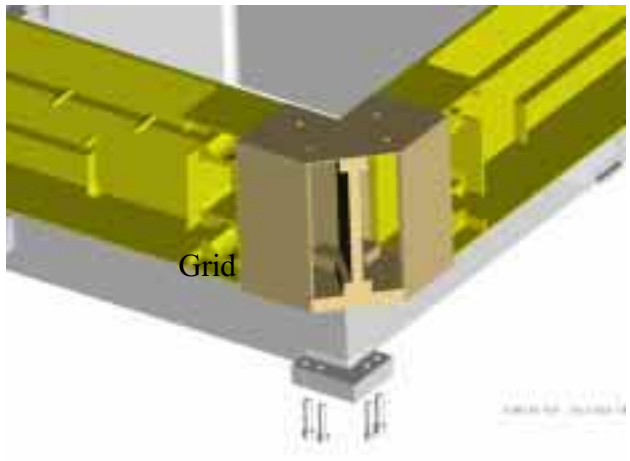


Side View



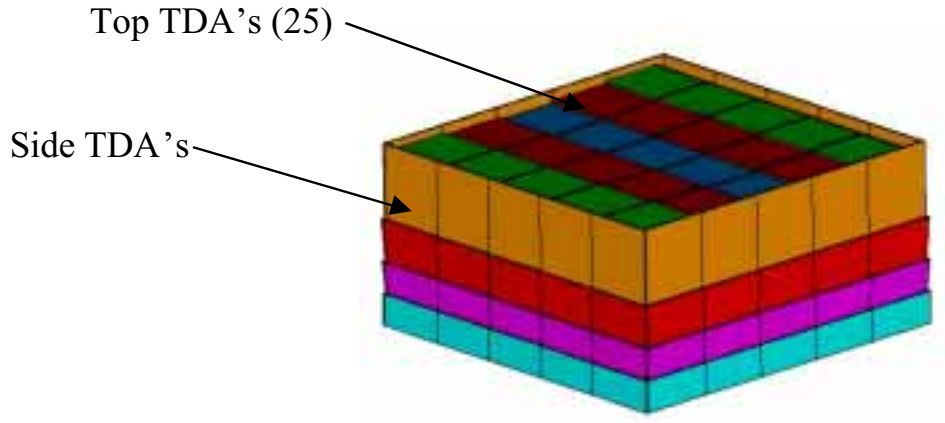
•BEA Center Mount (4 sides)
- •Accessed from side using standard tools
- •Standard hardware with exception of threaded boss
- •Threaded boss allows easy integration
- •Increases thermal contact with Grid
- •Improves BEA's stiffness.

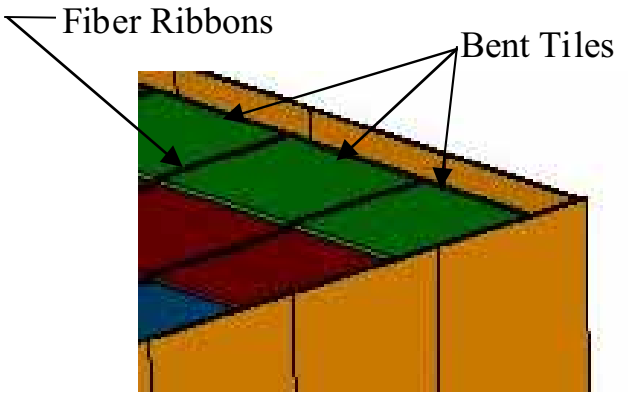
Corner Mount



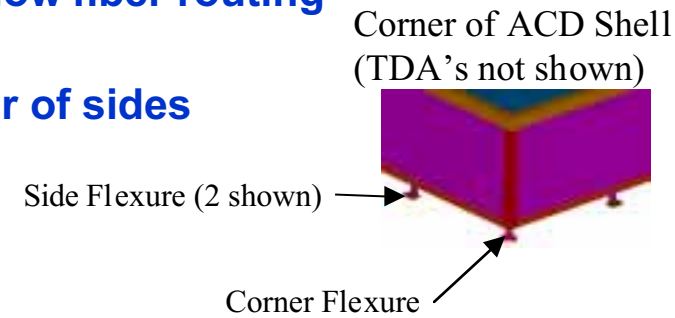
•BEA Corner Mount (4 corners)
- •Allows for ease of integration
- •Requires vertical access to remove ACD

TSA Mechanical Design

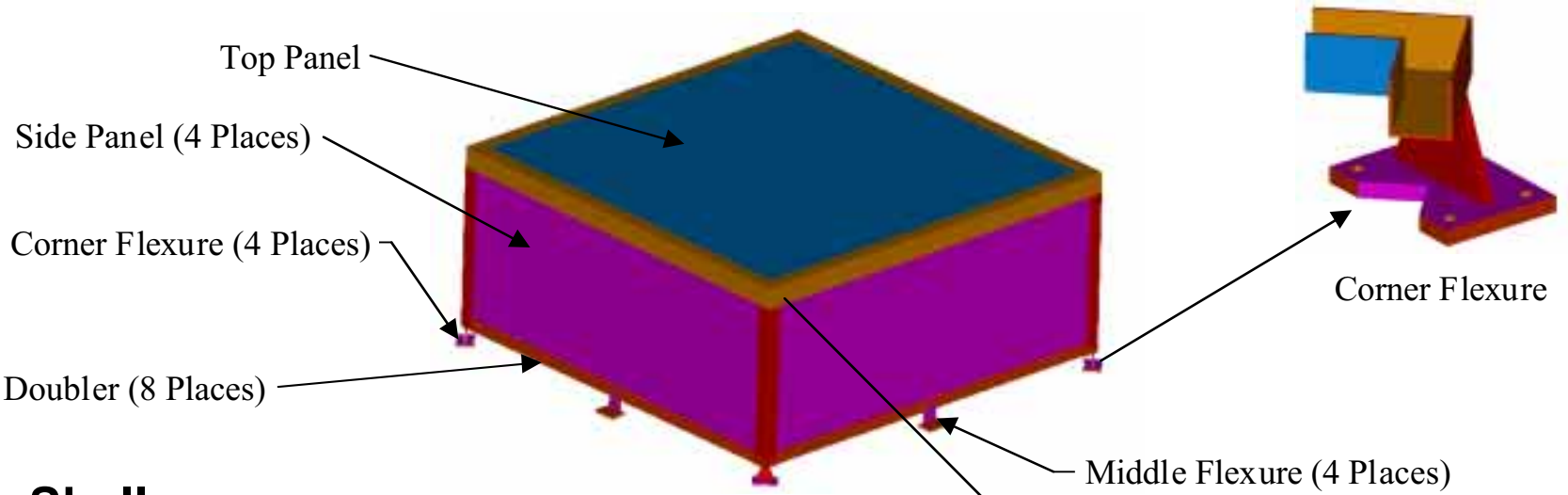




- **25 TDA's on Top and 16 TDA's on each side (3 rows of 5 TDA's and one single TDA on the bottom row**
- **Tile Detector Assemblies are overlapped 1 cm in 1-dimension**
  - **Gap between TDA's in 2nd dimension is covered with Fiber Ribbons**
  - **Vertical separation between TDA's is 1 mm**
- **All fiber cables from the top are routed down the X sides**
  - **Top side tiles on the X sides are bent to allow fiber routing**
- **TSA to BEA Interface**
  - **Flexures at 8 points - At corners and center of sides**
  - **All flexures single blade**
  - **Material: Titanium**
  - **Bonded to shell and bolted to BEA**



TSA Mechanical Design (cont.)



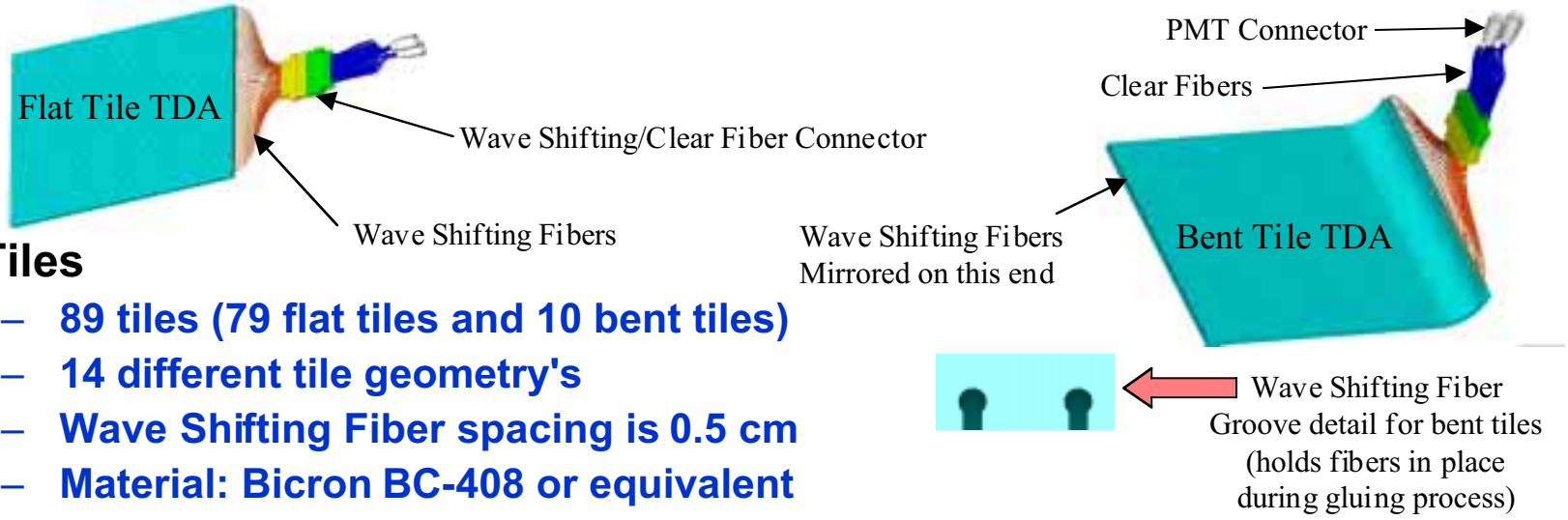
- **Shell**
  - **Honeycomb Panel Construction**
  - **Composite "extrusions" used for edge fittings**
  - **Dimensions**
    - **Outside - (1600.3 mm x 1600.3 mm x 701.75 mm high)**
    - **Inside - (1540.5 mm x 1540.5 mm x 645.95 mm high)**
    - **Honeycomb side panels are 26.4 mm thick**
    - **Honeycomb top panel is 51.8 mm thick**
  - **Materials**
    - **Core - Korex 3/16" - 2.0 psf**
    - **Facesheets - M46J/RS-3 - 0.5 mm thick**

TSA Mechanical Design (cont.)

- Shell is spaced 10 mm above the top of the Grid
- Shell supports the TDA's and Micrometeoroid Shield/Thermal Blanket
- Click Bond type harness tie-downs will be used to attach fiber bundles to shell
- Fiber Ribbons
  - 4 fiber ribbons across the gaps in the top continue down X sides with PMT's on each end
  - 4 fiber ribbons cover the gaps on each of the Y sides (total of 8 separate fiber ribbons on Y sides). One PMT on each Y side ribbon.
- % Radiation Absorbed

Layer	Equivalent Thickness (cm)	Radiation Length (cm)	% Radiation Adsorbed
Nextel Woven Fabric 312*	0.0283	6	0.47%
Solimide Foam* (2.8 cm)	0.016	28.6	0.06%
Thermal Blanket	0.1	28.7	0.35%
Kevlar*	0.05	20	0.25%
TDA Wrap (Tetratec)	0.025	15.8	0.16%
TDA Wrap (Tedlar)*	0.025	28.6	0.09%
Scintillator	1	42.5	2.33%
GrEP Facesheets	0.1	23.1	0.43%
Korex Core*	0.0587	17.8	0.33%
* Materials radiation length calculated and/or approximated		TOTAL	4.46%

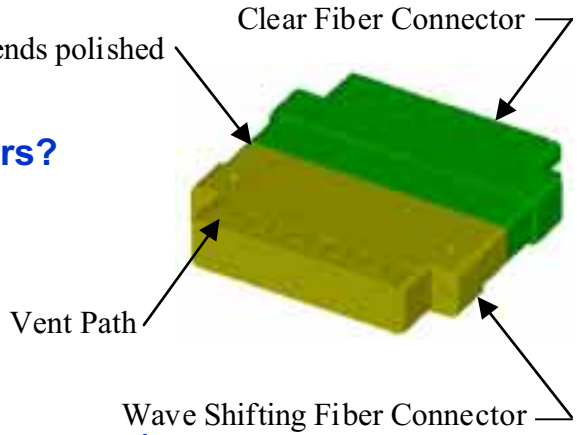
TDA Mechanical Design

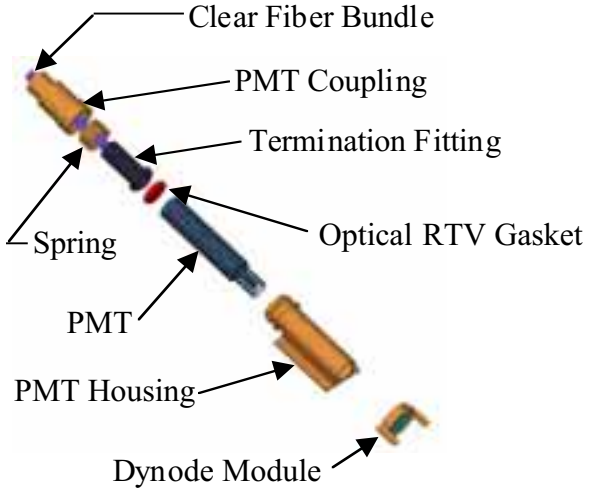


- **Tiles**
  - 89 tiles (79 flat tiles and 10 bent tiles)
  - 14 different tile geometry's
  - Wave Shifting Fiber spacing is 0.5 cm
  - Material: Bicron BC-408 or equivalent
  - Thickness: 10.00 +/- 0.15 mm with a flatness of 0.2 mm over 350 mm
  - Minimum bend radius of Scintillator Tiles: 4 x thickness of tile
- **Fibers**
  - Minimum bend radius of fiber: 25 x diameter of fiber
  - Wave Shifting Fibers (WSF)
    - 1 mm diameter
    - End bonded in tile to be mirrored with Vapor Deposited Aluminum
    - Material: Bicron BCF-91AMC or equivalent
  - Clear Fibers
    - 1.2 mm diameter
    - Material: Bicron BCF-98

TDA Mechanical Design (cont.)

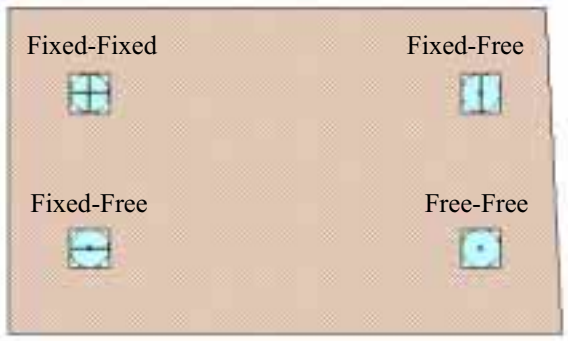
- **Fiber connectors**
  - **Wave Shifting Fiber to Clear Fiber connectors**
    - **Why switch from Wave Shifting Fibers to Clear Fibers?**
      - **Lower light loss than Wave Shifting Fibers**
      - **Easier handling and integration of TDA's**
    - **Hold up to 68 fibers in two rows**
    - **Provide venting of tiles and fiber bundles**
    - **Connectors pinned to maintain alignment**
    - **Provide light tight interface (wrappings taped to connectors)**
    - **Increase diameter of clear fibers to increase tolerance**
    - **Fabrication Method: Molding**
    - **Material: Liquid Crystal Polymer**
  - **PMT fiber connector and housing**
    - **Connects fiber bundle to PMT Window**
    - **Spring loaded to control preload**
      - **Eliminates overstressing PMT window**
      - **Eliminates gapping**
      - **Eliminates the need for precise positioning**
    - **Clear fibers bundled into circular connector**
    - **PMT housing and coupling are aluminum**
    - **Fiber Termination Fitting is Ultem**

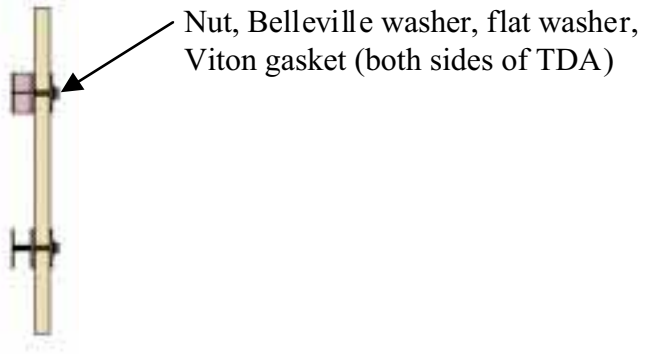




TDA Mechanical Design (cont.)

- Adhesive
  - Bicron BC-600 used to bond WSF to Tiles
  - Bicron BC-600 used to bond fibers into Fiber and PMT connectors
- TDA Wrappings
  - Reflective wrapping: Tetratec
  - Opaque wrapping: Black Tedlar
- Vendor to fabricate and assemble TDA's has been selected
- TDA Tiedowns
  - Four point kinematic mount
  - Provide compliance for thermal expansion and contraction of TDA's
  - TDA's attached using a threaded stud and nut
  - Viton gasket used on both sides of TDA to maintain light tight seal
  - Mounts bonded to shell





TDA Assembly Sequence

- Machine scintillator tiles to specified size.
- Machine grooves in the scintillator tiles (ball groove for bent tiles)
- Polish the edges of the scintillator tiles
- For bent scintillators, bend by using a warm temperature bending process
- Anneal the scintillator
- Cut, polish, mirror, and test wave shifting fibers
- Glue mirrored end of waveshifting fibers into grooved scintillator tile
- Install and glue transmitting end of waveshifting fibers into fiber connector
- Cut and polish the fibers and connector face perpendicular to the fiber axis
- Anneal the scintillator and wave shifting fiber assembly
- Wrap scintillator tile with Tetratec
- Wrap tile and fibers with two layers of black Tedlar
- Test TDA Assembly (light yield, uniformity, & light tight)

Micrometeoroid Shield/Thermal Blanket

- Micrometeoroid shield is required to prevent potential light leaks in TDA's
- Mass requirement < 0.3 g/sqcm
- Thickness requirement < 3.27 cm

- Preliminary Design Concept

Layer	Thickness (cm)	Areal Density (g/sqcm)
Nextel Woven Fabric 312	0.025	0.043
Solimide Foam	0.7	0.0054
Nextel Woven Fabric 312	0.025	0.043
Solimide Foam	0.7	0.0054
Nextel Woven Fabric 312	0.025	0.043
Solimide Foam	0.7	0.0054
Nextel Woven Fabric 312	0.025	0.043
Solimide Foam	0.7	0.0054
Thermal Blanket	0.32	0.0368
Kevlar	0.05	0.034
TOTAL	3.27	0.2644

- NASA's Micrometeoroid Shield experts at JSC have been tasked to verify and optimize design
- Orbit simulations using a 3D model of the GLAST Observatory have been performed
- High velocity impact testing of the proposed materials is underway
- When design is finalized a test unit will undergo impact testing
- The thermal properties of the shield will be tested and the required amount of thermal blankets will be added to the shield

Mass Budget

Item	Quantity	Estimted Mass (kg)	Calculated Mass (kg)	Actual Mass (kg)	Total Mass without margin (kg)	Total Mass with margin (kg)*
Mechancal Hardware						
Shell	1		25.4		25.4	27.94
Tile Tiedowns	105	0.04			4.2	5.04
Shell/Base Corner Flexures	4		0.58		2.32	2.552
Shell/Base Middle Flexures	4		0.5		2	2.2
Shell/Base Flexure Hardware	1	0.06			0.06	0.072
Base Frame with closeouts	1	28			28	33.6
ACD/LAT interface hardware	1	0.06			0.06	0.072
				Total Mechanical	**62.04**	**71.48**
Tile Detector Assemblies						
Tiles	1		91.05		91.05	100.155
Fiber	1	5.76			5.76	6.912
Fiber Ribbons (850 mm)	8	0.0175			0.14	0.168
Fiber Ribbons (3370 mm)	4	0.0696			0.2784	0.33408
Fiber connectors	65		0.0295		1.9175	2.10925
Fiber/PMT connectors	194	0.0125			2.425	2.91
Reflective wrapping	1	1.35			1.35	1.62
Opaque wrapping	1	5.7			5.7	6.84
Fiber to Tile adhesive	1	0			0	0
Wrapping adhesive	1	0.4			0.4	0.48
Fiber tiedowns	360	0.005			1.8	2.16
				Total TDA's	**110.82**	**123.69**
Electronic Hardware						
Event Modules	12	2			24	28.8
Cable tiedowns	20	0.15			3	3.6
E Board mounting hardware	1	0.5			0.5	0.6
				Total Electronics	**27.50**	**33.00**
Thermal Hardware						
Thermal control heaters	1	0.25			0.25	0.3
Thermostats	1	0.1			0.1	0.12
Wiring and tiedowns	1	0.3			0.3	0.36
Micrometerite/Thermal Blanket	1		27		27	29.7
Micro/Thermal blanket hardware	1	0.4			0.4	0.48
				Total Thermal	**28.05**	**30.96**
* Factors used to calculate margin: 20% estimated, 10% calculated, 0% measured				**TOTAL ACD**	**228.41**	**259.12**

Mechanical Analysis - Dynamic Design Requirements

- **Swept Sine Vibration**

Sinusoidal Vibration Levels at Spacecraft Separation Plane			
Axis	Frequency (Hz)	Acceptance (zero to peak)	Qualification (zero to peak)
Thrust	5 to 100	1.0 g	1.4 g
Lateral	5 to 100	0.7g	1.0 g

  - Above generic levels taken from Delta II Payload Planners Guide
  - Mission specific levels for GLAST will be derived from coupled loads and flight data
  - ACD specific levels will be derived from a basedrive analysis of GLAST observatory

- **Random Vibration**
  - Random vibration levels from GEVS
  - Levels attenuated for weight of ACD (245 kg).
  - Acoustic test will most likely be performed at ACD level instead of random.

ACD Random Vibration Levels		
	ASD Level (G^2/Hz)	
Frequency (Hz)	Acceptance	Qualification
20	0.01	0.01
20 - 50	0 dB/oct	+2.3 dB/oct
50 - 800	0.01	0.02
800 - 2000	0 dB/oct	-2.3 dB/Oct
2000	0.01	0.01
Overall	4.4 Grms	5.6 Grms

Mechanical Analysis - Dynamic Design Requirements (Cont.)

- **Acoustic**
  - Acoustic levels from Delta II Payload Planner's Guide
  - Levels for a 7920 Vehicle w/ 10' Composite Fairing and 3" Blankets
    - Flight OASPL = 140.6 dB
    - Proto-Flight OASPL = 143.6 dB

- **Shock**
  - Levels for ACD have not yet been determined
  - Need to work with spacecraft vendor to specify shock levels for ACD
  - Shock sources
    - Explosive bolts at spacecraft separation plane
    - Solar Array release mechanism

Mechanical Analysis - Finite Element Model

- **ACD Material Properties**

Component	Material	Young's Modulus (N/m**2)	Shear Modulus (N/m**2)	Density (kg/m**3)
ACD composite facesheets	M46J/934 Quasi-Isotropic Laminate	8.96E+10		1.66E+03
ACD composite core	Korex(Dupont), 3/16-2.0		5.86E+07	3.20E+01
Baseframe	Aluminum 6061-T6	6.83E+10		2.71E+03
Flexures	Titanium Ti-6Al-4V	1.10E+11	4.27E+10	4.43E+03

- **Finite Element Model**
  - ACD FEM delivered to SLAC
  - Boundary Conditions (Per side of base frame)
    - Corners constrained in 6 DOF representing two bolt attachment into LAT
    - Mid-side constrained at two bolt locations (3 DOF each)
  - Details
    - 1500 elements
    - 1477 nodes

Mechanical Analysis - Finite Element Model (cont.)

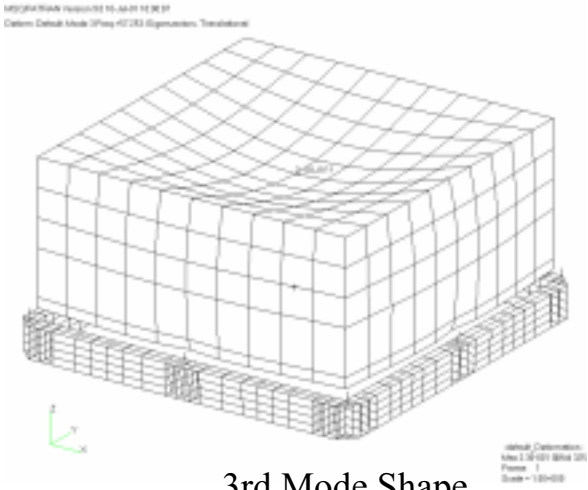
MOMENTS OF INERTIA ABOUT ORIGIN
BASIC COORDINATE SYSTEM

I-XX	I-YY	I-ZZ	I-XY	I-YZ	I-ZX
1.43E+02	1.42E+02	1.84E+02	-6.83E-09	1.07E-06	1.07E-06

EFFECTIVE MODAL WEIGHTS

MODE #	FREQUENCY (hz)	X-WT (kgs)	Y-WT (kgs)	Z-WT (kgs)	I-XX (N-m **2)	I-YY (N-m **2)	I-ZZ (N-m **2)	DESCRIPTION
1	54.91	161.85	0	0	1.35E-06	4.04E+01	1.51E-14	Lateral mode of ACD
2	54.91	0	163.71	0	4.04E+01	1.35E-06	4.25E-13	Lateral mode of ACD
3	57.25	0	0	47.43	6.84E-11	1.02E-10	6.57E-11	Drumhead mode of ACD Top
4	58.35	0	0	0	5.62E-10	6.79E-08	1.25E+00	
5	58.36	0.43	0	0	6.16E-10	1.20E-01	6.73E-07	
6	58.55	0	0	0.16	1.10E-06	7.38E-11	1.23E-09	
7	58.56	0	4.99	0	3.62E-01	7.62E-11	1.34E-09	
8	60.5	0	0	0	1.38E-13	1.66E-11	6.31E-02	
9	60.5	0.04	0	0	2.93E-13	9.29E-03	9.87E-11	Low mass modes within
10	60.51	0	0	0	2.55E-11	8.13E-14	1.38E-12	Base Frame
11	60.51	0	0	0	2.39E-03	8.35E-13	2.28E-13	
12	64.41	0	0	0	2.02E-10	3.10E-09	3.63E-02	
13	64.41	0	0	0	2.34E-10	3.19E-04	3.56E-07	
14	64.41	0	0	0	1.68E-09	2.25E-11	2.16E-09	
15	64.41	0	0.22	0	8.50E-03	9.26E-12	8.91E-10	
16	65.33	0	0	0	1.19E-12	2.92E-12	6.21E-12	ACD Side Panel mode
17	66.39	0	0	0	2.68E-08	2.67E-10	1.09E+00	
18	66.4	0	0.03	0	7.52E-03	2.62E-10	3.82E-06	
19	66.62	4.69	0	0	4.31E-12	2.00E-01	1.23E-09	
20	66.65	0	0	0	2.57E-12	7.45E-09	7.60E-10	
21	68.82	0	0	0	1.05E-12	8.09E-14	2.33E-02	
22	68.83	0	0	0	1.12E-04	1.70E-13	1.42E-10	Low mass modes within
23	68.84	0	0	0	4.06E-15	2.56E-03	4.59E-14	Base Frame
24	68.84	0	0	0	1.95E-14	3.14E-12	3.70E-13	
25	73.28	0	0	0	6.83E-11	3.07E-10	1.31E-01	
26	73.28	0	0	0	1.15E-04	4.65E-10	7.61E-08	
27	73.29	0.15	0	0	3.28E-12	1.56E-02	2.64E-09	
28	73.29	0	0	0	2.17E-12	4.05E-08	2.31E-09	
29	73.9	0	0	0	1.46E-11	5.25E-11	4.38E+01	ACD Side Panel mode
30	75.04	0	10.1	0	2.17E+01	1.34E-07	2.77E-11	ACD Side Panel mode

1st Mode Shape



3rd Mode Shape

Mechanical Analysis - Upcoming Work

- Analysis of thermally induced loads under operating and survival temperature limits
- Detailed strength assessment of ACD shell and base frame
- Acoustic analysis
  - Assessment of acoustic loading of ACD shell
  - Develop acoustic spectrum inside ACD shell for assessing LAT component vibration levels
- Derivation of swept sine vibration levels

Mechanical Analysis - Summary

- **Preliminary Margins of Safety**

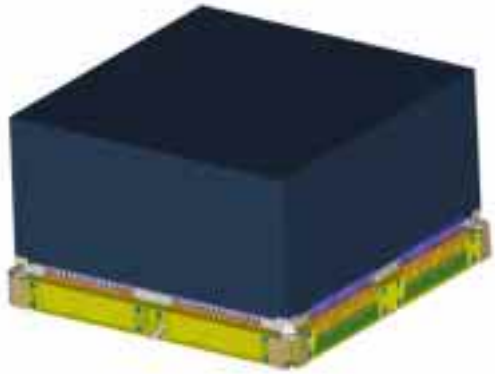
Component	Stress (GPa)	MS Yield	MS Ultimate	Location
Baseframe	16.5	10.7	11.5	Corner flange, flexure connection
Flexure	121.0	4.7	4.5	Corner Flexure
ACD Shell	21.6	N/A	6.7	Doubler, middle flexure connection

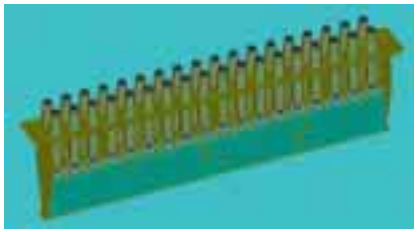
- **Predicted ACD shell deflections under design limit loads**

CASE	LOCATION	DISP (mm)	RQMNT (mm)
Max Lateral (RSS X & Y)	ACD Shell Side Panel	0.54	1.0
Max Vertical (Z)	ACD Top Panel	0.79	4.0

Thermal Analysis

- **Temperature Sensitive Components**
  - **ACD Event Boards**
    - **12 Electronics Boards are Mounted to Frame Structure**
      (+/- X sides 4 ea., +/- Y sides 2 ea.)
    - **Each board dissipates 1.5 watts (TBR) per board**
    - **18 watts (TBR) total power**
    - **TBD Temperature Requirements**
  - **ACD TDA's**
    - **No power dissipation**
    - **Material Operating Range (-60 to 50 C)**
    - **Survival Range (-120 [TBR] to 65 C)**



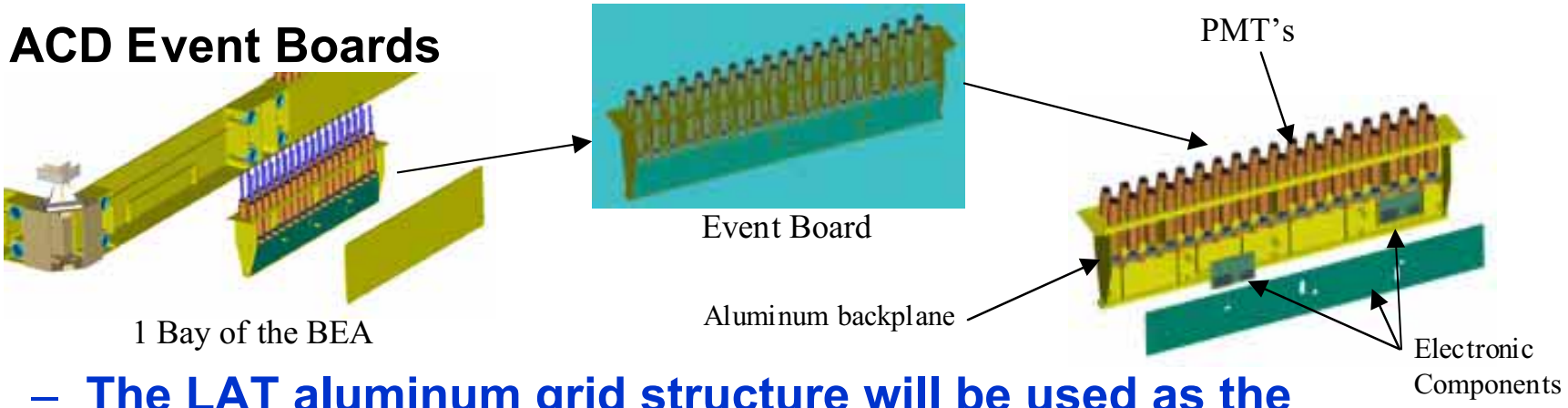


ACD Event Boards

ACD TDA's

Thermal Design Strategy

- **ACD Event Boards**



  - **The LAT aluminum grid structure will be used as the electronic boards heat sink**
  - **ICD with LAT (LAT-DS-00241-1 LAT-ACD) specifies that the grid operating temperature range is -10C to 25C**
  - **The conduction path between the boards and the grid will be modulated by thickening the frame, increasing the board to frame conductance, and frame to grid conductance parameters until satisfactory temperatures are achieved**
  - **Design analyses add and subtract 10 C to the grid operating range to assure a conservative design (-20C to 35C)**

Thermal Design Strategy

ACD Tile Detector Assemblies

- Satisfying the upper 50C tile temperature requirement is not a concern due to the silver Teflon outer blanket layer
- Satisfying the -60C minimum tile temperature requirement is a concern.
  - Outer MLI blanket layer gets extremely cold in the cold design case (-130C)
  - Tile temperatures will balance the heat flow radiated from the LAT with the heat flow through the MLI blanket
- Effective ACD emittance parameter will be specified in LAT/ACD ICD (LAT-DS-00241-1-D1)
- Perform thermal vacuum test to measure thermal insulation provided by micrometeoroid shield.
- Select appropriate number of outer blanket layers to satisfy tile minimum temperatures

Micrometeoroid Lay-up

Nextel Fabric
Solomide Foam
Nextel Fabric
Solomide Foam
Nextel Fabric
Solomide Foam
Solimide Foam
Thermal Blanket
Kevlar
ACD TDA's

Thermal Analysis

Conduction Only Thermal Analyses Performed to Establish ACD Event Boards/Frame/Grid thermal sensitivities

- **Base Line Configuration Assumptions**
  - **Minimum Frame thickness = 1 mm**
  - **Eight central frame locations with 2.54 cm diameter contact area per location**
  - **Sixteen corner locations with 20 cm^2 contact area per location**
  - **35C Grid Boundary Temperature**
  - **± X frame side has four boards per side and ± Y frame side has two boards per side**

- **Base Line Temperature Results**
  - **Thermal model calculates ±X board temperatures to be 64.2 C and the ±Y board temperatures to be 54.7**
  - **The acceptability of these temperatures is not known since no temperature requirements have been established.**

Thermal Parametric Analyses

Power Dissipation Parametric

	Power (W)	±X Boards (C)	±Y Boards (C)
	1.125	56.9	49.8
Base Line	1.5	64.2	54.7
	1.875	71.5	59.6

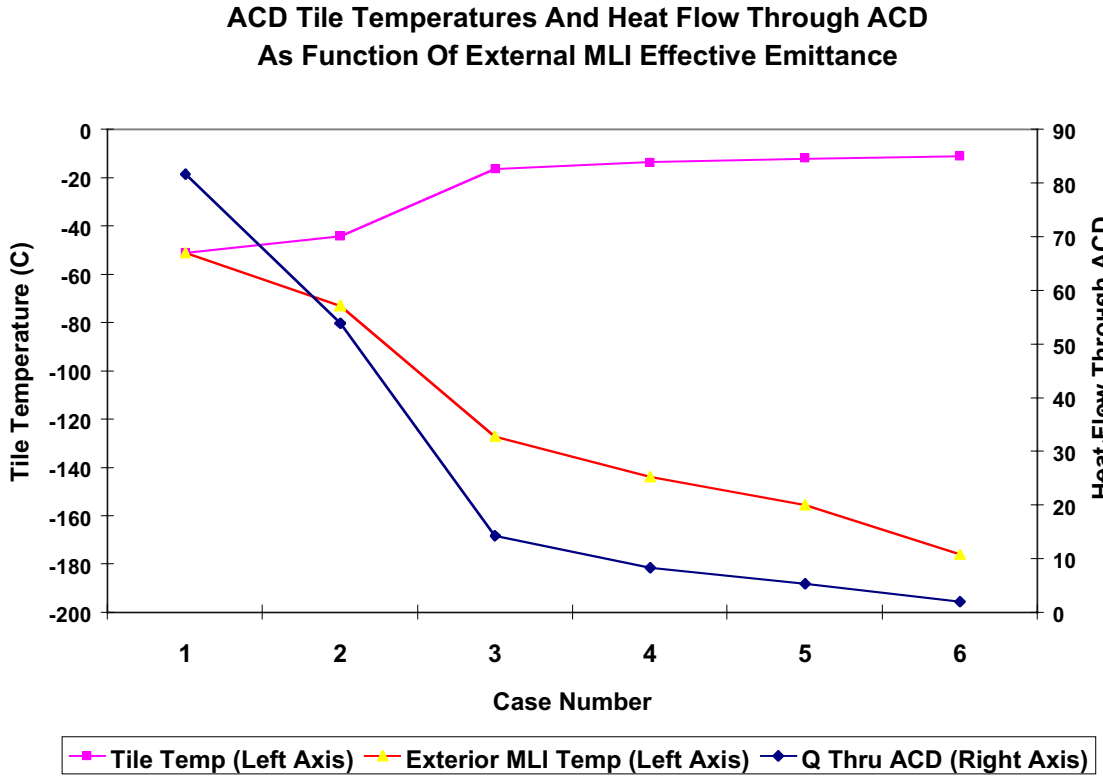
Frame Thickness Parametric

	Thickness (mm)	±X Boards (C)	±Y Boards (C)
Base Line	1.00	64.2	54.7
	1.50	58.3	51.7
	2.00	55.3	50.2
	5.00	49.9	47.5

Tile Thermal Analyses

- Cold Case Considered
- Thermal model developed to assess tile temperatures
  - Trackers towers assumed to be at -10 C
  - Tracker towers and ACD interior viewing trackers assumed to be high emittance
  - No delta T assumed between ACD interior and tiles
  - Dual series thermal resistance paths formed by the micrometeoroid shield and the outer MLI blanket layer
  - Outer MLI layer assumed to be high alpha / low emittance
  - Micrometeoroid shield thermal resistance assumed to be comprised of the 2.1 cm thick solimide foam
  - Manufacturers conductivity data assumed for solimide foam (0.045 W/MK)
- Parametric analyses performed to assess thermal performance assuming micro-meteoroid shield only and incrementally greater levels of exterior MLI performance

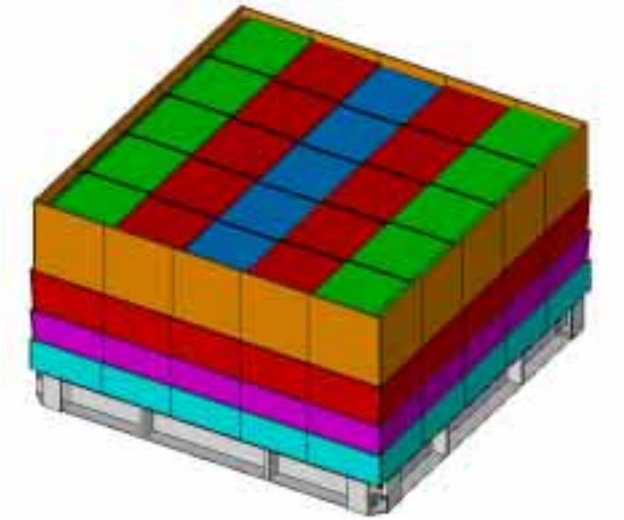
Tile Thermal Analyses (cont.)



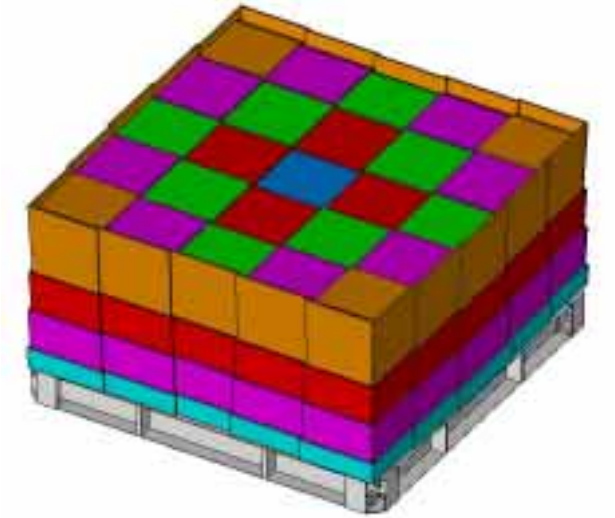
Case 1: Thermally Short Both Solomide Foam and Exterior MLI Blanket
Case 2: Solomide Foam Conductivity=0.045 W/MK ; Thermally Short Exterior MLI Blanket
Case 3: Solomide Foam Conductivity=0.045 W/MK ; MLI Blanket E*=0.10
Case 4: Solomide Foam Conductivity=0.045 W/MK; MLI Blanket E*=0.05
Case 5: Solomide Foam Conductivity=0.045 W/MK; MLI Blanket E*=0.03
Case 6: Solomide Foam Conductivity=0.045 W/MK; MLI Blanket E*=0.01

Mechanical Trade Studies

1-Dimension tile overlap verses 2-Dimension tile overlap



- 1-Dimension Overlap
  - Fiber ribbons used to eliminate gaps
  - Less Volume
  - Lower Mass (2 kg less)
  - Easier to integrate
  - 14 different tiles
  - More PMT's



- 2-Dimension Overlap
  - Solved gap problem
  - More mass
  - More volume
  - More difficult to integrate
  - 44 different tiles
  - 16 fewer PMT's

Mechanical Trade Studies (cont.)

Base Frame verses No Base Frame

- **Base Frame**
  - Provides support for electronics onboard the ACD
  - Easy to Integrate and Test
  - Provides good interface to LAT Grid
  - Eliminates CTE mismatch between ACD and LAT
  - Provides thermal joint between ACD and LAT
- **No Base Frame**
  - No place for electronics on ACD
  - Difficult, more costly and time consuming to Integrate and Test
  - Difficult interface to LAT Grid
  - CTE mismatch between ACD and LAT

Mechanical Ground Support Equipment

- **MGSE Required**
  - ACD Turnover/Assembly dolly
  - Shell Handling Dolly
  - Tile Shell Assembly lifting sling
  - Handling cases for the TDA's
  - Instrument Handling Dollies
    - 2 required, 1 for ETU and 1 for Flight
  - Instrument Lifting Slings
    - 2 required, 1 for ETU and 1 for Flight
  - Shipping Container
  - mass simulators for all of the TDA's and electronics boards
  - mass simulator of the ACD

Verification Matrix

		Hardware Description						Structural Mechanical												Thermal	
Item	Level of Assembly	S/N	Unit Type	Supplier	Qualification Status	Modal Survey (low level sine survey)	Static Loads	Sine Burst	Sine Vibration	Random Vibration	Acoustics	Proof Test @ 2X & NDE	Annual Proof Test @ 1.5X & NDE	Mechanical Function	Performance Testing (Optical)	Mass Properties	Micrometeorite Testing	No. of Thermal-Vacuum Cyc	No. of Thermal Cyc (Non Vac)	Thermal Balance	Remarks
ACD Subsystem	S		EM	GSFC	1	X-e		X-e	X-e	X-e	X-e			X		X		4-c		X-c	With EM electronics and TDA's
ACD Subsystem	S		F	GSFC	2	X-e		X-e	X-e	X-e	X-e			X		X		8			
Shell	C	1	EM	TBD	2		X-a									X					
Shell	C	2	F	TBD	2		X-a									X					
Tile Shell Assembly	SA		EM	TBD	1				X	X						X					
Tile Shell Assembly	SA		F	TBD	2				X	X						X					
TDA Tiedown	P		D	GSFC	1	X	X-b	X	X	X				X		X			8		Characterize flexures
TDA Tiedown	P		EM	GSFC	2		X-c									X					Test bonded Joint
TDA Tiedown	P		F	GSFC	3		X-c									X					Test bonded Joint
Tile Detector Assembly	C		D	TBD	2		X	X	X	X					X-d	X		4-d			Functional testing byCode 660
Tile Detector Assembly	C		EM	TBD	2										X-d	X					20 TDAs
Tile Detector Assembly	C		F	TBD	3										X-d	X					117 Flight TDAs (28 flight spares)
PMT/Fiber Connector	C		D	TBD	2		X	X	X	X				X	X-d	X			8-d		
PMT/Fiber Connector	C		PT	TBD	2		X	X	X	X				X	X-d	X			4-d		
PMT/Fiber Connector	C		F	TBD	3										X-d	X					
WSF/Clear Fiber Connector	C		D	TBD	2		X	X	X	X				X	X-d	X			8-d		
WSF/Clear Fiber Connector	C		PT	TBD	2		X	X	X	X				X	X-d	X			4-d		
WSF/Clear Fiber Connector	C		F	TBD	3										X-d	X					
Base Frame	C	1	EM	GSFC	1		X									X					
Base Frame	C	2	F	GSFC	3		X									X					
Base Electronics Assembly	SA		EM	GSFC	2	X-e-c	X-e-c	X-e-c	X-e-c	X-e-c						X					Qualification Level
Base Electronics Assembly	SA		F	GSFC	2											X					
Shield & Thermal Blanket	C		D	JSC	2												X	1			Characterize thermal performance
Shield & Thermal Blanket	C		EM	JSC	2											X					Similarity to development model
Shield & Thermal Blanket	C		F	JSC	3											X					Similarity to development model
Turnover/Assembly Dolly	G	1		TBD	4							X									
Shell Handling GSE	G	1		TBD	4							X									
Base Frame Handling Dolly	G	1		TBD	4							X									
Base Frame Handling Dolly	G	2		TBD	4							X									
Shipping Container Lifting Sling	G	1		TBD	4							X	X								
Lifting Sling	G	1		TBD	4							X	X								
Lifting Sling	G	2		TBD	4							X	X								

LEGEND:

LEVEL OF ASSEMBLY	
S	Subsystem
SA	Subassembly
C	Component
P	Part
G	Ground Support Eqp

UNIT TYPE	
D	Development Model
EM	Engineering Model
PT	Prototype
F	Flight

QUALIFICATION STATUS	
1	Complete qual required
2	Partial qual required (see remarks)
3	Otherwise qualified (see remarks)
4	Proof test @ 2 x allowable load

NOTES:

a. Composite structure, see Sec.4.3
b. Test-to-failure
c. May be tested at next higher assembly
d. Test for light yield and repeatability
e. Test with mass models

Issues and Concerns

- Mass needs to be reallocated
  - Allocation is based on old design
  - Mass of electronics is divided between ACD and LAT
- Interfaces to LAT have to be finalized
- Integration area for the ACD at SLAC - Limited crane hook height (10 feet)
- Gap between lower tile and trackers needs science assessment
- Loads transmitted to the ACD from the LAT Grid
  - Coupled loads currently being performed will address this concern
- Fiber routing
  - Particularly difficult on Y-sides where fibers have to cross
  - Bottom tile routing will be difficult due to limited space

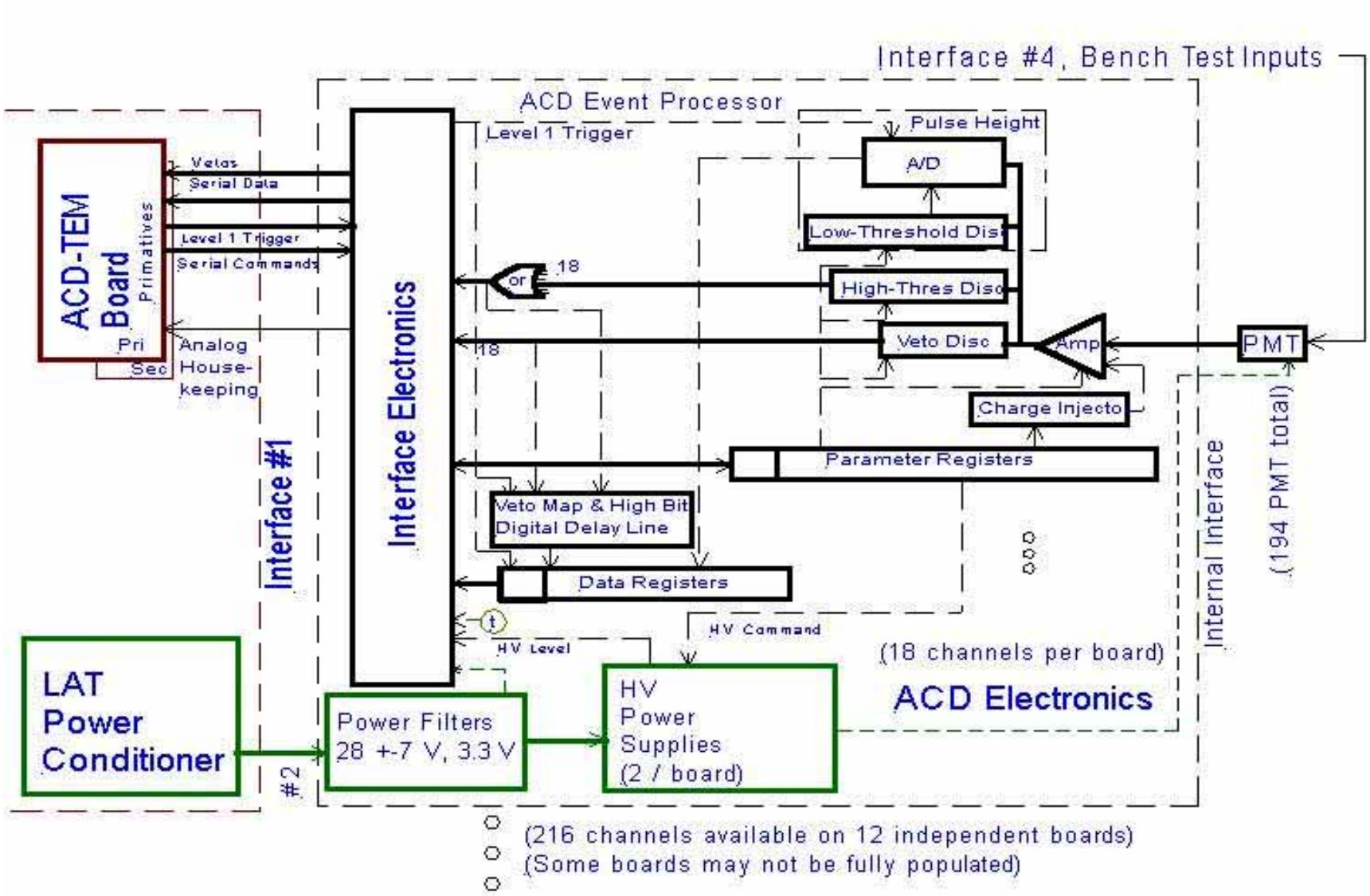
Conclusion

- ACD mass problem has to be resolved
- ACD Volume constraints are tight, but achievable
- Prepared to address all design issues and continue with the design of the ACD

ACD ELECTRONICS
David Sheppard

Last Updated: 7/27/01 09:25

Block Diagram: Electronics



ACD Level IV Electrical Requirements / Specifications

Req't #	Title	Level IV, Electronic Design Response	Verif. Method
5.2	Detection of Charged Particles	Design of Event Processor front end.	T
5.3	Adjustable Threshold on Detecting Charged Particle	Digitally set in Veto Discriminator.	T
5.4	Detection Efficiency	Design of tiles, fibers, PMT, and Event Processor front end.	T, A
5.5	Instrument Coverage	Design of tiles, tapes, and supports.	I
5.6	Mean Thickness	Design of tiles and supports	A
5.7	False VETO due to Backsplash	Design of Event Processor front end.	A
5.8	False VETO due to Electrical Noise	Design of Event Processor front end and Veto Discriminator.	A
5.9	High-Threshold Detection	Design of High Threshold Detector.	A
5.10	Adjustable High-Threshold	Design of High Threshold Detector and Parameter Regsister.	A
5.11.1	Fast VETO Signal	Design of Event Processor front end, Veto Discriminator, and output driver.	D
5.11.2	Fast VETO Signal Latency	Design of Event Processor front end, Veto Discriminator, and output driver.	T
5.11.3	Logic VETO Signal	Design of Veto Discriminator, and output driver.	D
5.11.4	Logic VETO Signal Latency	Design of Veto Discriminator, and output driver.	T
5.11.5	Logic VETO Signal Timing	Design of Veto Discriminator, and output driver.	T
5.11.6	Fast VETO Signal Width	Design of Veto Discriminator, and output driver.	T

T- Test A - Analysis I - Inspection D - Design

ACD Level IV Electrical Requirements / Specifications

Req't #	Title	Level IV, Electronic Design Response	Verif. Method
5.11.7	Fast VETO Recovery Time for Large Signals	Design of Veto Discriminator, and output driver.	D
5.11.8	High-Threshold Signal Latency	Design of High-Threshold.	A
5.11.9	ACD Trigger Primitives	Interface with ACD-TEM computer	T
5.12	ACD Performance Monitoring	Design of Pulse Height circuit, charge injector and parameter registers.	D
5.12.1	Low-Threshold Signal	Design of Pulse Height circuit.	D
5.12.2	Low-Threshold Adjustability	Design of Low-Threshold discriminator and parameter registers.	D
5.12.3	Signal Content	Design of Pulse Height circuit.	D
5.12.4	Pulse Digitization	Design of Pulse Height circuit.	D
5.12.5	Pulse Height Measurement Latency	Design of Pulse Height circuit.	D
5.13	Reliability - Electronics	Design of a circuits, design of HV power supply, selection of components, and selection of chip technology	A
5.14	Reliability - Tiles	Design of Tiles, blankets, and fibers.	A
5.15	Reliability - System	Design of all components, selection of parts and materials.	A
5.16.1	Detector On/Off Commands	Design of Parameter Registers and command interface	T
5.16.2	Detector Gain Commands	Design of Parameter Registers and command interface	T

T- Test A - Analysis I - Inspection D - Design

ACD Level IV Electrical Requirements / Specifications

Req't #	Title	Level IV, Electronic Design Response	Verif. Method
5.16.3	Electronics On/Off Commands	Design of Parameter Registers and command interface	T, D
5.16.4	VETO Threshold Commands	Design of Parameter Registers and command interface	T, D
5.16.5	High-Threshold Commands	Design of Parameter Registers and command interface	T, D
5.16.6	ACD Monitoring Commands	Design of Parameter Registers and command interface	T, A
5.16.7	Low-Gain Mode Commands	Design of Parameter Registers and command interface	T
5.17	Power Consumption	Design of electronic circuits and HV power supply	D, A
5.18	Mass	Overall design	D
5.19	Center of Gravity	Overall design	T
5.20	Environmental	Design of blanket and footprint	T, D, A
5.21	Physical Size	Overall design	D
5.22.1	Thermal Blanket/ Micrometeoroid Shield Areal Mass Density	Design of shield / blanket	D, A
5.22.2	Micrometeoroid Protection	Design of shield / blanket	A
5.22.3	Thermal Control	Design of blanket, electronic structure, and foot print.	A
5.23	Performance Life	Overall design	A
5.24	Operation in High Rate Conditions	Design of Parameter Registers, command interface, D/A converter, and HV supply.	A
5.24.1	Notification of Mode Change	Design of Data Registers and command interface	D, T
5.24.2	Tile Linear Response	Design of tiles, fibers, PMT, and Event Processor front end.	D, T

T- Test A - Analysis I - Inspection D - Design

ACD Subsystem Electrical Trade Studies

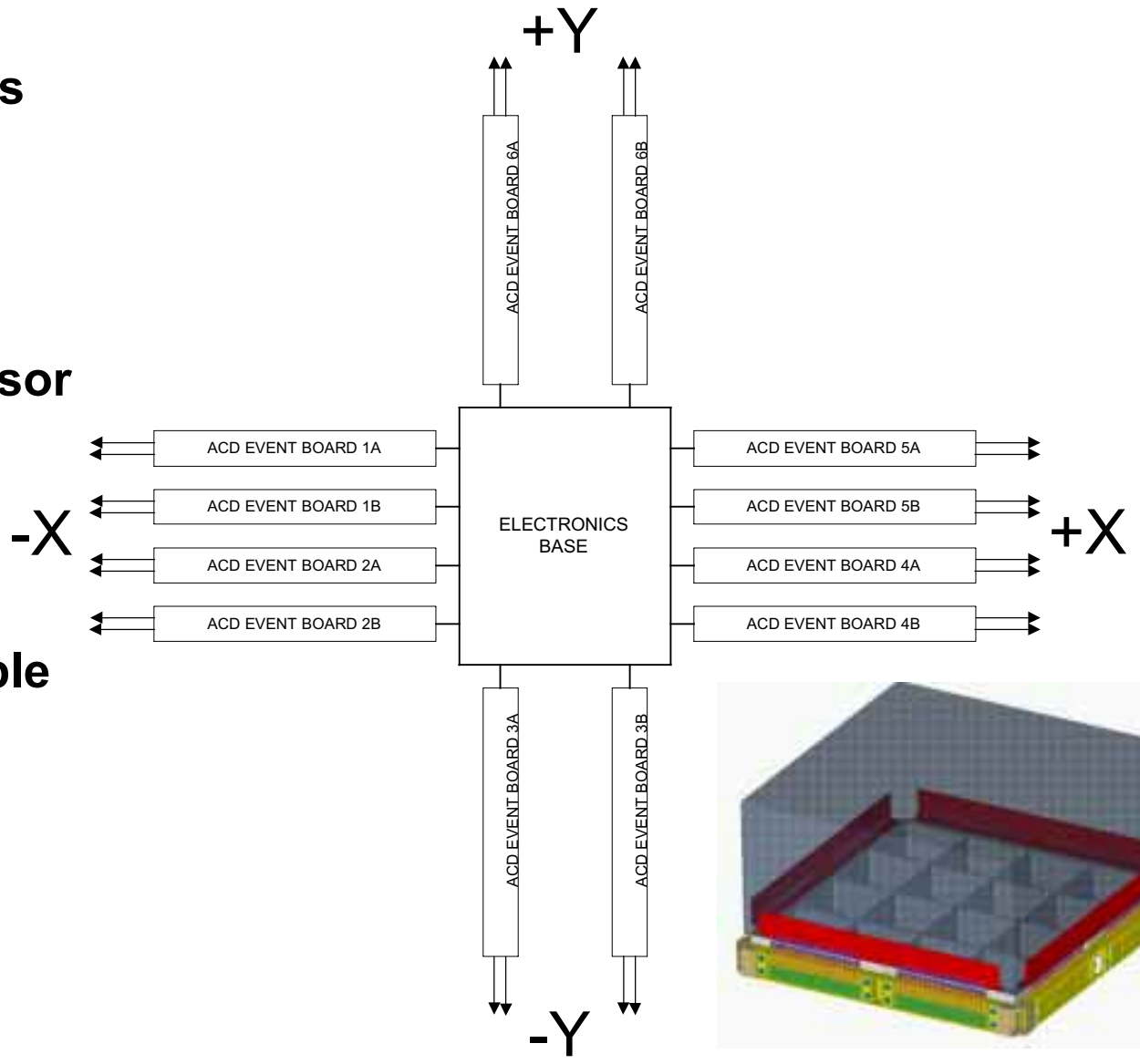
- Requirement to support 194 analog signal channels (reduced from the original 290 channels)
- Requirement to limit number of connections to the ACD-TEM to 16 (increased from previously required 2)
- Requirement to minimize overall electronics cost (and therefore) the number of Event Processor boards
- Requirement to accomodate an asymmetrical routing of fibers to ACD base due to the top tiles and ribbons
- Result of trade study is 12 boards, each with 18 analog channels and dual cables. (12 x 18 = 216 channels available)

ACD Electronics System Design

18 PMT Channels per Event Processor

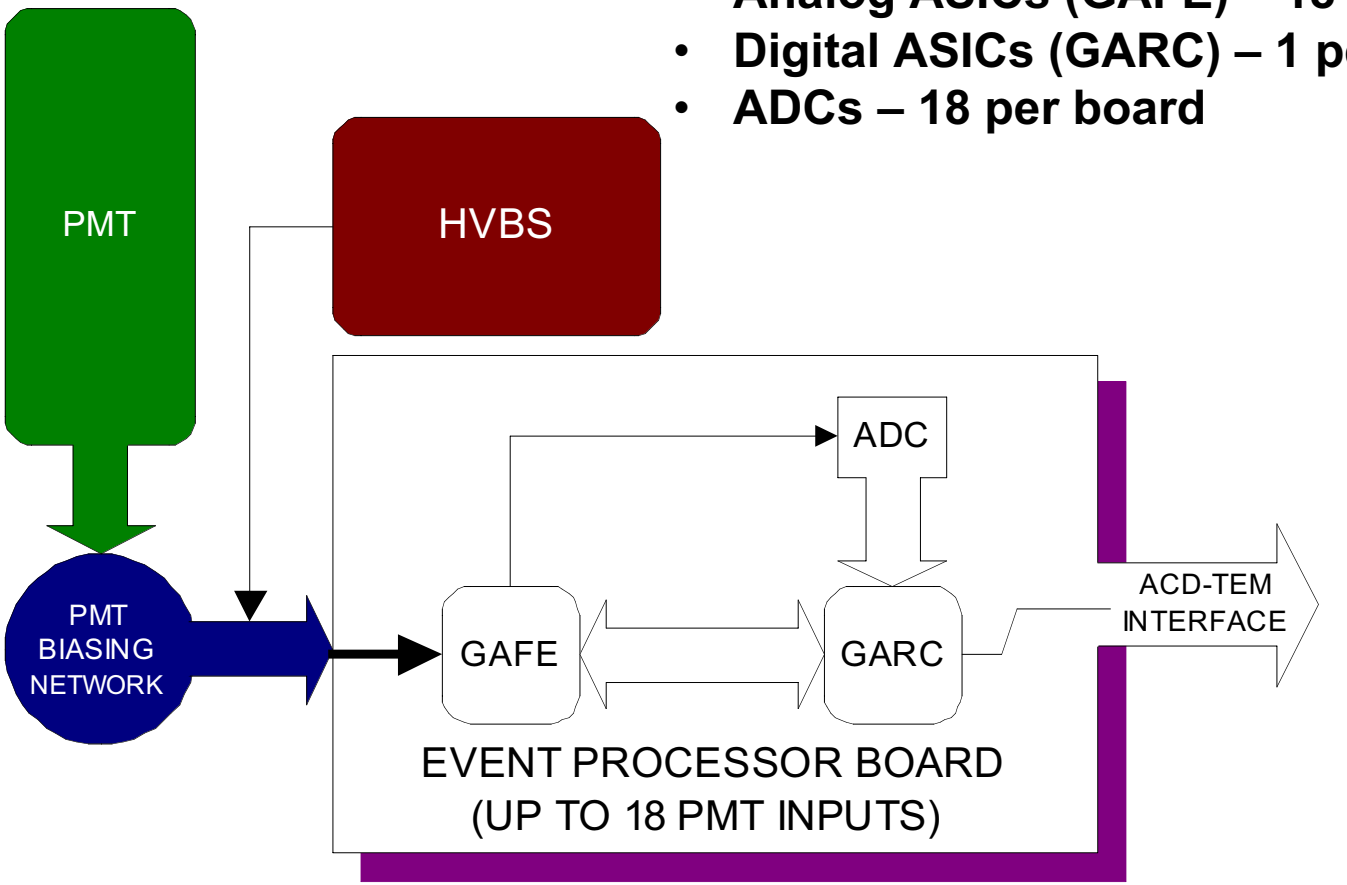
12 Event Processor Boards per ACD

216 Total PMT channels available



ACD Electronics System Assemblies

- Photomultiplier Biasing Resistor/Capacitor Networks
- High Voltage Bias Supplies (2 per board)
- Event Processor Boards
  - Analog ASICs (GAFE) – 18 per board
  - Digital ASICs (GARC) – 1 per board
  - ADCs – 18 per board



ACD Electronics- Heritage and Design Baseline

- Where applicable, parts are selected from the NASA GSFC approved parts list. Parts selected from NPSL have flight heritage and established reliability
- ASIC fabrication process based on CAL and TKR experience and qualification. The present baseline is the HP (Agilent) 0.5 μm process
- ADC is a commercial part, identical to that used on CAL and TKR (qualified parts for flight use will be provided to GSFC by SLAC)

Electronics Modeling, Test, and Simulation Status

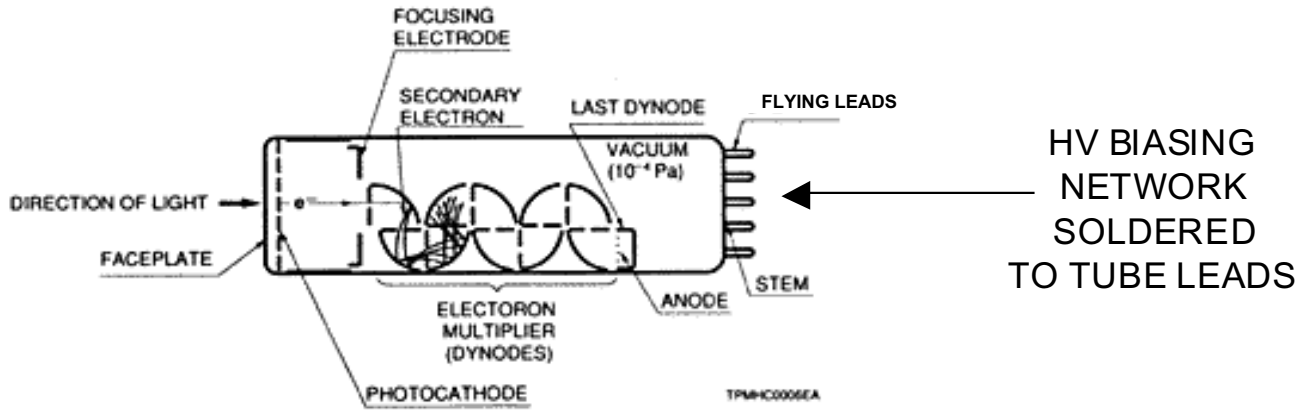
- **Analog ASIC** preliminary version has been fabricated and tested. Conceptual design and process has changed. SPICE simulations continue.
- **Digital ASIC** is in conceptual design phase.
- **ADC** choice will follow TKR and CAL.
- **HVBS** is in the conceptual design phase. Some breadboarding has been performed, including planar transformer verification.
- **PMT Bias Resistor Network** is in the conceptual design phase.

ACD Electronics Component Design Verification

- **Analog ASICs to be tested & screened (selected for flight) with a separate bench-top test station.**
- **Digital ASICs to be verified in a similar manner with a separate test station**
- **Event Processor boards to be tested on the bench prior to integration with ACD**
- **High Voltage Bias Supplies will be setup and tested on the bench; environmental test completed at LHEA**
- **Biasing Resistor Networks for phototubes screened by flight-approved vendor**

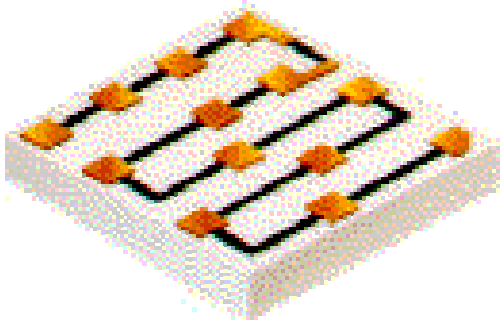
Phototube Biasing Resistor Network Design

- **The photomultiplier tube baseline is the Hammatsu R4443 (a ruggedized version of the R647)**

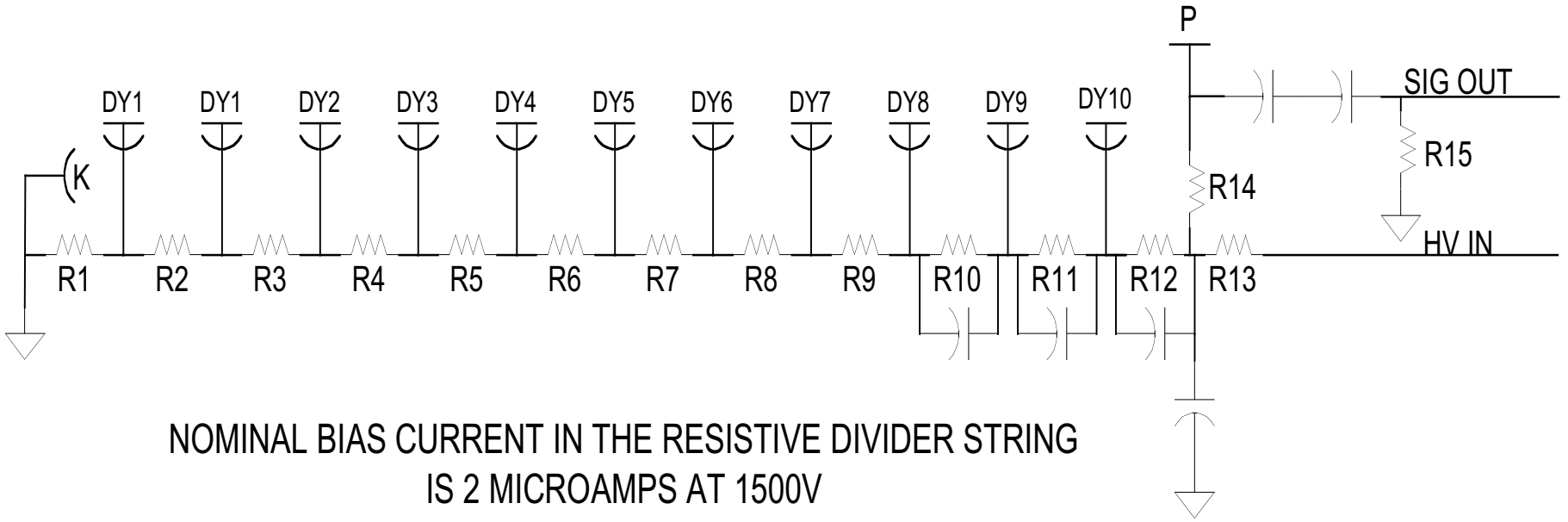


- **The baseline dynode string biasing current is 2 μA at 1500V**

- **A conceptual design is being studied by a flight-approved vendor (SOA). This design consists of printing the thick film resistors on two or three cylindrical alumina disks that solder to the phototube leads (through-hole). Bypass capacitors will also be located on these disks.**



ACD Electronics Phototube Biasing Circuitry

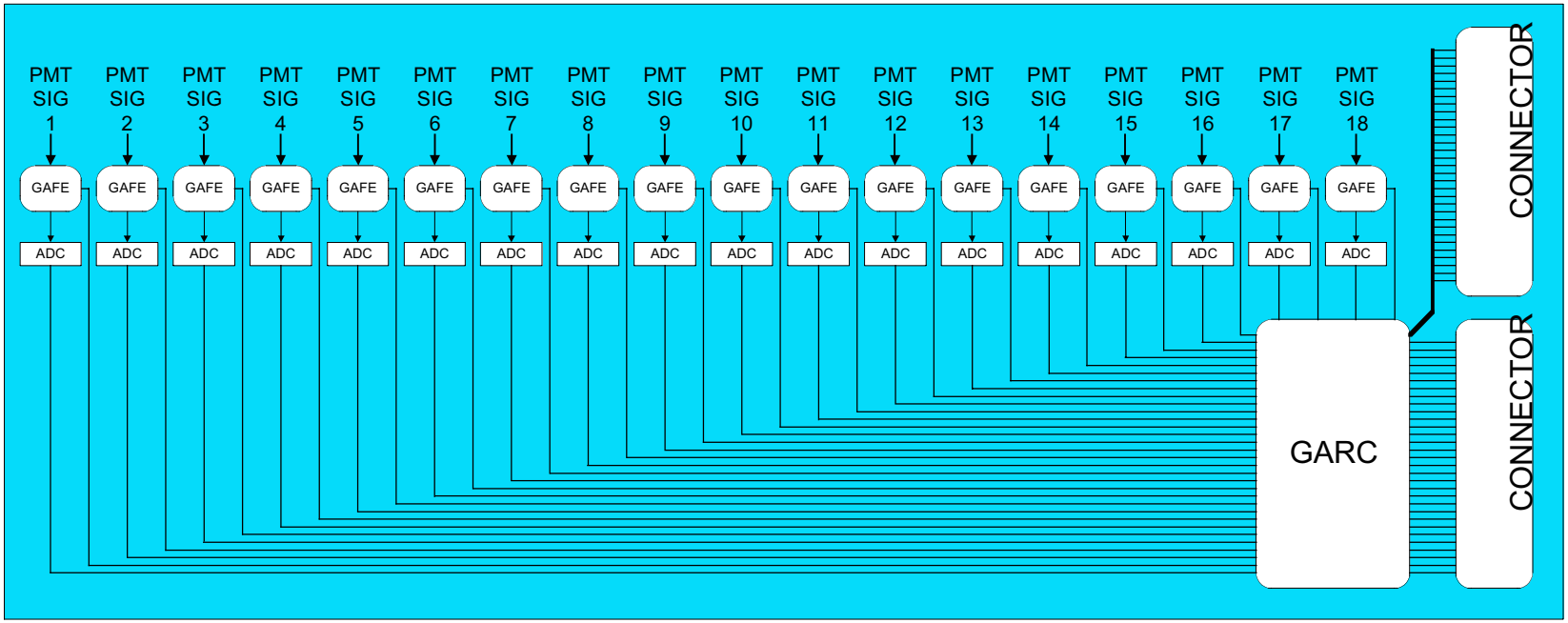


NOMINAL BIAS CURRENT IN THE RESISTIVE DIVIDER STRING
IS 2 MICROAMPS AT 1500V

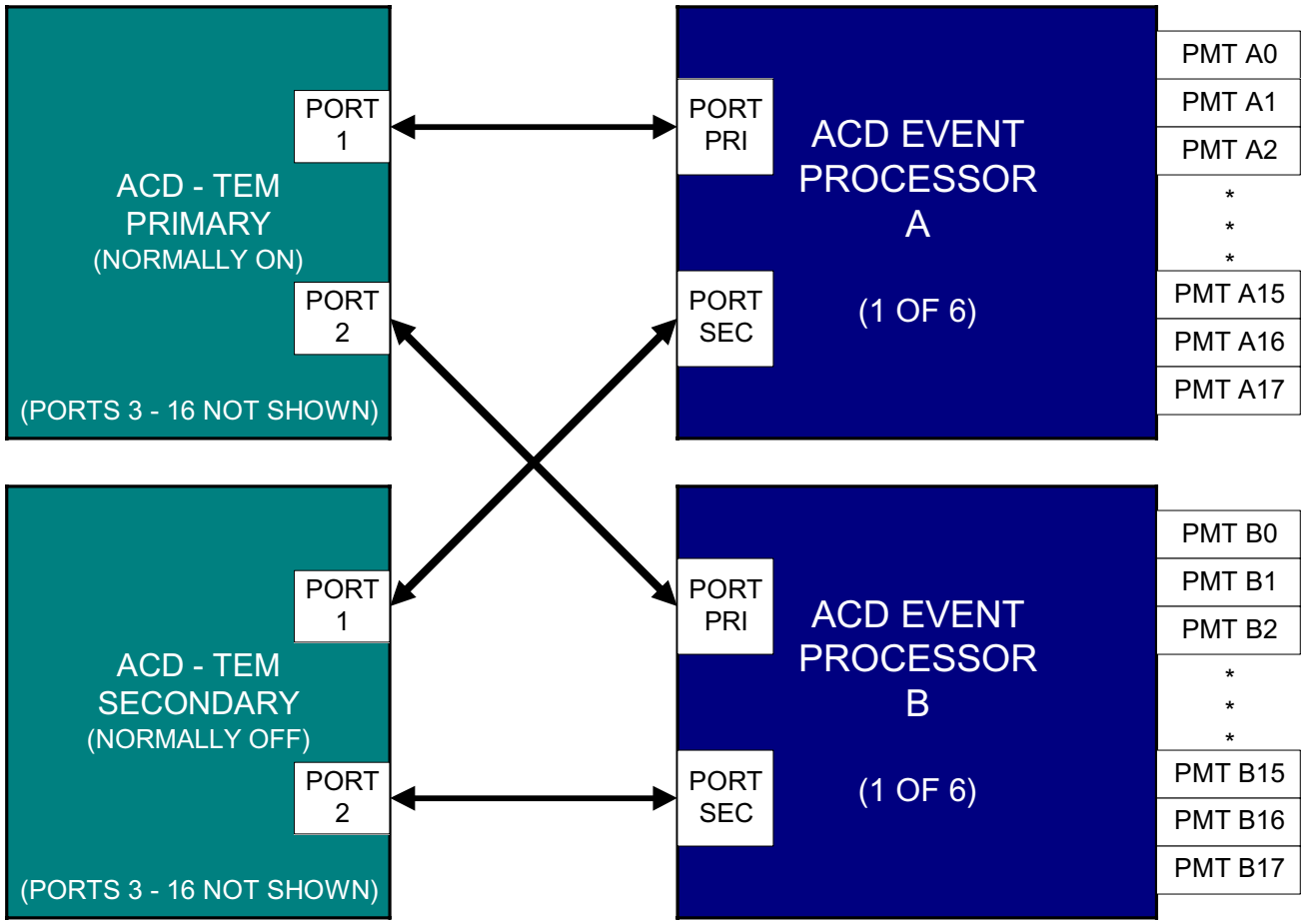
PMT BIASING CIRCUITRY

ACD Electronics Event Processor Design

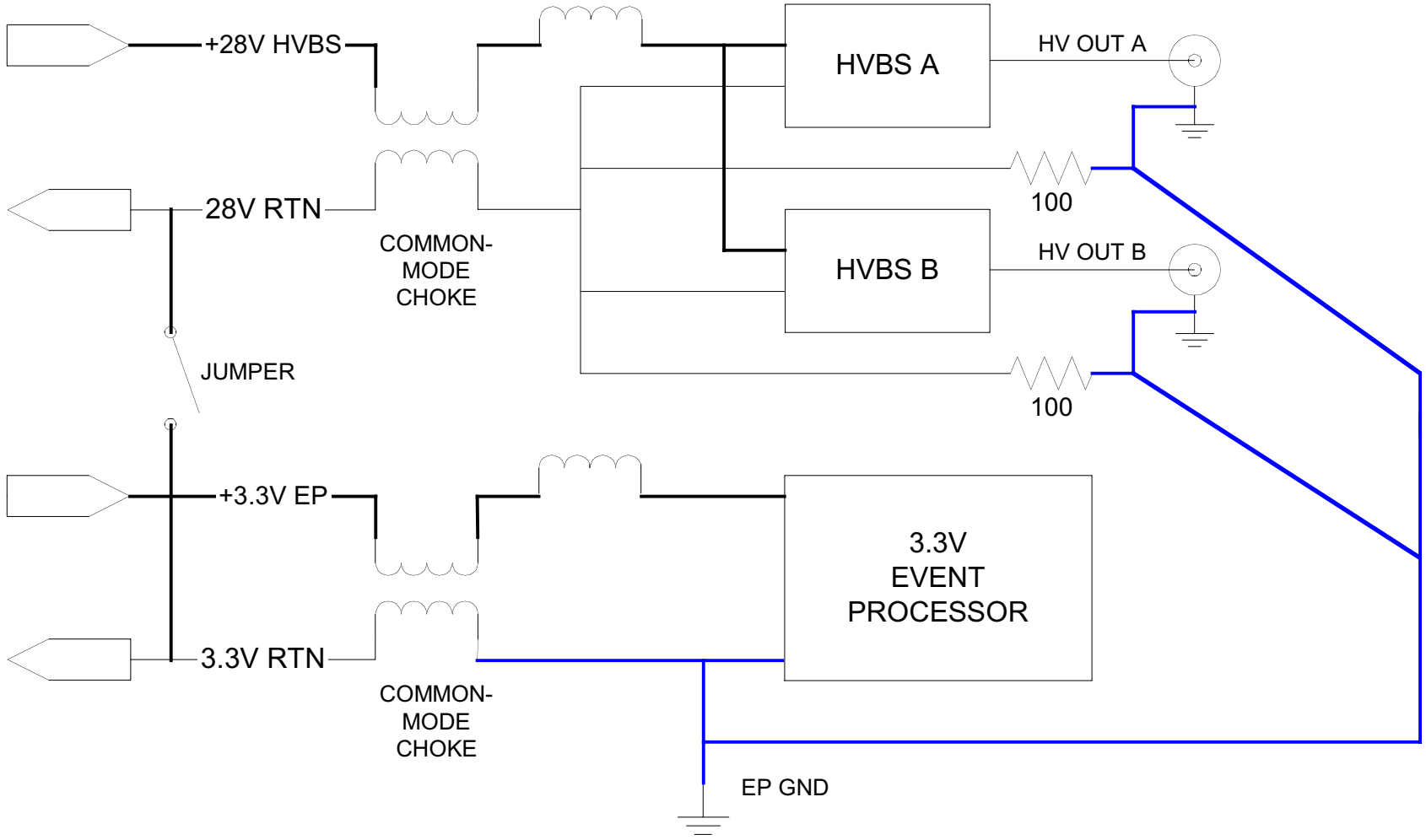
- The Event Processor will have
  - Two interface connectors – one for TEM Primary, one for TEM Secondary
  - 18 phototube inputs
  - 18 analog ASICs (GAFE)
  - 18 analog-to-digital converters
  - 1 digital ASIC (GARC)
  - 2 parallel high voltage bias supplies (mounted off board)



ACD Electronics Cross-Strapping



ACD Electronics Grounding

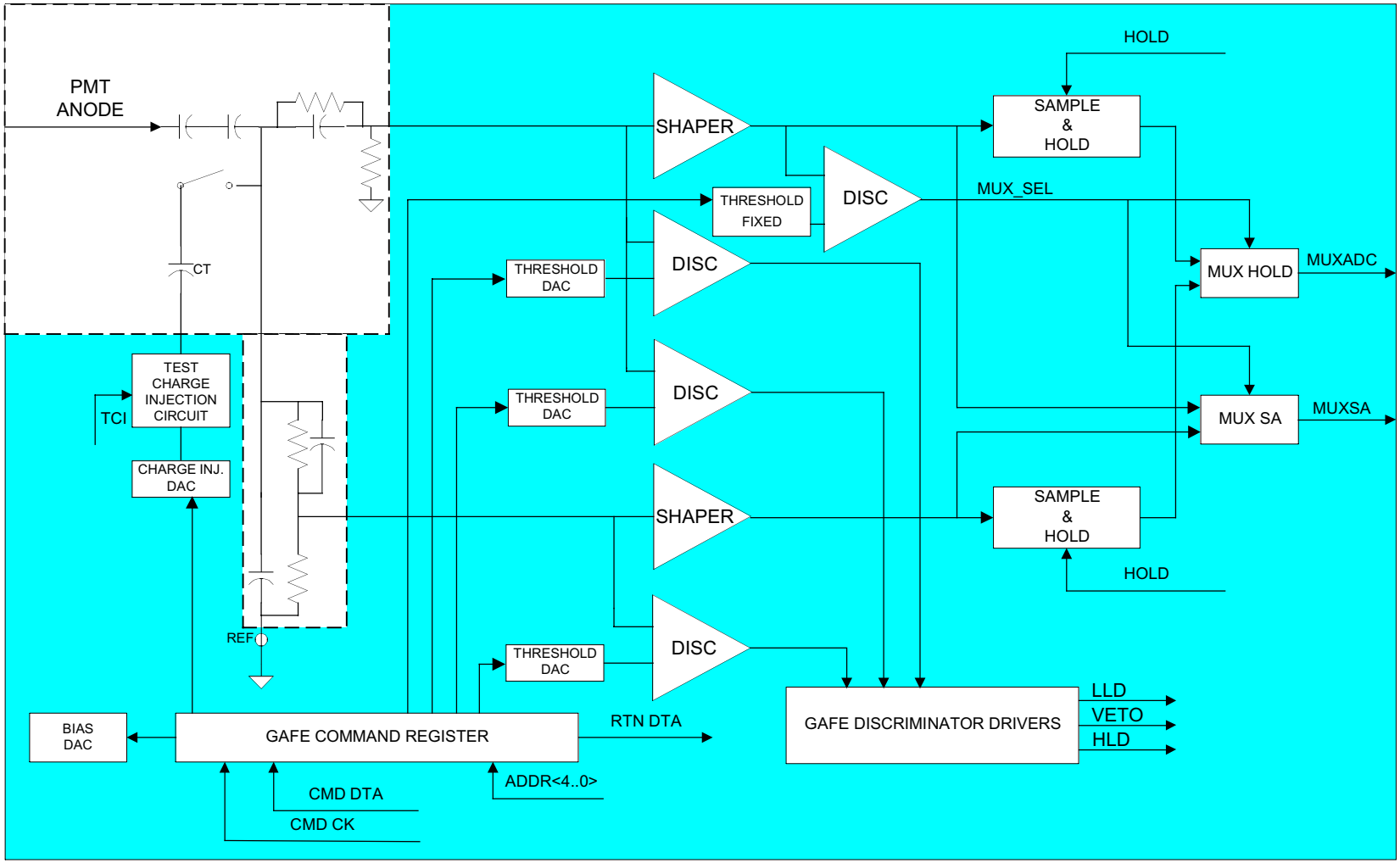


EVENT PROCESSOR GROUNDING DIAGRAM

ACD Analog ASIC (GAFE) Design

- The Analog ASIC (GAFE) will have:
  - An AC-coupled input from the PMT anode
  - Three discriminators:
    - a low level discriminator (LLD) to be used for PHA suppression
    - a VETO discriminator to be used for ACD anti-coincidence
    - a high level discriminator (HLD) to be used to identify heavy nuclei
  - Two shaping amplifiers and hold circuits for coarse spectroscopy
    - Low energy range (~ 0.2 – 20 MIP range)
    - High energy range (~ 10 – 1000 MIP range) (self calibrating)
  - Test Charge Injection circuit to allow for characterization and test of the electronics system

ACD Analog ASIC Conceptual Block Diagram

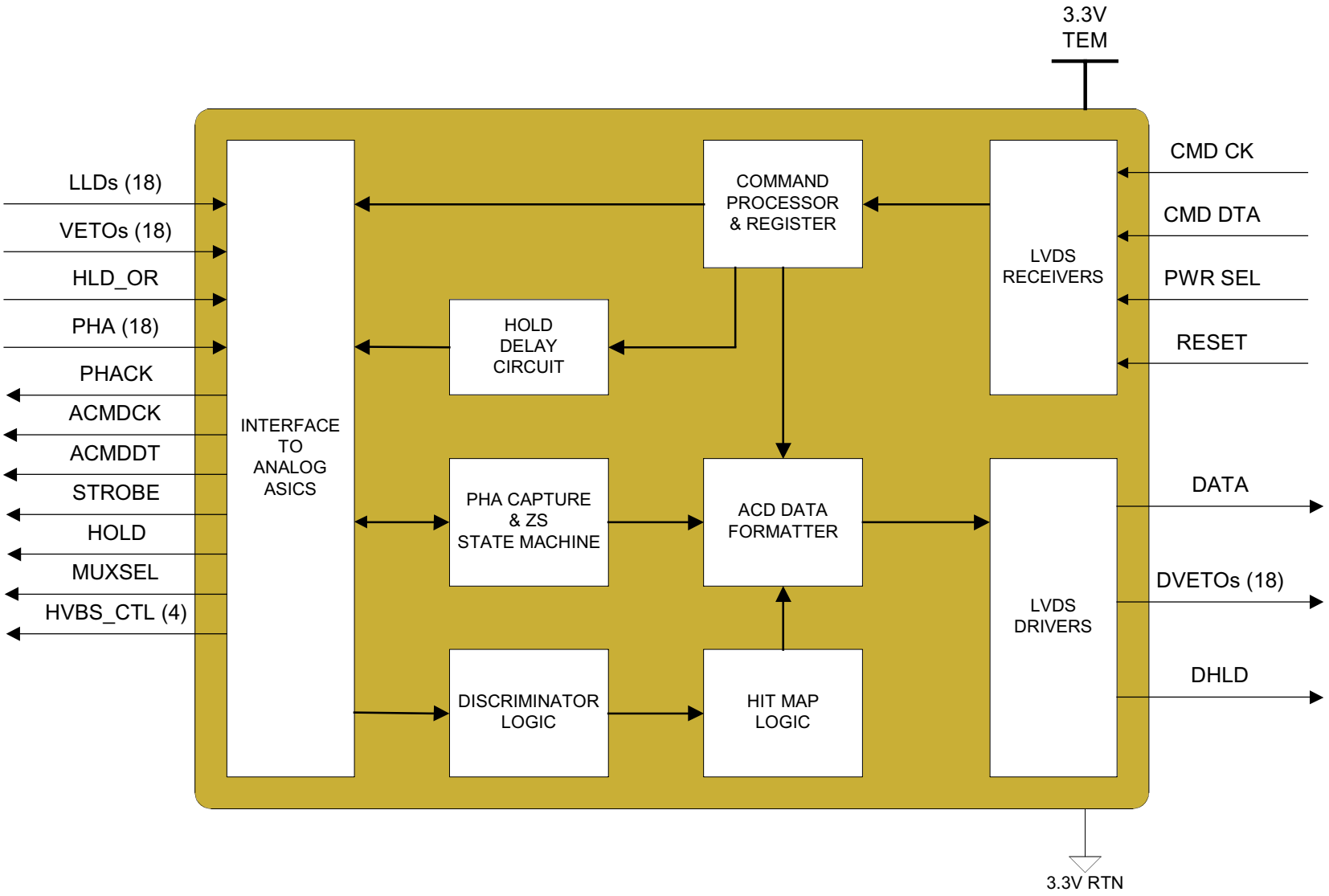


(CURRENT - TO - VOLTAGE CONVERSION NOT DETAILED; RESISTORS & CAPACITORS EXTERNAL)

ACD Digital ASIC (GARC) Design

- The Digital ASIC (GARC) will have
  - A command processor to receive configuration from the ACD-TEM
  - A telemetry formatter to distribute data to the ACD-TEM
  - A PHA state machine to control the event processor ADCs and provide the zero-suppression function
  - LVDS interfaces to the TEM for digital signals
  - Low power current-mode interfaces for digital signals connected to the analog ASIC
  - A hit map register for the VETO and HLD discriminators (including a commandable delay)
  - A commandable delay for the analog HOLD signal

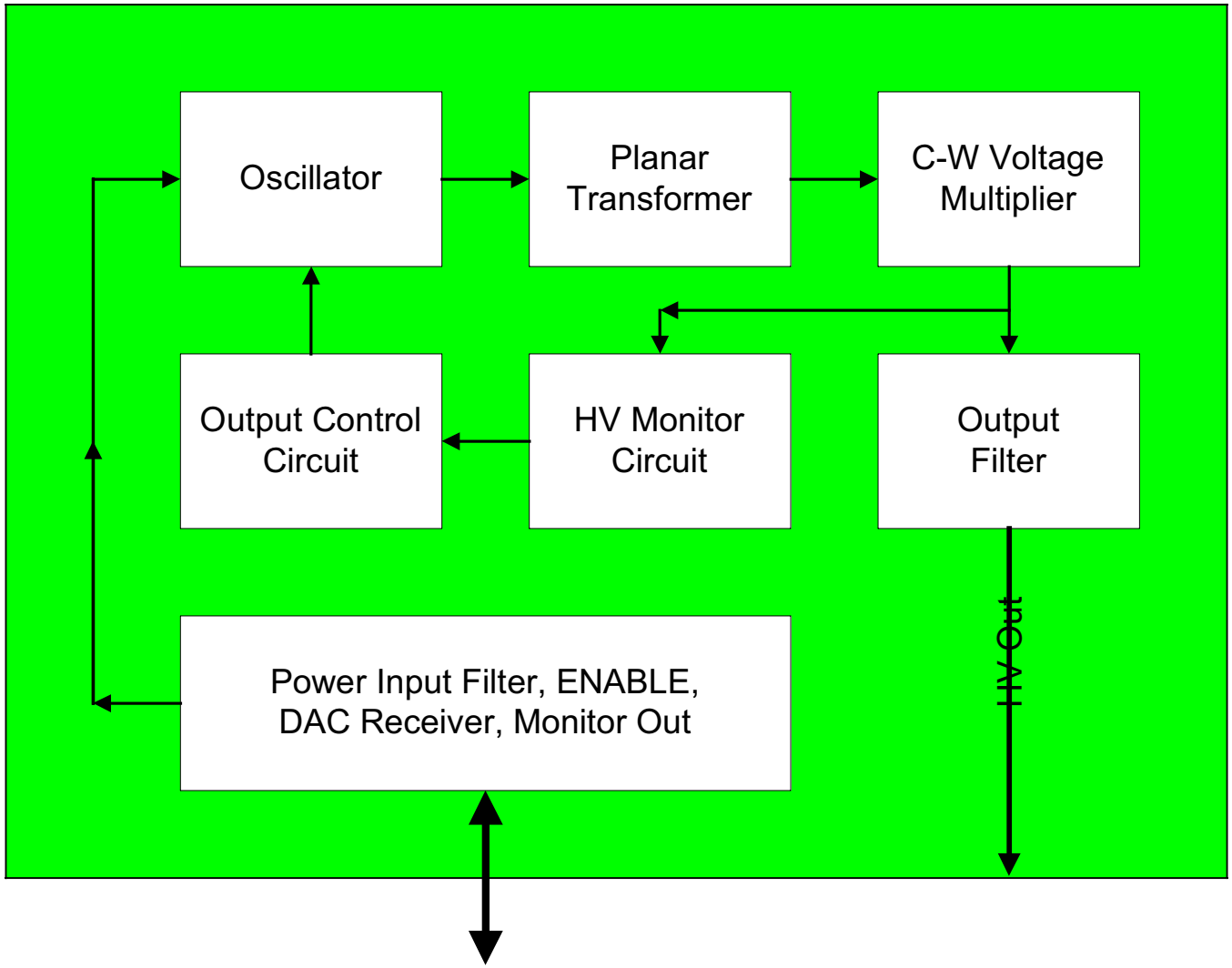
ACD Electronics Digital ASIC (GARC) Design



ACD Electronics High Voltage Bias Supply Design

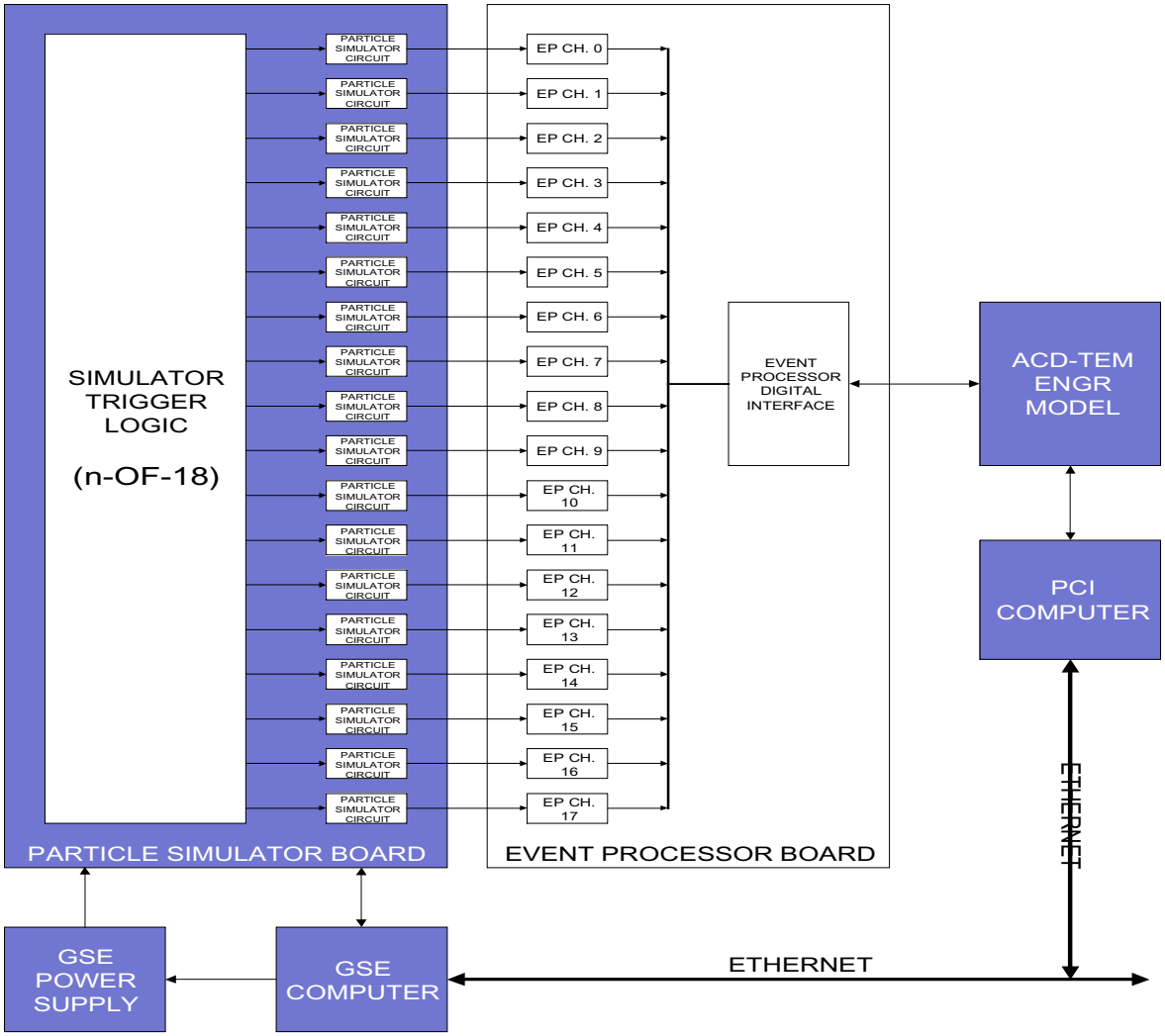
- The High Voltage Bias Supply (HVBS) will have:
  - Input voltage of +28V supplied via the TEM interface
  - Adjustable output voltage of 0 to 1600V DC, controllable via DAC command
  - Commandable enable/disable
  - Diode ORing to provide capability for two supplies in parallel
  - A maximum output current of 80 microamps

ACD HV Bias Supply Concept



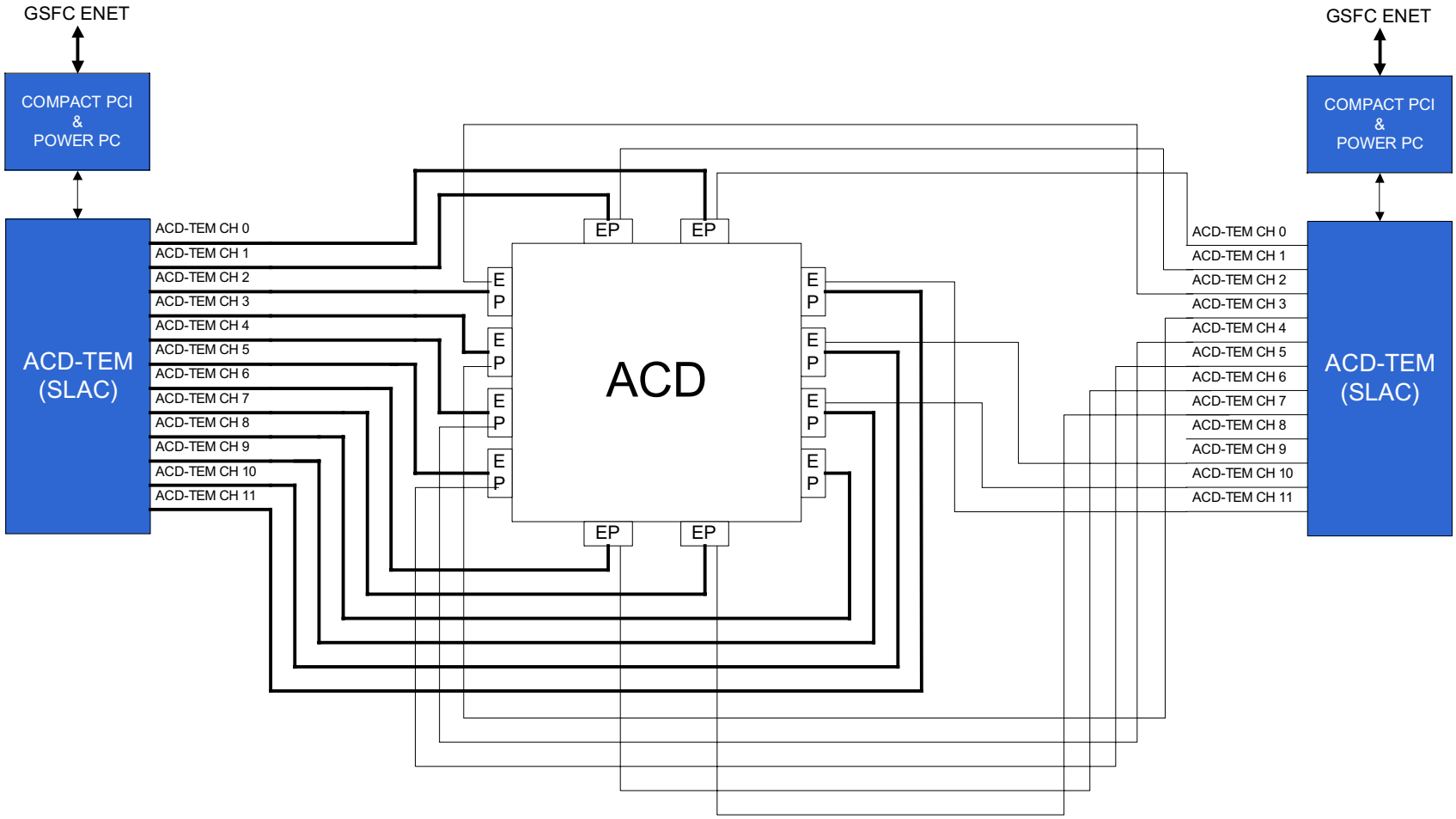
ACD Electrical GSE for Event Processor Test

Event Processor test setup includes a phototube simulator for each event input, programmable via software interface. Each Event Processor interfaces with an engineering model ACD-TEM for ground test.

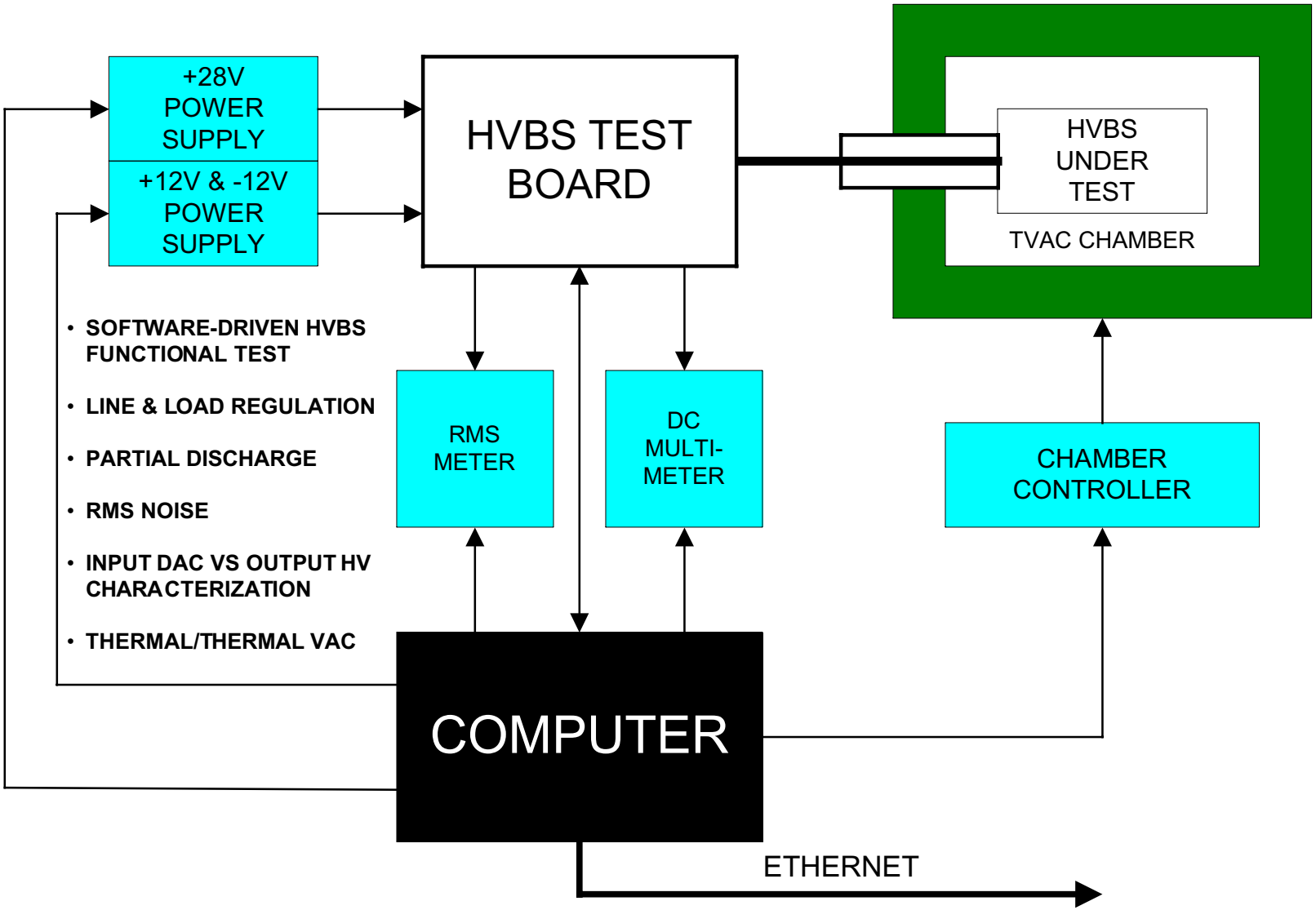


Ground/Flight Setup for Integrated ACD and both ACD-TEMs

Complete flight setup requires 12 EP boards, two ACD-TEMs, and 24 cables



ACD Electrical GSE - High Voltage Bias Supply Test Fixture



ACD – TEM Electrical Interface Summary

CABLES

- 24 Cables Total
- 68 wires in each cable
- Each of 12 ACD Event Boards interface to 2 cables (TEM P and TEM S)
- MIL-C-38999 Series III connectors at the ACD end.
- S-311-P-407 High Density D-Subminiture connectors at the TEM end.
- 26 gauge wire for signals
- 24 gauge wire for power
- Twisted pairs for all differential signals.
- Twist 3.3 volt power and returns.
- Twist 28 volt power and returns.
- single shield braid.
- Polyester overwrap.

SIGNALS

- 20 MHz Clock from TEM
- Command from TEM
- Reset from TEM
- Power Select from TEM
- Data to TEM
- VETOs to TEM (18)
- CNO to TEM
- High Voltage Monitors to TEM (2)
- Thermistor to TEM(1)
- Power from TEM, 3.3 and 28 volts

ACD – TEM Electrical Interface Summary (continued)

SIGNAL CHARACTERISTICS

- LVDS for digital signals
- Pseudo differential analog for HV Monitors
  - 0-2.5 volt signal on one line
  - Ground on other line
  - 10K source impedance both lines

POWER SWITCHING

- ACD switches between primary and secondary power based on PWRSEL input

INTERFACE DOCUMENTATION

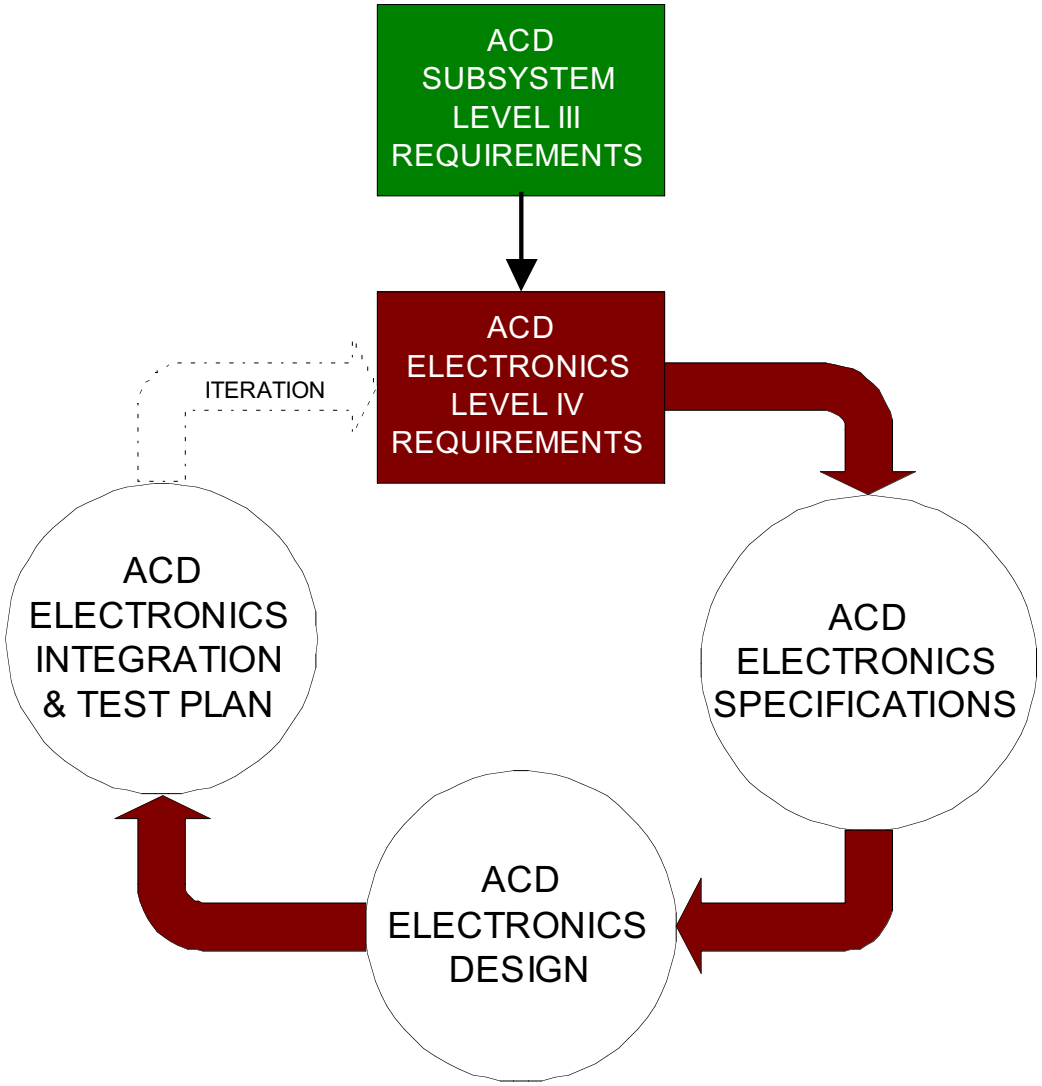
- ACD – TEM Interface Information sheets have been written
- Details being discussed
- Formal LAT Document to follow

COMMAND AND DATA FORMAT

- Preliminary format written
- Discussion and iterations begun

Issues and Concerns with the Electronics

- We have had a less than structured design process, as compared to the diagram at right.
- Requirements for the electronics at Level IV have been changing over the past one year (first draft available July 2001)
- There are a lot of cables in this design, making the integration and test effort more complex (24 cables x 65 conductors > 1500 wires)



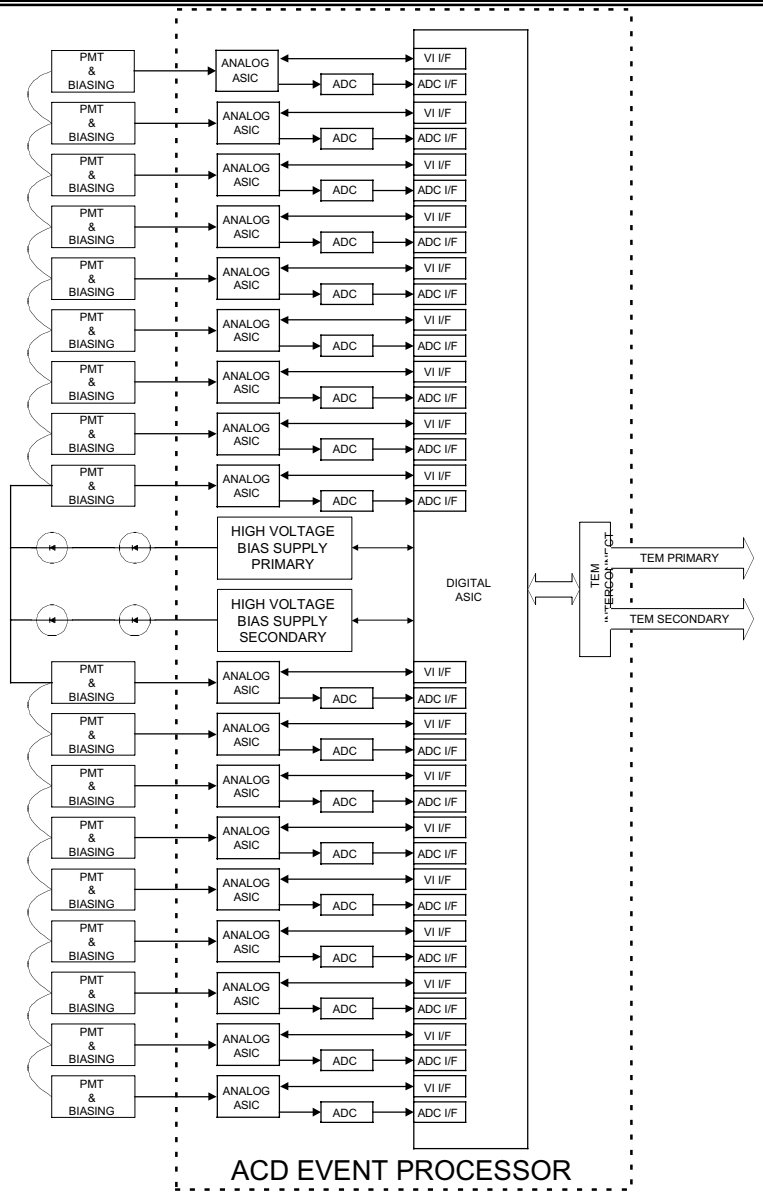
ACD ELECTRONICS SLIDES BACKUPS

ACD Electronics Reliability and Redundancy

- The requirements for the ACD electronics calculated reliability have been evolving over the past months and are still being refined.
- The ACD electronics reliability requirements are needed to accurately determine the requirement for redundancy.
- The present design reflects a trade between reliability versus cost and schedule.

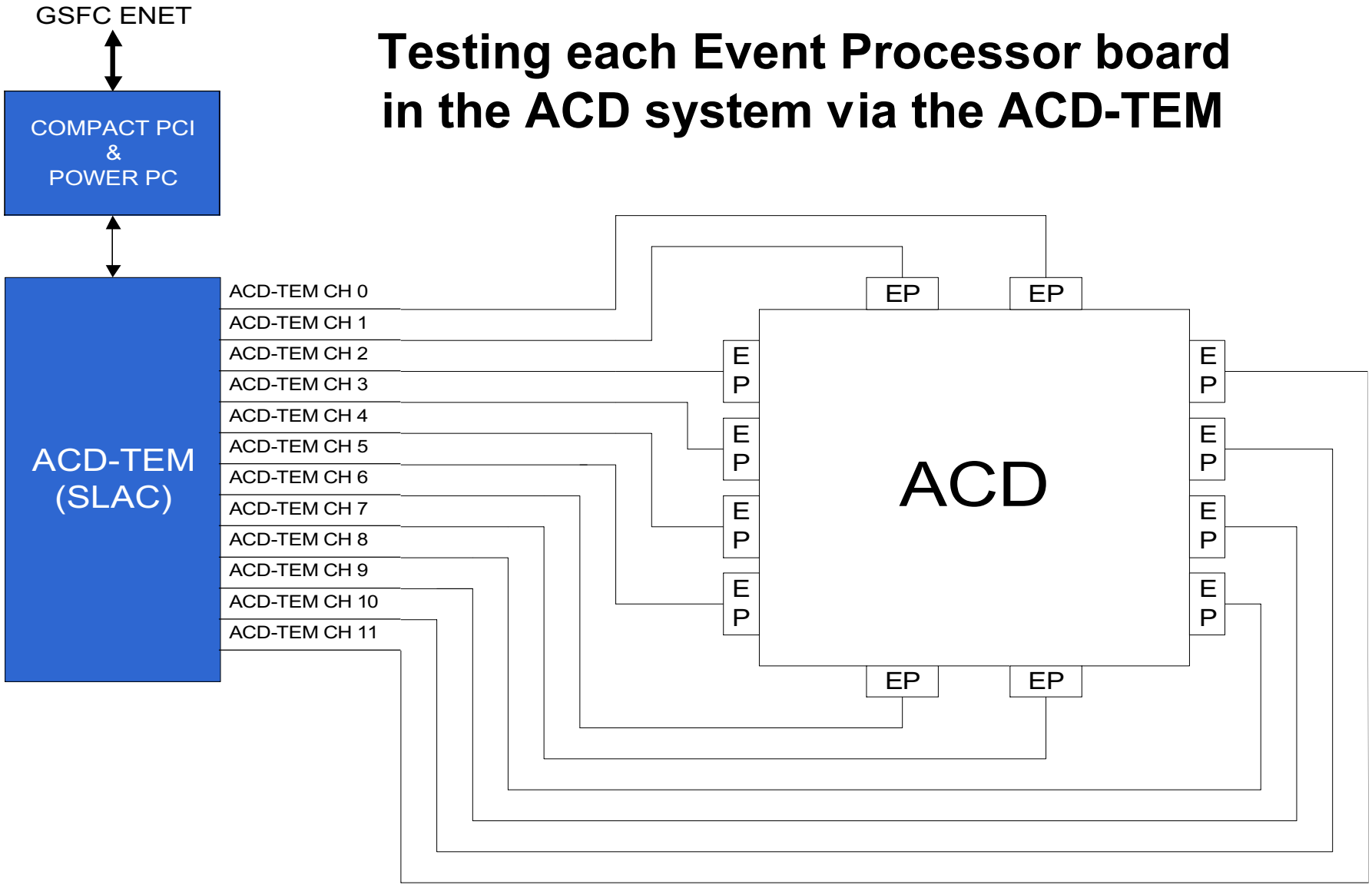
ACD Electronics Design

Event Processor Block Diagram

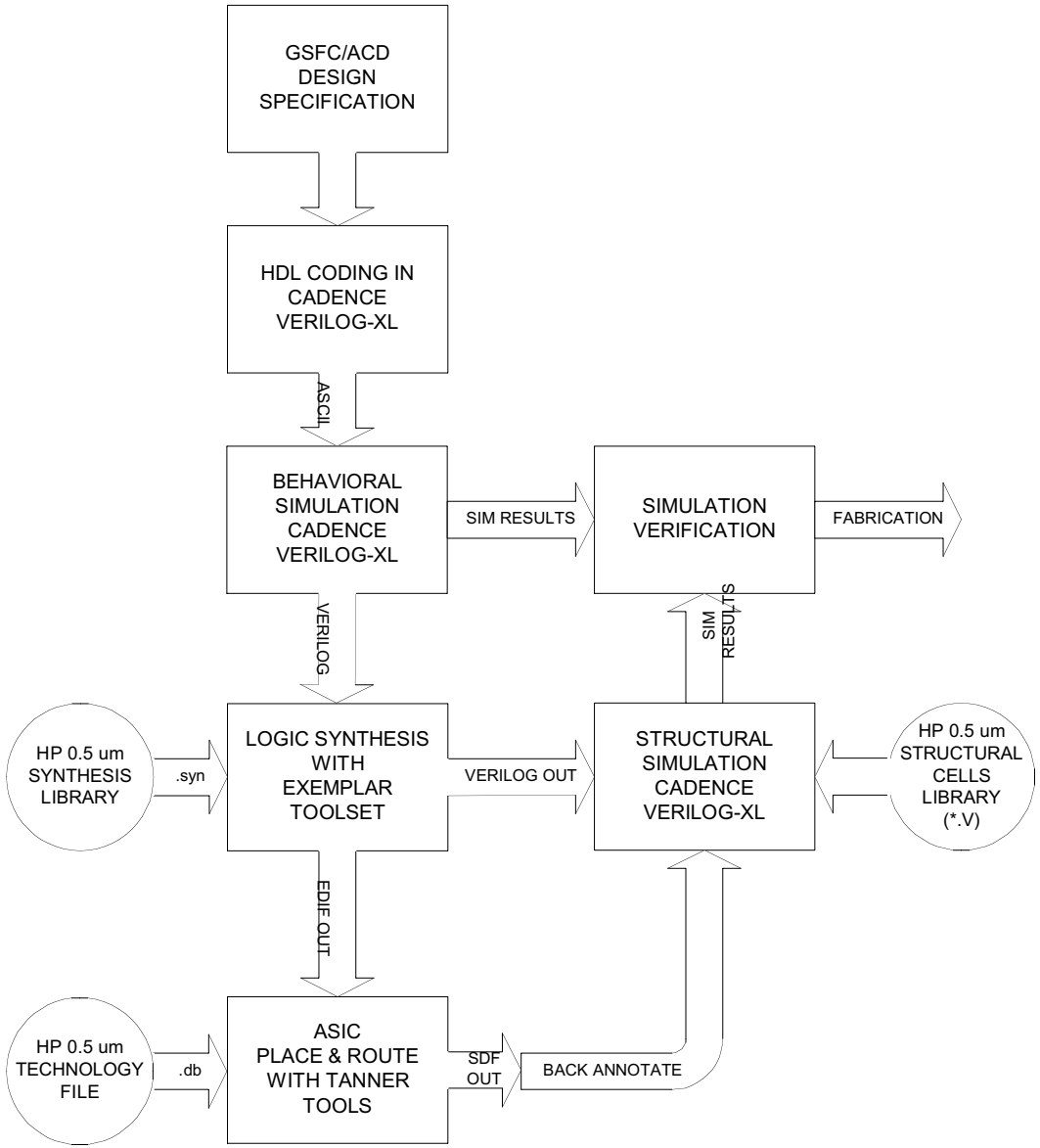


Ground Test Setup for Integrated ACD and ACD-TEM

Testing each Event Processor board in the ACD system via the ACD-TEM



Digital ASIC Design Process



ACD Electronics Parts Qualification and Selection

(preliminary list)

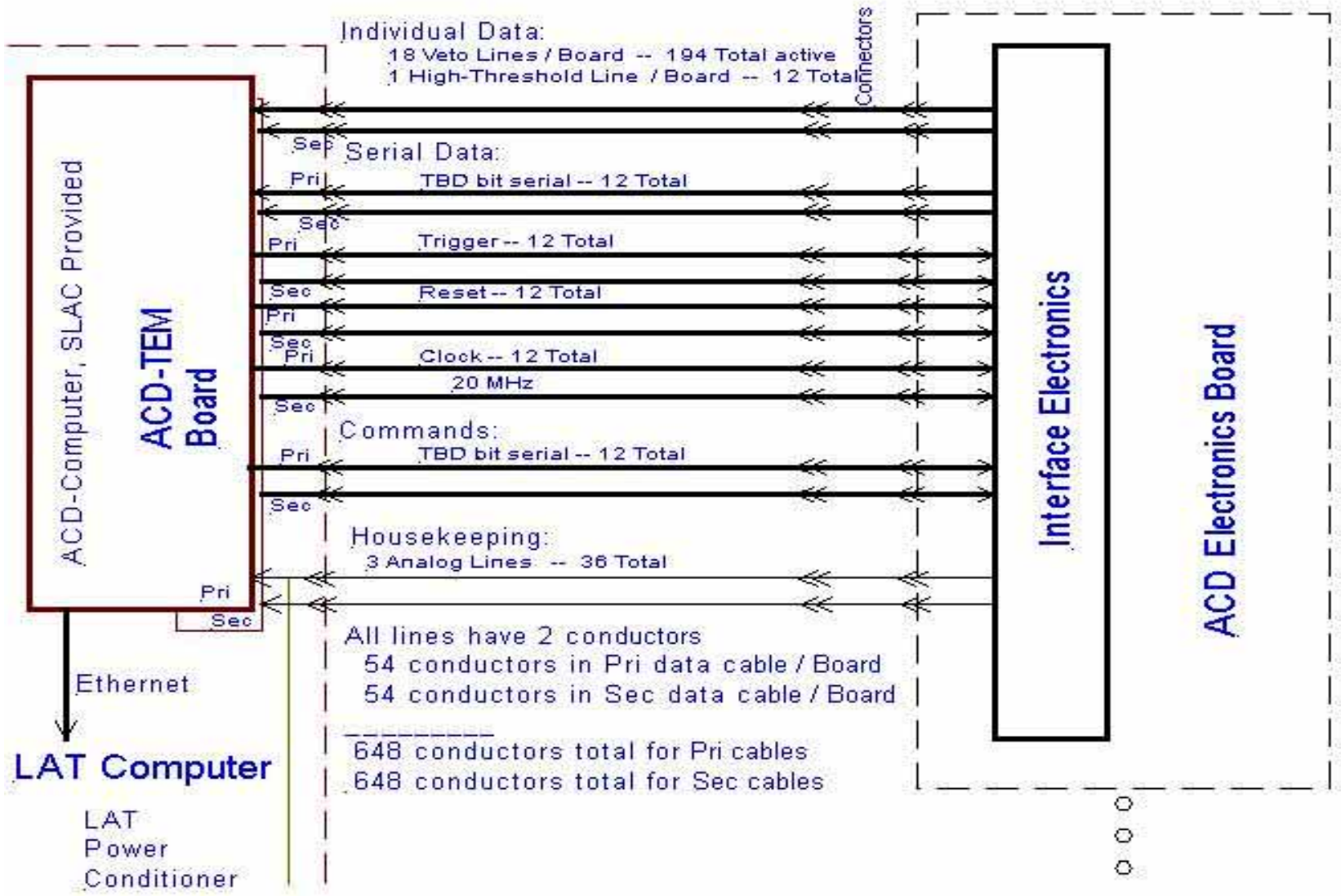
- Resistors from NPSL: MIL-R-55342, 1%, class S, RM0805, RM1206 sizes
- Ceramic Capacitors from NPSL: MIL-C-55681, 5%, 100 volt, class S, CDR31, CDR32
- Tantalum Capacitors: MIL-C-55365, 10%, 6 volt (for 3.3 volt use) and 50 volt (for 28 volt use), FLR class C
- High Voltage Capacitors: 680 pF, 2500 volt, surface mount package, MIL process control, 36 per board. Multiple manufacturers under consideration.
- Front End ASIC (GAFE): custom ASIC, Agilent 0.5 μm process, ~ 48 pin plastic quad flatpack package (vendor same as Tracker and Calorimeter), quantity 18 per board.
- Readout Controller ASIC (GARC): custom ASIC, Agilent 0.5 μm process, 208 or 240 pin plastic quad flatpack package (vendor same as Tracker and Calorimeter), quantity 1 per board.
- ADC: Type TBR (same as Calorimeter), 18 per board, provided by common buy.
- Thermistor: 30K YSI, (311P18-10S10R or similar) 1 per board
- PWB: polyimide printed circuit board per IPC-6012 Class 3, 100% netlist testing and coupon analysis.
- Connector: MIL-C-38999 Series III, 79 pin, size 22 crimp-type contacts.
- Wire: MIL-W-22759, Teflon insulation, #24 or #26
- Coatings: Uralane 5750/5753

Digital ASIC Pin Allocation

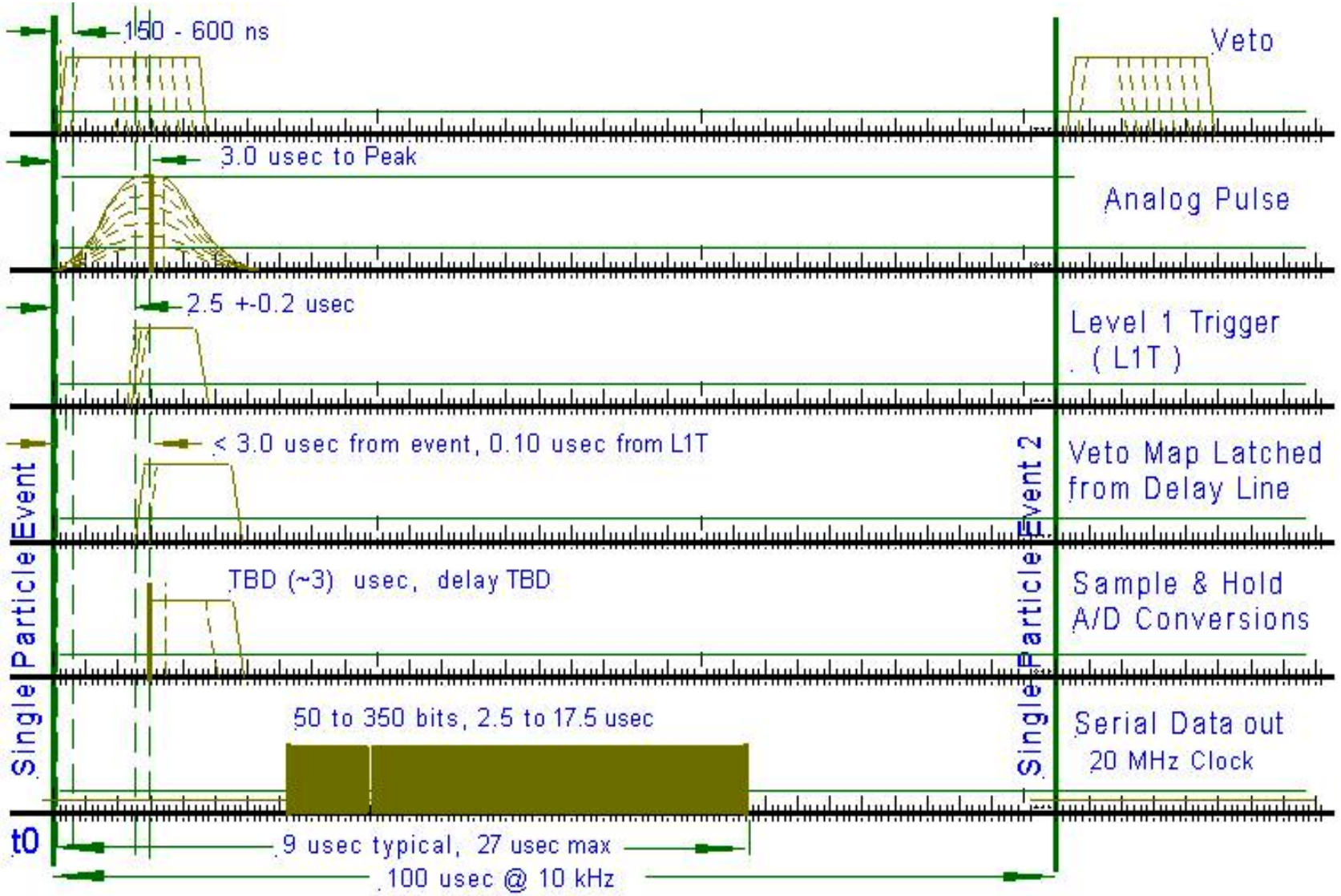
Function	#pins	#pins
3.3 Volt Power	8	8
Power Return	8	8
Clocks from TEM	4	4
Command from TEM	4	4
Power Select from TEM	4	4
Reset from TEM	4	4
Data to TEM	4	4
Vetos to TEM	72	72
CNO to TEM	4	4
LLD from GAFE	18	0
Veto from GAFE	18	18
HLD from GAFE	18	1
iret from GAFE	18	18
muxsel to GAFE	18	18
data from ADC	18	18
cmd CK to GAFE	2	2
cmd Data to GAFE	2	2
rtn data from GAFE	2	2
tci strobe to GAFE	2	2
hold to GAFE	2	2
adc clock	1	1
adc cs	1	1
hvps control	4	4
total pins	**236**	**201**

Block Diagram: Computer Interface

(Backup)



Timing Diagram
(Backup)

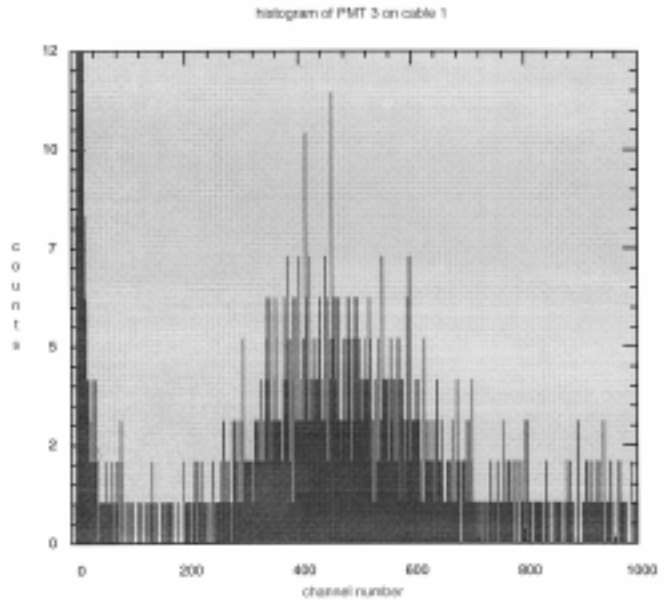


ACD Subsystem Calibration and Operation

Basic Goal: keep all ACD signals for Minimum Ionizing Particles (MIP) large enough to be detected

Primary Tool: Pulse Height Anaysis (PHA) spectra such as the example shown here.

Technique: raise HV for groups of phototubes so that the weakest tube still gives an adequate signal above noise.



Safety & Mission Assurance
Patty Huber

Safety & Mission Assurance

GENERAL

- The ACD S&MA Program will be conducted in accordance with:
  - LAT MAR, GSFC 433-MAR-0001
  - LAT PAIP, SLAC LAT-MD-00039-1
  - ACD Quality Plan, GSFC 661-TBD
- The ACD technical review program will utilize a typical GSFC technical review program, tailored via the LAT MAR/PAIP as well as the ACD Quality Plan.
- The ACD design verification program is described in the “ACD Integration and Test” and “ACD Verification Matrix” presentations of this review.
- The ACD ground data systems assurance program will be developed in accordance with LAT MAR/PAIP.
- Lessons learned from other programs will be utilized through-out the program.

Safety & Mission Assurance

System Safety Program

- The ACD safety program will be conducted in accordance with the LAT System Safety Program Plan, SLAC LAT-MD-00078-01.
- Draft ACD inputs have been submitted to the LAT System Safety Engineer at SLAC for the LAT Preliminary Hazard Analysis.
- The ACD System Safety Engineers are providing guidance to ACD designers with respect to orbital debris mitigation procedures.
  - This includes eliminating certain types of materials in the design process; however, this does not preclude using those materials for specific reasons (e.g., stiffness, reflectivity).
  - All materials used in the ACD are types that will disintegrate/demise upon reentry.
    - Analysis demonstrated that the titanium flexures that were added for stiffness will demise during de-orbiting.

Safety & Mission Assurance

Parts and Packaging Program

- **See "ACD Electronics Design" presentation.**
- The LAT EEE Part Program Control Plan, SLAC LAT-MD-00099-02, is being implemented for the ACD.
  - The LAT Parts Control Board (PCB) will manage parts activities.
    - ACD designers will generate parts list for submission to the PCB for approval.
    - The PCB will verify that all parts meet radiation, quality level, specifications, screening, DPA, testing, and source inspection requirements.
  - Grade 2 parts will be utilized per GSFC-311-INST-001 which governs the selection, screening, and qualification processes.

Safety & Mission Assurance

Parts and Packaging Program (Continued)

- All EEE parts will be derated in accordance with GSFC PPL-21 and a stress analysis will be performed for comparison against the nominal stress derating criteria.
- Initial parts activities are focusing on long lead active parts including ASIC's, Photo Multiplier Tubes (PMT's), the high voltage power supplies, etc.
  - Procurement strategies are being identified and implemented.
- Printed wiring board coupons will be evaluated prior to population.

Safety & Mission Assurance

Materials & Processes Program

- The ACD Materials Program will adhere to the LAT Mechanical Parts Plan, SLAC LAT-SS-00107-1.
- The ACD Materials Engineers have formulated a comprehensive materials and processes (M&P) program to ensure the success and safety of the mission by selecting appropriate materials and lubricants to meet the operational requirements of the instruments.
- To the maximum extent practicable, conventional and compliant materials with flight heritage have been chosen to avoid costly and time consuming testing of unproven M&P.
- When non-conventional or non-compliant materials are considered for use or when off-the-shelf items for which there is no flight history or clear identification of materials are considered, the ACD Materials Engineer will thoroughly investigate the material prior to its incorporation into the ACD.

Safety & Mission Assurance

Materials & Processes Program (Continued)

- The ACD will participate in the LAT M&P Control Board process.
  - The Board will include engineering, quality assurance, materials, and any other discipline which may be applicable to the particular situation.
  - The Board will make decisions on out-of-spec materials, material failures, out-of-date items, and limited-life items.

Safety & Mission Assurance

Reliability and Risk Management Program

- **Also see "ACD Electronics Design" presentation.**
- The ACD reliability and risk programs will be conducted in accordance with the LAT MAR and PAIP as well as the LAT Risk Management Plan.
- As part of the FMEA and CIL activities, the ACD Reliability Engineer is participating in the LAT FMEA Working Group.
- The ACD Reliability Engineer is in the process of identifying circuits that may require worst case analysis.
- ACD functional block diagrams (FBD's) have been developed as part of the ACD FMEA and Probabilistic Risk Assessment (PRA) activities.
- Reliability assessment activities have been initiated with reliability "targets" allocated to each of the ACD components from the overall ACD reliability target for mission success.
  - Portions of the ACD design/hardware which require further analysis are being identified and studied by the ACD designers, the Reliability Engineer, and the Parts Engineers.

Safety & Mission Assurance

Reliability and Risk Management Program (Continued)

- As part of the overall reliability assessment activity, analyses of the alternative design/redundancy approaches have been prepared in an effort to aid team selections to maximize the probability for mission success.
  - Six high voltage power supply design schemes, each incorporating different levels of active/stand-by redundancy, have been evaluated as part of the reliability assessment activities.
    - Reliability, cost, and design sensitivities were considered.
    - A reliability sensitivity timeline was analyzed for each option.
    - Further iterations may be required as assumptions or design specifications change.
  - Other reliability trade-offs (e.g., Photo Multiplier Tubes [PMT] gain adjustability versus degradation) and ACD components that may require further analysis have been identified.

Safety & Mission Assurance

Software Quality Assurance Program

- The ACD Software Assurance Program will be conducted in accordance with the LAT Flight Software Management Plan, SLAC LAT-MD-00104-01.
- The ACD Software Assurance Program will be formulated prior to the LAT CDR as the ACD/LAT flight software requirements are developed.
  - The Program will be consistent with the GSFC Recommended Approach to Software Development, SEL-81-305, and NASA Software Standards.
- The ACD Software QE will have insight into both flight and ground software activities including development, testing, and verification.

Safety & Mission Assurance

Hardware Quality Assurance Program

- The ACD QE is working with the ACD team as they develop designs, select parts and materials, and participate in reliability studies and analyses as well as procurement activities, trade-off studies, and the development of ACD S&MA documentation.
- The ACD QE's program participation will continue through design, fabrication/assembly, integration, and testing with the QE performing workmanship inspections and test monitoring.
- The ACD QE will assist the ACD System Assurance Manager in overseeing the entire ACD S&MA program.
- The ACD hardware will be built utilizing NASA workmanship standards with only certified personnel performing fabrication, assembly, and inspection duties.
  - To date, no new or special processes have been identified.

Safety & Mission Assurance

Contamination Control Program

- The ACD contamination control program will be governed by the LAT and GLAST contamination control plans which are under development.
- To be consistent with the LAT/GLAST contamination control plans:
  - All materials used in the ACD will meet space flight quality levels (i.e., TML < 1.0%, CVCM < 0.1%).
  - The ACD will be assembled in an appropriately clean environment consistent with LAT/GLAST requirements including the use of clean room garments and equipment.
  - All ACD surfaces will meet visibly clean flight levels per Level 750B of MIL-STD-1246.
  - ACD hardware will be baked-out at either the component-level or system-level to the contamination levels necessary to prevent the contamination of the spacecraft star trackers.

Safety & Mission Assurance

Back-up Information

Safety & Mission Assurance

UNCONTROLLED REENTRY FORM DECAYING ORBIT										
Parent object is in line 1										
Object						Material	Demise		Casualty Area (m^2)	
Surface	Type	Diameter (m)	Length (m)	Height (m)	Mass (kg)	Type	Altitude (km)	Qty	Incident	Total
ACD	Box	2.0000	2.0000	2.0000	452.0000	Al 2024-T3	77.944	1	0	0
Flexure	Box	0.0900	0.0600	0.5400	0.5000	Titanium	0	8	0.5447	4.3576
ACD flex	Box	0.0900	0.0600	0.5400	0.5000	ACD flex	77.944	8	0	0
Totals										4.3576
Scenario - flexure modeled as box using DAS 1.5.3 - ACD flex = synthetic Ti										

Safety & Mission Assurance

Primary Materials Reference Documentation

- GSFC 731-0005-83, "General Fracture Control Plan for Payloads Using the Space Transportation System (STS)", November 25, 1988.
- GSFC 541-PG-8072.1.2, "GSFC Fastener Integrity Requirements", March 5, 2001.
- NASA-STD-5001, "Structural Design and Test Factors of Safety for Spaceflight Hardware", June 21, 1996.
- NASA Reference Publication 1124, "Outgassing Data for Selecting Spacecraft Materials" June 1997
- NASA-STD-6001, "Flammability, Odor, Off-gassing and Compatibility Requirements & Test Procedures for Materials in Environments That Support Combustion" February 9, 1998.
- MSFC-SPEC-522, "Design Criteria for Controlling Stress Corrosion Cracking", July 1, 1987.
- MIL-HDBK-5H, "Metallic Materials and Elements for Aerospace Vehicle Structures", December 1998.
- SP-R-0022A, "General Specification-Vacuum Stability Requirements of Polymeric Materials for Spacecraft Applications".
- ASTM E-595, "Standard Test Method for Total Mass Loss and Collected Volatile Condensable Materials from Outgassing in a Vacuum Environment, Re-approved 1999.

Safety & Mission Assurance

FMEA - GLAST LAT ACD Failure Modes

(D1)

RCH, June 11, 2001

Component	Function	Failure Type or Cause	Failure Effect	Possible Mitigation	Performance after Mitigation	Remarks
ACD Subsystem	Background rejection	Elec. power loss	1) ACD unavailable to L1T; 2) Charged particle filtering much more difficult =>Large reduction in LAT throughput	none	---	Category 2
ACD TEM	ACD interface	Total	"	Redundant TEM	Nominal	Category 2R
ACD Side (1 of 4)	Background rejection	Elec. power loss	1) ACD less effective in L1T; 2) Charged particle filtering more difficult =>Significant reduction in LAT throughput	none	---	Category 2 or3 (may not be possible)
Event board	HV generation and signal (9 or 18) processing	Elec. power loss	Efficiency loss for 9(18?) tiles (0.9997=>0.997)	Reduce thresholds for redundant PMT's	possibly some LAT efficiency loss	Category 3
Event board	HV generation and signal (9 or 18) processing	Command/data clock loss	1) 9(18?) VETO thresholds fixed; 2) 9(18?) CNO thresholds fixed; 3) Loss of PHA data for 9(18?) PMT; 4) Partial loss of VETO MAP	none	---	Category 3
Event board	HV generation and signal (9 or 18) processing	Command loss	1) 9(18?) VETO thresholds fixed; 2) 9(18?) CNO thresholds fixed; 3)Test mode unavailable	none	---	Category 3
Event board	HV generation and signal (9 or 18) processing	Loss of output data signal	1) Partial loss of VETO MAP; 2) Loss of PHA data for 9(18?) PMT's	none	---	Category 3
Event board	HV generation and signal (9 or 18) processing	Loss of TRIGACK	1) Partial loss of VETO MAP; 2) Loss of PHA data for 9(18?) PMT's	none	---	Category 3

Safety & Mission Assurance

FMEA – GLAST ACD Failure Modes continued

Component	Function	Failure Type or Cause	Failure Effect	Possible Mitigation	Performance after Mitigation	Remarks
HVPS failure	Activate 9 PMT's	Failed internal component	Efficiency loss for 9 tiles (0.9997=>0.997)	Switch to redundant HVPS(?)	Nominal(?)	Category 3or 4
ASIC	PMT signal (9) processing	Elec. power loss	Efficiency loss for 9 tiles (0.9997=>0.997)	Reduce threshold for redundant PMT	Probably some loss of efficiency	Category 3 or 4
ASIC	PMT signal (9) processing	Channel loss due to internal failure	Efficiency loss for 1 tile (0.9997=>0.997)	Reduce threshold for redundant PMT	Probably some loss of efficiency	Category 4
PMT	Detect light from scintillator tile	Internal failure or loss of HV connection	Efficiency loss for 1 tile (0.9997=>0.997)	Efficiency loss for 1 tile (0.9997=>0.997)	Efficiency loss for 1 tile (0.9997=>0.997)	Category 4
PMT	Detect light from scintillator tile	Degradation (some expected)	Signal degradation	raise HV or lower thresholds	nominal	Category 4
VETO Signal	VETO function	Loss	Efficiency loss for 1 tile (0.9997=>0.997)	Efficiency loss for 1 tile (0.9997=>0.997)	Efficiency loss for 1 tile (0.9997=>0.997)	Category 4
Scintillator Tile Assembly	Detect charged particles via scintillation light	Light-exposure - penetration of light-tight wrap	Loss of functionality => some loss of DAQ filtering efficiency	none	---	Category 3 or 4
Fiber coupling	Conduct light from tile to PMT	Degradation due to vibration or aging	Signal degradation	raise HV or lower thresholds	Possibly some efficiency loss	Category 4
Fiber	Conduct light from tile to PMT	Break	Reduced efficiency in related portion of tile	raise HV or lower thresholds	Possibly some efficiency loss	Category 4
Analog sensor	Diagnostic information	Loss	Diagnostic information lost	none	---	Category 4

Safety & Mission Assurance

REQUIREMENT:

Reliability Assessment Scope (MAR/PAIP Paragraph 8.2.4): "When necessary/prudent or when agreed upon with the GSFC Project Office, GLAST LAT will perform comparative numerical reliability assessments to:

a) Evaluate alternate design concepts, redundancy and cross-strapping approaches, and part substitutions

b) Identify the elements of design which are the greatest detractors of system reliability

c) Identify those potential mission limiting elements and components that will require special attention in part selection, testing, environmental isolation, and/or special operations

d) Assist in evaluating the ability of the design to achieve mission life requirement and other reliability goals as applicable

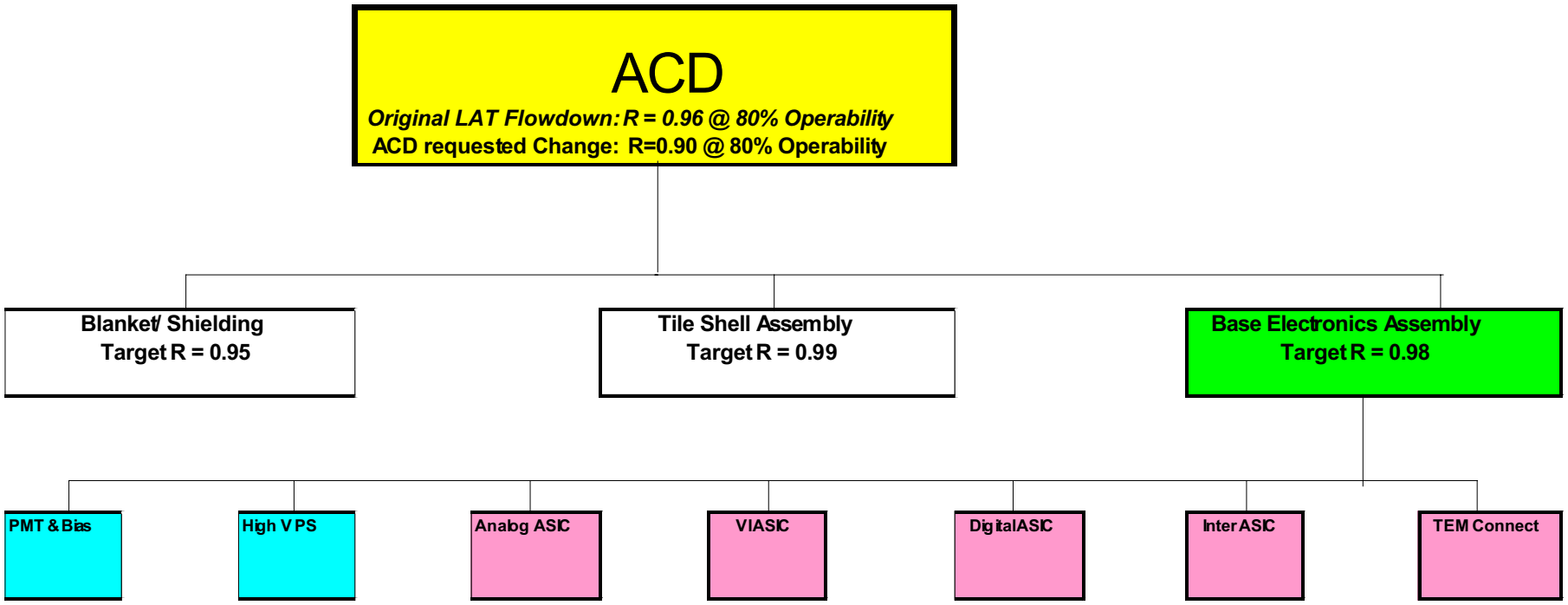
e) Evaluate impact of proposed engineering changes and waiver requests on Reliability"

ACD ASSESSMENT:

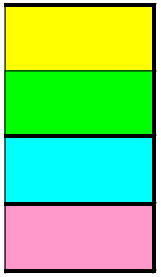
- In accordance with Paragraph 8.2.4a of the LAT PAIP and MAR, a numerical assessment was performed to evaluate ACD component reliability allocations as well as different High Voltage Power Supply redundancy approaches in order to maximize the probability for mission success over the life (5 Year minimum) of GLAST.
- The ACD reliability target, flowed-down from the LAT, was originally 0.96 at 80% operability (i.e., less than 20% degradation of the effective LAT area) over 5 years minimum.
    - A change from 0.96 to 0.90 was requested to maintain the 0.95 target for the meteorite shield as defined in the Level 3 specification (i.e., 1% chance of a puncture somewhere per year). (See chart on next sheet.)

Safety & Mission Assurance

Redundancy



Legend:



Reliability/Operability Goal flowdown from SLAC

Target area for Comparative Numerical Assessments

Reliabilty Estimates based on Mil-217F and supplier data

Reliability allocated as needed to meet SLAC flowdown

Safety & Mission Assurance

Redundancy

Base Configuration:

- 12 ACD Event Processor boards with 18 PMTs, 18 VI_ADC ASICs, 18 Analog ASICs, 2 Digital ASICs, 1 Interface ASIC, & 1 TEM Interconnect each

High Voltage P/S Redundancy configurations analyzed:

A - 1 P/S per board, 0 stand-by (1 active P/Ss per 18 PMT's)

B - 2 P/S per board, 1 stand-by (1 active P/Ss per 18 PMT's)

C - 3 P/S per board, 2 stand-by (1 active P/Ss per 18 PMT's)

D - 2 P/S per board, 0 stand-by (2 active P/Ss per 18 PMT's)

E - 4 P/S per board, 2 stand-by (2 active P/Ss per 18 PMT's)

F - 6 P/S per board, 4 stand-by (2 active P/Ss per 18 PMT's)

Key Points

- Assumptions (see next page) are subject to change
- Intent of analysis is to show reliability sensitivity to various P/S redundancy approaches

Safety & Mission Assurance

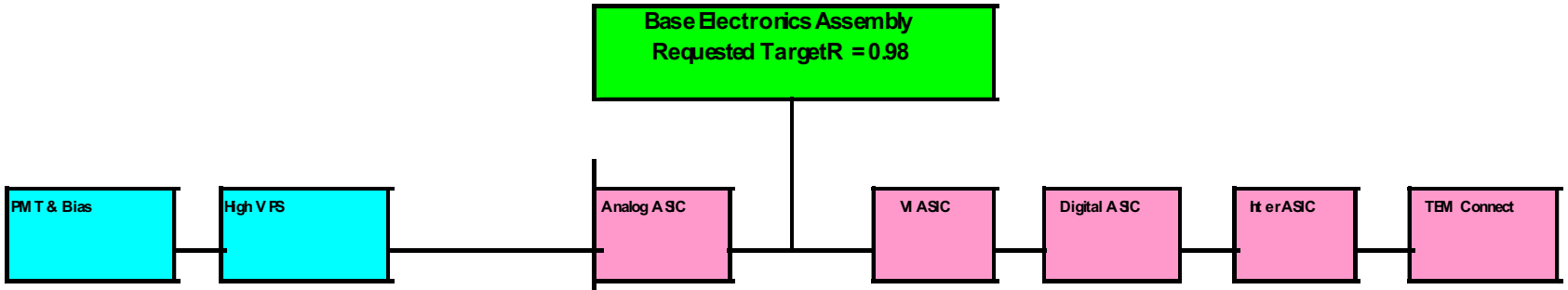
Redundancy

Assumptions/Ground Rules

- The ACD Base Electronics Assembly allocation is 0.98, flowed down from the ACD reliability target of 0.96 reliability at 80% operability or, in other words, no more than 20% degradation of the overall effective LAT area.
  - The ACD Team is requesting that ACD reliability target be lowered to 0.90.
- An inability to process information from more than 1 tile constitutes failure (where failure is defined as the inability to process data from both PMT's).
- The ACD is comprised of the PMT & Bias, High Voltage P/S, Analog ASIC, VI ASIC, Digital ASIC, Interconnect ASIC, & TEM Connect generated for the PMT & Bias and High Voltage P/S only.
  - All other reliability values are represented as allocations.
- Power supply failure rates are based on MIL-STD-217F (Notice 2) without considerations to temperature or derating.
- PMT failure rates are based on Hamamatsu projections for fully screened space parts.
- Solder connection and board reliability need not be considered.
- Fourteen of 18 PMT's are functional per board.
- Stand-by switching operates without any anomalies.

Safety & Mission Assurance

Redundancy



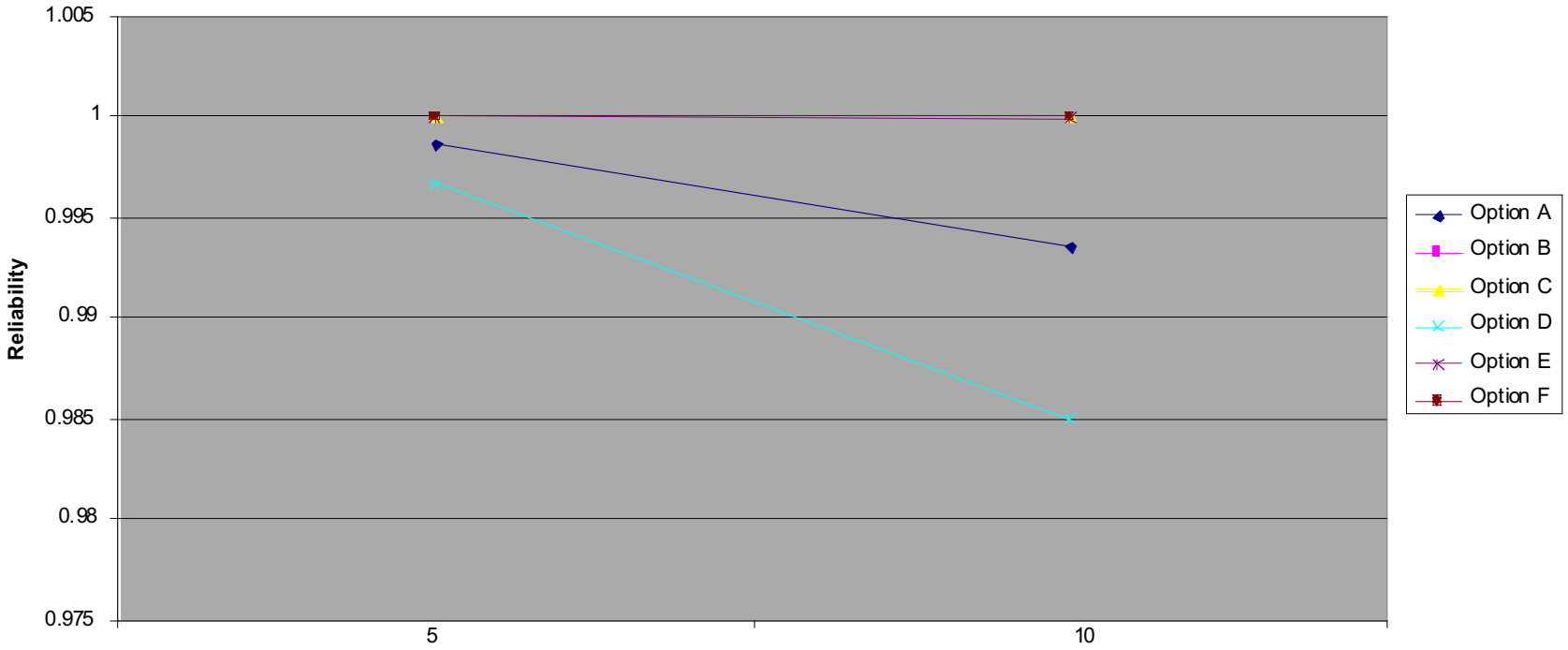
Options	Estimated Reliabilty (5 yr)					Required Allocation (5 yr)
A	0.999999994	x	0.998704116	=	0.998704154	0.98127158
B	0.999999994	x	0.999999814	=	0.999999808	0.98000019
C	0.999999994	x	0.99999997	=	0.999999964	0.98000004
D	0.999999994	x	0.9967	=	0.996699994	0.98324471
E	0.999999994	x	0.999970726	=	0.99997072	0.9800287
F	0.999999994	x	0.999999	=	0.999998994	0.98000099

Options	Estimated Reliabilty (10 yr)					Required Allocation (10 yr)
A	0.999999994	x	0.993601386	=	0.99360138	0.98631103
B	0.999999994	x	0.99998553	=	0.999985524	0.98001419
C	0.999999994	x	0.99999997	=	***0.999999964***	0.98000004
D	0.999999994	x	0.98499	=	0.984989994	0.99493396
E	0.999999994	x	0.999937697	=	0.999937691	0.98006107
F	0.999999994	x	0.999999	=	***0.999998994***	0.98000099

Safety & Mission Assurance

Redundancy

Power Supply Reliability over time



Safety & Mission Assurance

Redundancy

PER MIL217-F /HV in series,

ACD - HVPS Failure 3.79E-01 failures/10 ^{6} hours *Translates into 3.32E-03 failures/year*

MTBF - Years/failure 301.20

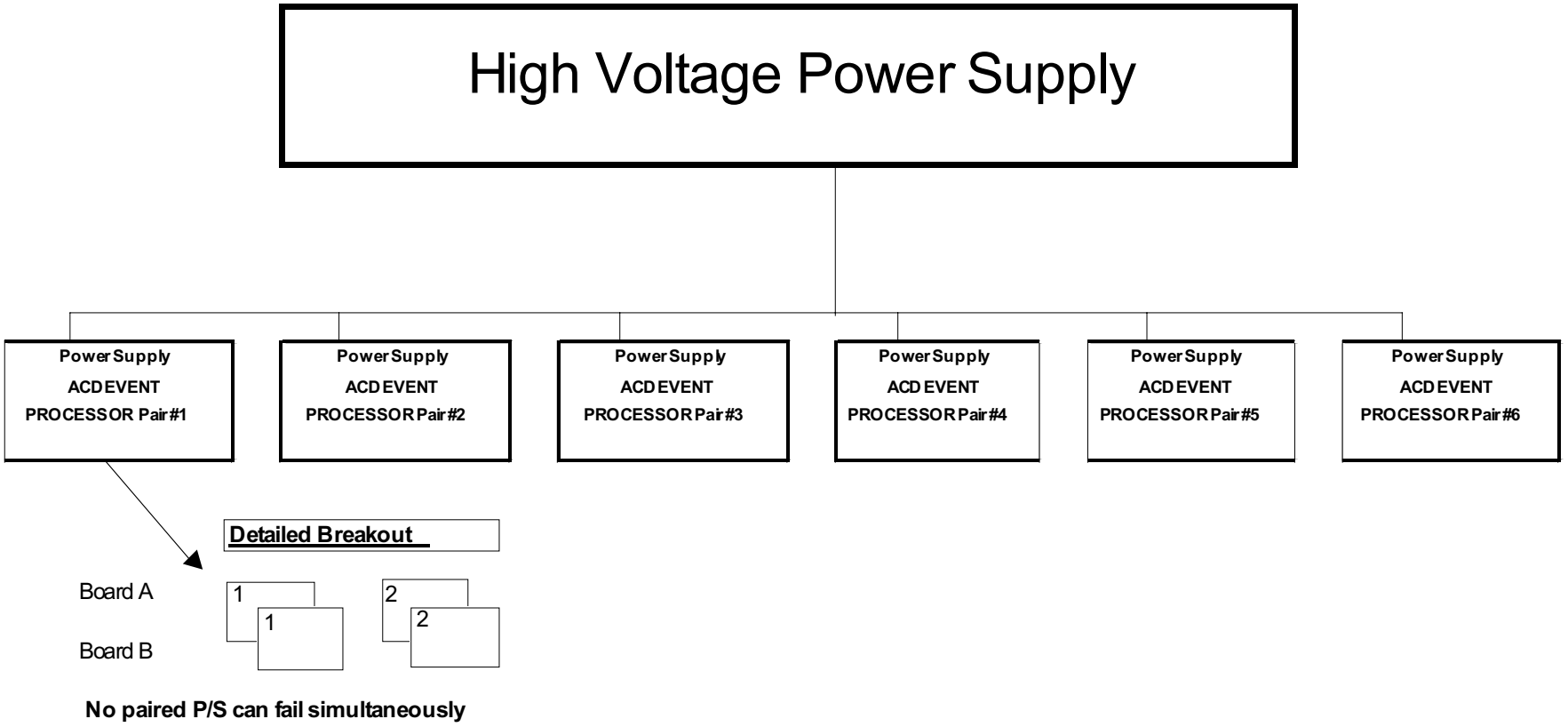
Hours/Year	8760
Transistor, NPN	**ST1, ST2**
Years/Failure	146917.96
L_P_Total (fail/10 ^{6} hours)	7.77E-04
Quanity	3
L_g (fail/10 ^{6} hours)	7.40E-04
PI_Q	7.00E-01
PI_E	5.00E-01
Switching/Zenor Diode	**ST3, ST4**
Years/Failure	15531.33
L_P_Total (fail/10 ^{6} hours)	7.35E-03
Quanity	7
L_g (fail/10 ^{6} hours)	3.00E-03
PI_Q	7.00E-01
PI_E	5.00E-01
High Voltage Diode	**ST5**
Years/Failure	415.11
L_P_Total (fail/10 ^{6} hours)	2.75E-01
Quanity	20
L_g (fail/10 ^{6} hours)	5.00E-03
PI_Q	5.50E+00
PI_E	5.00E-01
Op Amp	**ST6**
Years/Failure	3004.09
L_P_Total (fail/10 ^{6} hours)	3.80E-02
Quanity	1
L_g (fail/10 ^{6} hours)	3.80E-02
PI_Q	1.00E+00
PI_E	1.00E+00
RM1206 Resistor	**ST7**
Years/Failure	24682.22
L_P_Total (fail/10 ^{6} hours)	4.63E-03
Quanity	25
L_g (fail/10 ^{6} hours)	3.70E-03
PI_Q	1.00E-01
PI_E	5.00E-01

Hours/Year	8760
Capacitor, Ceramic	**ST8**
Years/Failure	11891171.99
L_P_Total (fail/10 ^{6} hours)	9.60E-06
Quanity	8
L_g (fail/10 ^{6} hours)	2.40E-03
PI_C	1.00E-03
PI_S	5.00E-01
HV Resistor	**ST9**
Years/Failure	1585489.60
L_P_Total (fail/10 ^{6} hours)	7.20E-05
Quanity	2
L_g (fail/10 ^{6} hours)	2.40E-03
PI_Q	3.00E-02
PI_E	5.00E-01
Inductor MPP Core	**ST10**
Years/Failure	253678335.87
L_P_Total (fail/10 ^{6} hours)	4.50E-07
Quanity	1
L_g (fail/10 ^{6} hours)	3.00E-05
PI_Q	3.00E-02
PI_E	5.00E-01
Transformer, CM	**ST11**
Years/Failure	21139.86
L_P_Total (fail/10 ^{6} hours)	5.40E-03
Quanity	1
L_g (fail/10 ^{6} hours)	5.40E-03
PI_Q	1.00E+00
PI_E	5.00E-01
Transformer, Pulse	**ST12**
Years/Failure	3.03E+09
L_P_Total (fail/10 ^{6} hours)	1.10E-02
Quanity	1
L_g (fail/10 ^{6} hours)	2.20E-02
PI_Q	1.00E+00
PI_E	5.00E-01

Hours/Year	8760
Transformer, Osc.	**ST13**
Years/Failure	4659.40
L_P_Total (fail/10 ^{6} hours)	2.45E-02
Quanity	1
L_g (fail/10 ^{6} hours)	4.90E-02
PI_Q	1.00E+00
PI_E	5.00E-01
Capacitor, Tantalum	**ST14**
Years/Failure	475646.88
L_P_Total (fail/10 ^{6} hours)	2.40E-04
Quanity	1
L_g (fail/10 ^{6} hours)	4.00E-04
PI_C	1.20E+00
PI_E	5.00E-01
Capacitor, HV 20pF	**ST15**
Years/Failure	329452.38
L_P_Total (fail/10 ^{6} hours)	3.47E-04
Quanity	2
L_g (fail/10 ^{6} hours)	9.90E-04
PI_C	3.50E-01
PI_E	5.00E-01
Capacitor, HV 6800pF	**ST16**
Years/Failure	10676.70
L_P_Total (fail/10 ^{6} hours)	1.07E-02
Quanity	20
L_g (fail/10 ^{6} hours)	9.90E-04
PI_C	5.40E-01
PI_E	5.00E-01
Capacitor, HV 6800pF	**ST17**
Years/Failure	8.42E+08
L_P_Total (fail/10 ^{6} hours)	9.90E-04
Quanity	2
L_g (fail/10 ^{6} hours)	9.90E-04
PI_C	5.40E-01
PI_E	5.00E-01

Safety & Mission Assurance

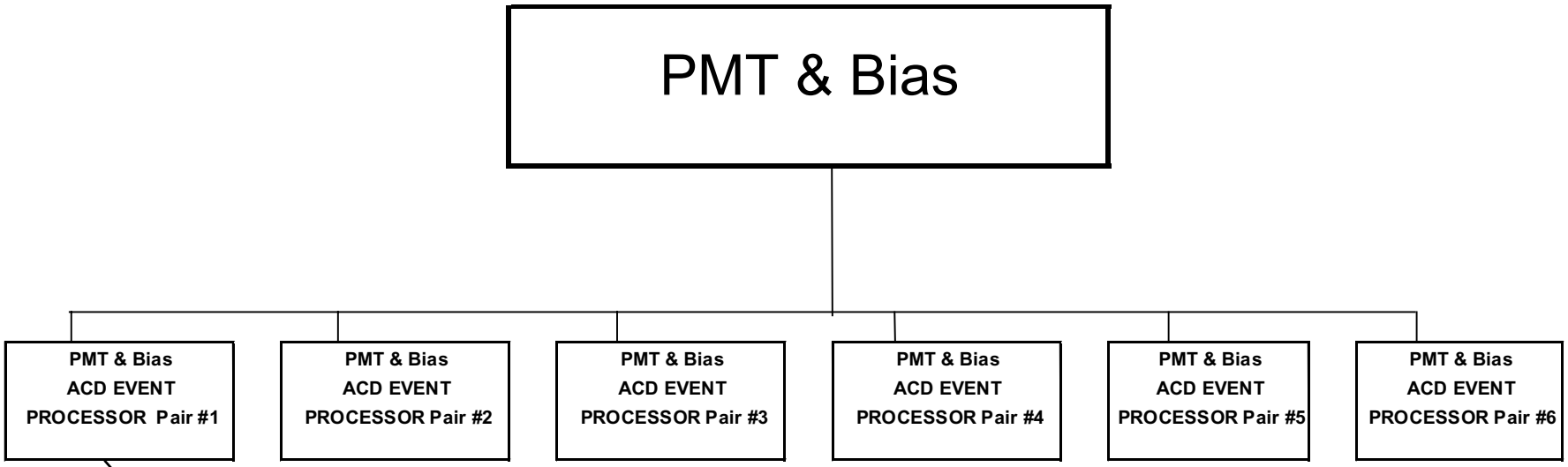
Redundancy

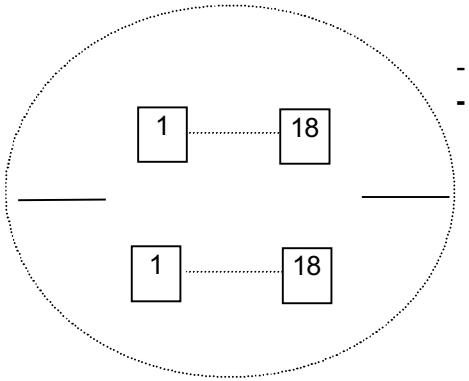


No paired P/S can fail simultaneously

Safety & Mission Assurance

Redundancy





- There are 18 PMTs per board, 32 PMTs per pair.
- **For analysis purposes, it was assumed that a minimum 14 of the 18 PMT"s were operational**

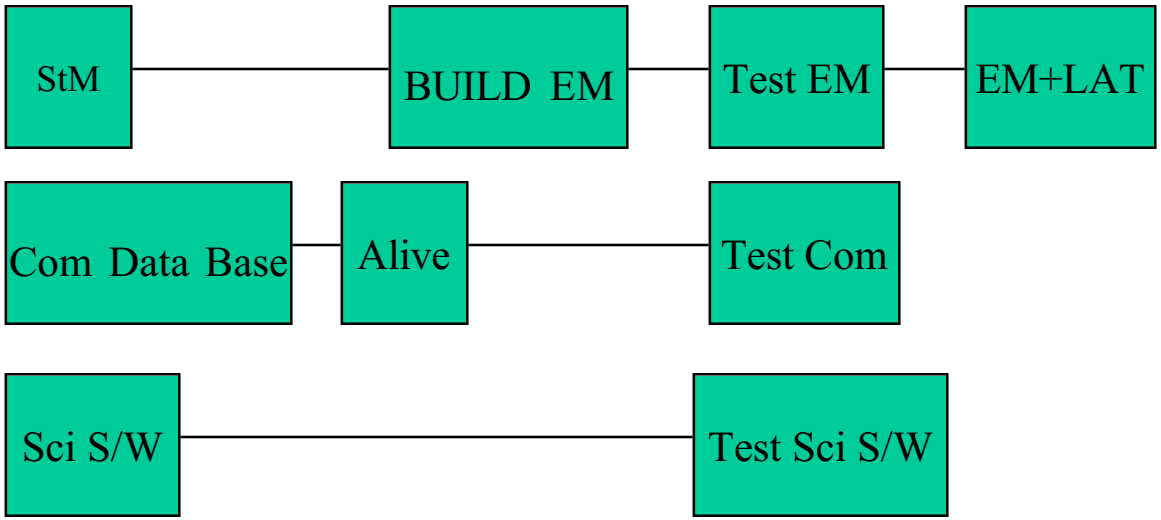
ACD I&T

ACD Integration & Test
John Lindsay

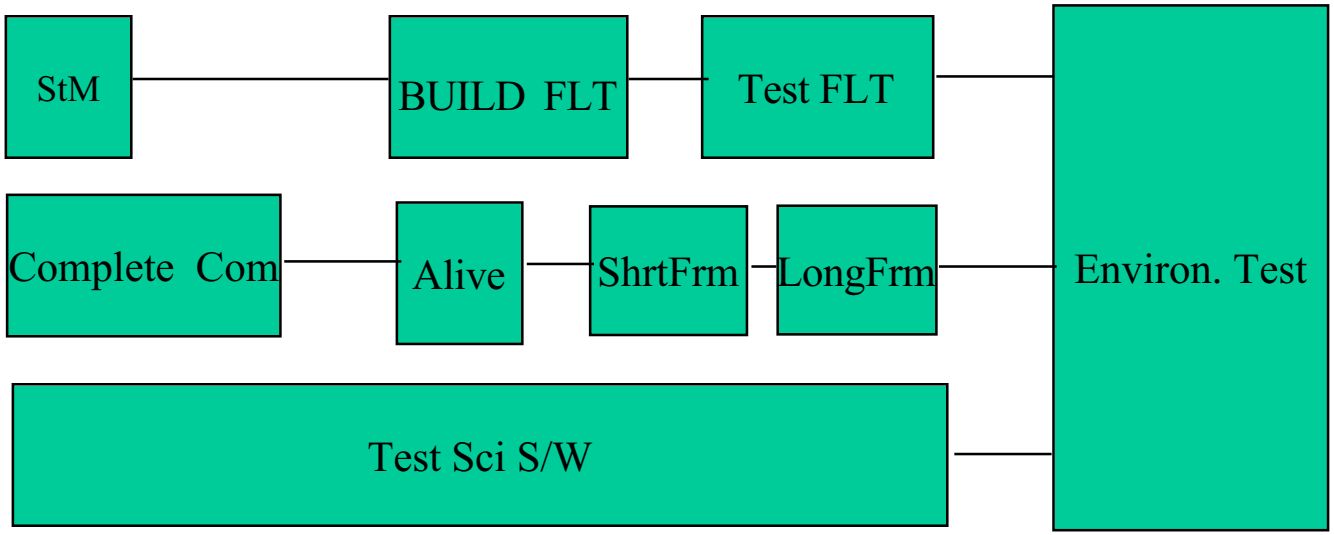
ACD I&T Tasks

- EM I&T
  - Handling a couple of detector strips
    - Assembly-electro-optical
    - Test-minimal
    - Support at LAT level
- Flight I&T
  - Full up assembly (Tiles, Harness, Boxes)
  - Harness (Flight, GSE)
  - GSE (Test)
  - Commanding
- LAT support

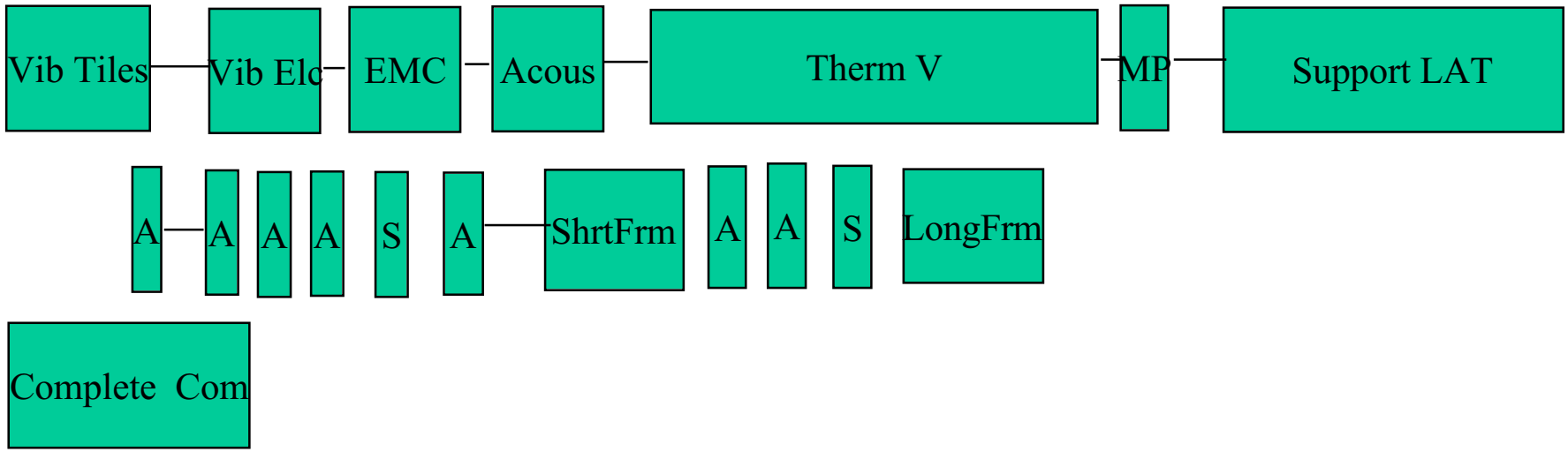
ACD EM FLOW


StM
BUILD EM
Test EM
EM+LAT
Com Data Base
Alive
Test Com
Sci S/W
Test Sci S/W

ACD FLT-U FLOW 1



ACD FLT-U ENVIRONMENTAL



ACD EM

- Integration
  - Practice tile and detector assembly
    - electrical
    - optical-fiber connections
  - Safe-to-mate-method and format established for flight
  - Hardware integration-first cut at procedures
  - Commanding-first cut at procs, scripts
    - Alive, ShortFrom, LongForm
- EM/SLAC practice

ACD FM

- Integration-lessons learned from EM
- Test/Characterization/Calibration
  - Acoustic
  - EMI-isolation
  - Thermal Vac/Thermal Balance
  - Vibration
- Support LAT at SLAC
  - Assembly
  - ShortForm

ACD Status

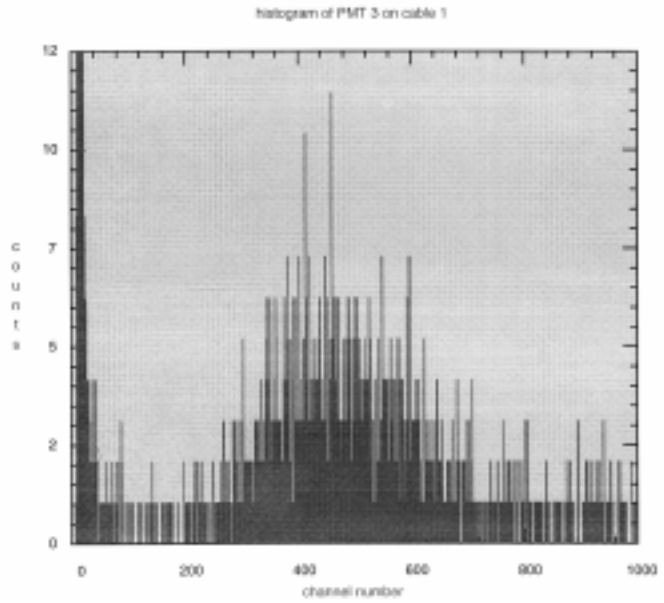
- Personnel
  - One at present/part time
  - People needed to fill roles, currently working other projects
- Facilities
- Schedule--covered elsewhere

ACD Subsystem Calibration and Operation

Basic Goal: keep all ACD signals for Minimum Ionizing Particles (MIP) large enough to be detected

Primary Tool: Pulse Height Anaysis (PHA) spectra such as the example shown here.

Technique: raise HV for groups of phototubes so that the weakest tube still gives an adequate signal above noise.



ACD Subsystem Status

ACD Management
Rudy Larsen

Subsystem status

Management

- ***ACD Subsystem Team has staffed up.***
- ***The WBS dictionary has been established to level 6***
- ***ACD Schedule and Cost Estimate are effectively completed.***
- ***The ACD was reviewed as part of the DOE/NASA Review Committee (a.k.a. The Lehman Review) on February 13-15 at SLAC in Palo Alto, CA. The ACD subcommittee review lead is Pawel de Barbaro from University of Rochester and Fermilab.***
- ***He stated that the detector technology chosen for the ACD matches performance requirements well.***
- ***Recommendations specific to the ACD are:***
  - ***Perform optimization of the Optics design. - Complete***
  - ***Perform tests to prove scintillating fiber ribbons meet efficiency requirements. - Complete***
  - ***Provide complete technical drawings for mounting tiles and Photo-Multiplier Tubes (PMTs) - Complete***

Subsystem status

Systems

- ***Tom Riley as ACD Systems Engineer and has been developing block diagrams, flowdown of level III requirements, interface requirements and trade studies. Additional Systems help has been assigned.***

Safety and Mission Assurance

- ***Prepared the ACD Quality Plan to augment the LAT PAIP with NASA/GSFC-mandated requirements.***
- ***ACD Reliability Engineer has performed redundancy analyses and reliability assessments on ACD hardware, participated in LAT FMEA activities, and prepared ACD functional block diagrams.***

Tile Shell Assembly

- ***Visited Pawel de Barbaro at Fermilab to investigate Tile Detector Assembly fabrication techniques.***

Subsystem status

Tile Shell Assembly (cont.)

- *Visited suppliers of scintillator tile, ElJen in Sweetwater Texas.*
- *Conducted light output experiments on scintillator tile and tapes.*
- *Developed complete assembly flow diagram of Tile Shell Assembly and Dase Electronics Assembly.*
- *Developed tile wrapping and bagging techniques including materials selection.*
- *Developed connector concepts for waveshifting to clear fiber coupling and clear fiber to PMT coupling. Prototypes of connector fabricated*
- *Developed preliminary design for Tile Shell Assembly including honeycomb foam core and face sheets material selection.*
- *Developed Tile Detector Assembly mounting technique.*
- *Chose 1d overlapping tile layout with scintillating tapes over 2d complete tile overlapping schemes to reduce overall complexity.*
- *Developing optical fiber routing layouts.*
- *Updated ACD Mass estimates.*

Subsystem status

Base Electronics Assembly

- *Met with Hammamatsu to discuss Photomultiplier Tube specifications, qualification and pricing.*
- *Researched alternative PMT suppliers.*
- *A first draft of the Level IV electronics requirements was received in July*
- *Analysis of system reliability continued, being refined as requirements were updated*
- *Generated newer and more detailed block diagrams of the ACD electrical system as the requirements and subsequent design were refined*
- *Generated a slide package for the electronics peer review*
- *Made good progress on discussion and documentation of the ACD-to-LAT electrical interfaces.*
- *Trigger primitives and rate counters have been moved to the TEM*
- *Completed ACD architecture trade studies*
- *Updated the ACD Electronics Specifications document to reflect the current status of the design*

Subsystem status

Base Electronics Assembly (cont.)

- ***Designed and built proto-type PMT housing and coupler***
- ***Working on routing of the ACD/LAT electrical cables***

Micrometeoroid Shield & Thermal Blanket

- ***Goal is to meet or exceed GLAST Anti-Coincidence Detector (ACD) Meteoroid/Debris requirements established by ACD Project Office.***
- ***Combined hypervelocity impact test and analysis approach used to develop & verify GLAST ACD meteoroid/debris shielding***
- ***Baseline shield concept evaluated by initial hypervelocity impact tests***
- ***Initial ballistic limit equations developed and coded into BUMPER program***
- ***Initial results of tests and analyses by JSC have been received by GSFC.***

Subsystem status

Software Support

- ***Accomplished major rewrite of ACD instrument for balloon code to match coding standards of new SLAC FSW management.***
- ***Implemented new SLAC based CM system (CMX) for flight software.***
- ***Supported checkout and testing of BFEM ACD instrument before and after arrival at SLAC.***
- ***Diagnosed BFEM ACD hardware problems with integrated BFEM LAT.***
- ***Defined BFEM ACD data formats.***
- ***Integrated ACD BFEM software with DAQ during FSW integration meeting at SLAC.***
- ***Defined, designed, and tested code for commanding BFEM ACD during testing and flight.***
- ***Provided WBS and cost estimates for ACD FSW effort.***
- ***Created ACD specific GSE for balloon flight to display rates,***
- ***housekeeping, and pulse height histograms.***
- ***Obtained and set up backup computer (from excess) for FSW building and testing.***

Subsystem status

I&T

- ***Provided schedule and cost estimates for ACD Hardware/ Software Integration, LAT I&T support and Mission I&T support.***

Ground Support Facilities and Equipment

- ***Developed requirements for ACD Mechanical GSE including handling fixtures and shipping containers.***
- ***Refined requirements for ACD Electrical GSE.***

Risks and Mitigations

♦ *Accelerated schedule - Issue: risk to readiness for the LAT Preliminary Design Review. Mitigation is additional staff and funding, early ACD Design Peer Review*

♦ *Revised cost estimate - Issue: threat to LAT budget Mitigation: Complete redesign of ACD electronics; shared use of LAT resources.*

♦ *Mass constraint - Issue: risk to efficiency, redundancy, and margin of the Anticoincidence Detector. Mitigation: careful design; additional mass request*

♦ *Thermal blanket/micrometeoroid shield performance - Issue: risk to durability of ACD over its lifetime. Mitigation: agreement for design help from Johnson Space Center, which specializes in protection against penetrations.*

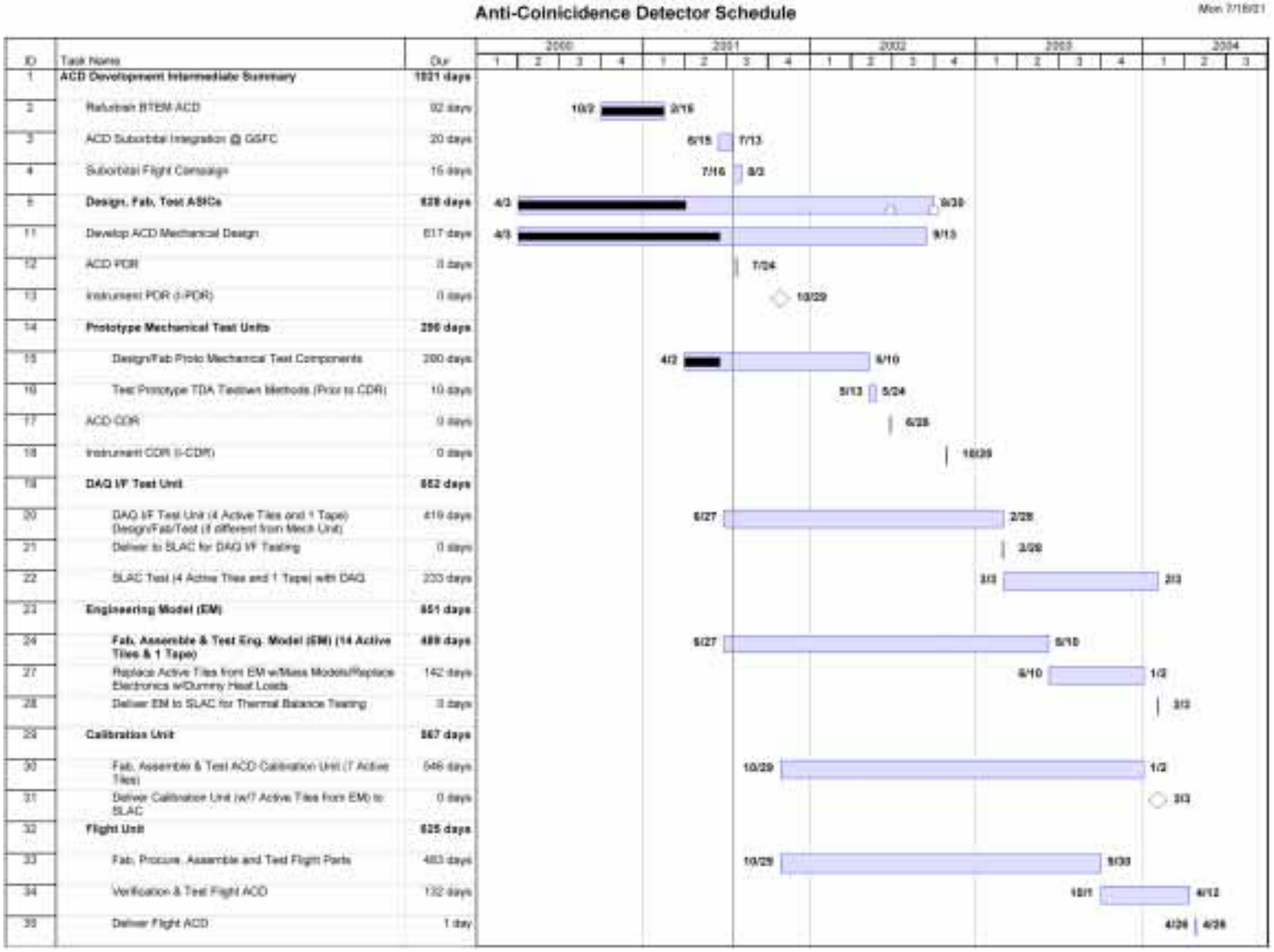
♦ *Light collection from scintillator tiles - Issue: affects efficiency throughout the life of the mission. Mitigation: Tests to optimize the light collection and use of clear optical fiber transmission lines.*

♦ *Gaps between scintillator tiles - Issue: Lowers Background rejection efficiency. Mitigation: cover gaps with scintillating tapesin one dimension and overlap detector tiles in the other.*

Risks and Mitigations

- ***Electronics Cost - Different cost estimates within GSFC and SLAC reflect disagreements on ways of doing business. Mitigation is all parties meet to understand differences and reach agreement***
- ***Reliability Requirements - To yield higher reliability number Micrometeoroid Shield may need thickening which could lead to higher background. Mitigation is more analyses are needed.***
- ***Background entering at the edge of the bottom of the ACD - Mitigation***
is further analyses needed.
- ***LAT other subsystems' ability to compensate for loss of effective area - Mitigation is also further analyses.***

TOP LEVEL SCHEDULE

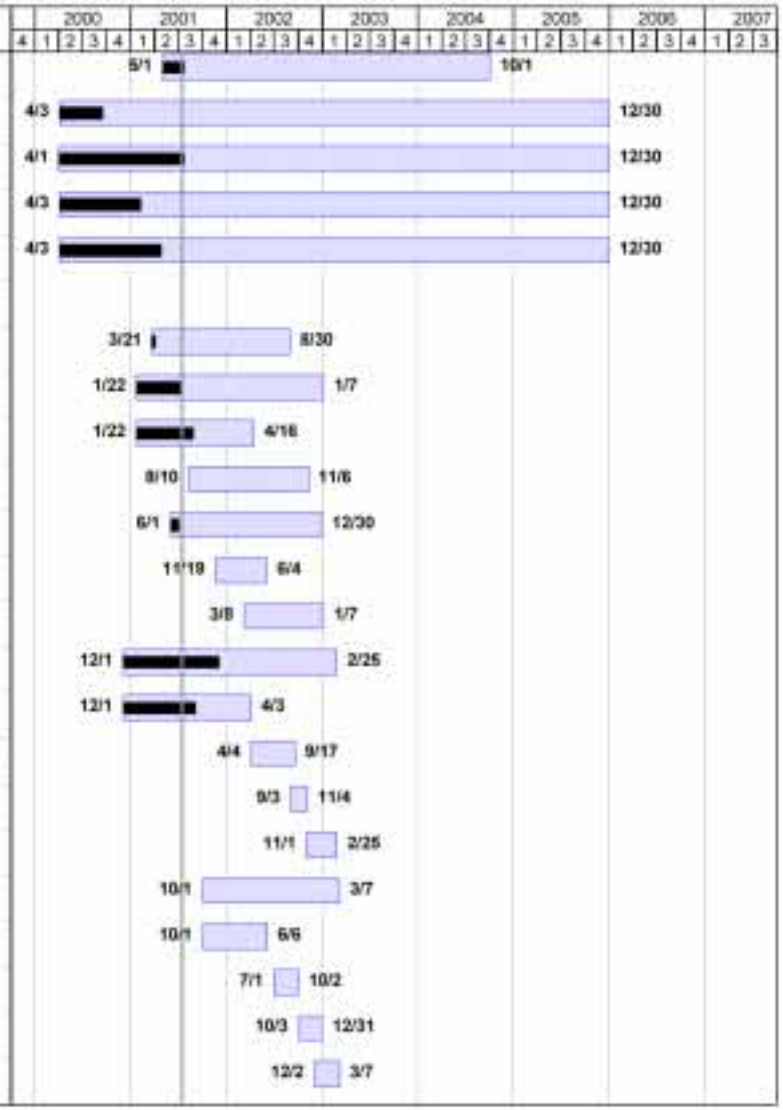


Anti-Coincidence Detector Subsystem Schedule (Preliminary)

ID	WBS	Task Name	Start	Finish
1		**GLAST LAT Project-Level Control Milestones**		
11	**4.1.6**	**Anti-Coincidence Detector (ACD) Subsystem**		
12	**4.1.6.1**	**ACD Project Management / Subsystem Engineering**	4/1	12/30
13	**4.1.6.1.1**	**Project Management**	4/3	12/30
14	4.1.6.1.1.1	Project Administration / Support	4/3	12/30
15	4.1.6.1.1.2	Contracts / Procurement	4/3	12/30
16	4.1.6.1.1.3	Project Control	4/3	12/30
17	4.1.6.1.1.4	Project Scheduling	4/3	12/30
18	**4.1.6.1.1.5**	**Configuration & Data Management**	4/3	12/30
23	4.1.6.1.1.6	GSFC Code Taxes	4/3	12/30
24	4.1.6.1.1.7	Travel	4/3	12/30
25	4.1.6.1.1.8	ADP & Computer Support	4/3	12/30
26	**4.1.6.1.1.9**	**ACD Shipping**	11/20	4/26
34	4.1.6.1.1.A	Program Review Support	4/3	12/30
35	4.1.6.1.1.A	Shell Peer Review	1/21	1/21
36	**4.1.6.1.2**	**System / Subsystems Engineering**	4/1	12/30
37	**4.1.6.1.2.1**	**System / Subsystem Requirements and Specifications**	4/1	10/29
39	**4.1.6.1.2.2**	**System / Subsystem Interface Definition & Control**	2/15	9/4
42	**4.1.6.1.2.3**	**Subsystems Analyses and Trade Studies**	11/7	4/29
53	**4.1.6.1.2.4**	**System / Subsystem Engineering**	4/4	12/30
55	4.1.6.1.3	Science Support	4/3	12/30
56	4.1.6.1.4	Simulations	4/3	12/30
57	**4.1.6.2**	**Reliability and Quality Assurance**	4/1	12/30

Anti-Coincidence Detector Subsystem Schedule (Preliminary)

ID	WBS	Task Name
58	4.1.6.2.1	Reliability
68	4.1.6.2.2	Safety
81	4.1.6.2.3	Flight Assurance
96	4.1.6.2.4	Parts Control
102	4.1.6.2.5	Materials
110	4.1.6.3	Tile Shell Assembly (TSA)
111	4.1.6.3.1	Tile Shell Assembly (TSA) Analysis / Design
116	4.1.6.3.2	Tile Detector Assemblies (TDAs)
117	4.1.6.3.2.1	Tile Detector Assembly (TDA) Analysis / Design
145	4.1.6.3.2.2	Wave Shifting Fibers Procurement
152	4.1.6.3.2.3	Photo-Multiplier Tube (PMT) and Divider Assembly Procurement
162	4.1.6.3.2.6	Tile Detector Assy (TDA) Proc/Fab/Assy/Test for DAQ I/F, Full Scale EM (Qual), & Calibration Units
171	4.1.6.3.2.7	Tile Detector Assy (TDA) Proc/Fab/Assy/Test for Flight Unit
180	4.1.6.3.3	Shell Subassembly
181	4.1.6.3.3.1	Shell Subassembly Analysis / Design
187	4.1.6.3.3.3	Shell Subassembly Proc/Fab/Assy/Test for Full Scale EM (Qual) Unit
191	4.1.6.3.3.4	Shell Subassembly Proc/Fab/Assy/Test for DAQ I/F and Calibration Units
194	4.1.6.3.3.5	Shell Subassembly Proc/Fab/Assy/Test for Flight Unit
198	4.1.6.3.4	Tile Mounting Hardware & Assemblies
199	4.1.6.3.4.1	TDA Tiedown Prototype
206	4.1.6.3.4.3	Tile Mounting Hardware & Assembly Proc/Fab/Assy/Test for Full Scale EM (Qual) Unit
209	4.1.6.3.4.4	Tile Mounting Hardware & Assembly Proc/Fab/Assy/Test for DAQ I/F and Calibration Units
211	4.1.6.3.4.5	Tile Mounting Hardware & Assembly Proc/Fab/Assy/Test for Flight Unit

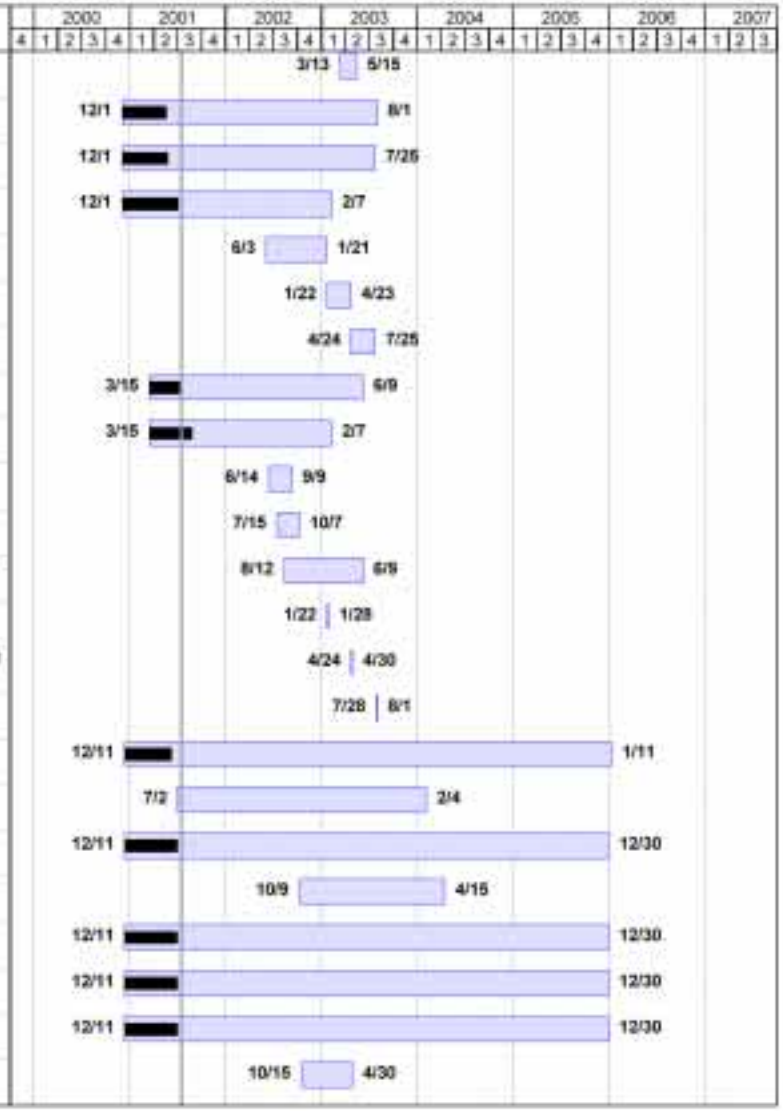


Anti-Coincidence Detector Subsystem Schedule (Preliminary)

ID	WBS	Task Name	
214	4.1.6.3.6	Tile Shell Assembly (TSA) Full Scale EM Unit Integration & Test	11/1 – 1/3
216	4.1.6.3.7	Tile Shell Assembly (TSA) DAQ I/F and Calibration Unit Integration & Test	10/2 – 1/10
221	4.1.6.3.8	Tile Shell Assembly (TSA) Flight Unit Integration & Test	3/3 – 4/28
223	4.1.6.4	Base Electronics Assembly (BEA)	
224	4.1.6.4.1	Base Electronics Assembly (BEA) Analysis / Design	8/1 – 8/30
226	4.1.6.4.2	Base Frame Assembly	2/19 – 3/12
227	4.1.6.4.2.1	Base Frame Assembly Analysis / Design	2/19 – 7/3
230	4.1.6.4.2.3	Base Frame Assembly - Proc/Fab/Assy/Test for Full Scale EM (Qual) Unit	7/5 – 11/13
233	4.1.6.4.2.4	Base Frame Assembly - Proc/Fab/Assy/Test for DAQ I/F and Calibration Units	11/5 – 2/19
236	4.1.6.4.2.5	Base Frame Assembly - Proc/Fab/Assy/Test for Flight Unit	10/21 – 3/12
239	4.1.6.4.3	High Voltage Power Supply Analysis & In-House Build	6/1 – 9/23
248	4.1.6.4.4	Analog ASIC Design / Procurement	9/12 – 9/30
269	4.1.6.4.6	Front-End Electronics and Event (FREE) Circuit Card Assembly (CCA)	3/9 – 5/21
270	4.1.6.4.6.1	FREE CCA Analysis / Design	3/9 – 3/14
335	4.1.6.4.6.3	FREE CCA - Proc/Fab/Assy/Test for DAQ I/F Unit and Full Scale EM	4/5 – 3/28
351	4.1.6.4.6.5	FREE CCA - Proc/Fab/Assy/Test for Flight Unit & Spares	9/30 – 5/21
356	4.1.6.4.9	BEA Electronics Mounting Hardware and Assemblies	3/21 – 6/9
357	4.1.6.4.9.1	BEA Electronics Mounting Hardware & Assembly Analysis / Design	3/21 – 6/26
359	4.1.6.4.9.3	BEA Electronics Mounting Hardware & Assembly Proc/Fab/Assy/Test for Full Scale EM (Qual) Unit	7/5 – 9/27
362	4.1.6.4.9.4	BEA Electronics Mounting Hardware & Assembly Proc/Fab/Assy/Test for DAQ I/F and Calibration Units	8/2 – 10/28
364	4.1.6.4.9.5	BEA Electronics Mounting Hardware & Assembly Proc/Fab/Assy/Test for Flight Unit	8/30 – 6/9
368	4.1.6.4.B	Base Electronics Assembly (BEA) Full Scale EM (Qual) Unit Integration & Test	11/14 – 2/19
371	4.1.6.4.C	Base Electronics Assembly (BEA) for DAQ I/F and Calibration Unit Integration & Test	10/18 – 3/27

Anti-Coincidence Detector Subsystem Schedule (Preliminary)

ID	WBS	Task Name	Start	Finish
377	4.1.6.4.D	**Base Electronics Assembly (BEA) Flight Unit Integration & Test**	3/13	5/15
380	4.1.6.5	**Micrometeoroid Shield / Thermal Blanket Assembly**	12/1	8/1
381	4.1.6.5.1	**Micrometeoroid Shield / Thermal Blanket**	12/1	7/25
382	4.1.6.5.1.1	**Micrometeoroid Shield / Thermal Blanket Analysis / Design**	12/1	2/7
392	4.1.6.5.1.3	**Micrometeoroid Shield / Thermal Blanket Proc/Fab/Assy/Test for Full Scale EM (Qual) Unit**	6/3	1/21
397	4.1.6.5.1.4	**Micrometeoroid Shield / Thermal Blanket Proc/Fab/Assy/Test for Calibration Units**	1/22	4/23
399	4.1.6.5.1.5	**Micrometeoroid Shield / Thermal Blanket Proc/Fab/Assy/Test for Flight Unit**	4/24	7/25
401	4.1.6.5.2	**Micrometeoroid Shield / Thermal Blanket Mounting and Assembly Hardware**	3/15	6/9
402	4.1.6.5.2.1	**Micrometeoroid Shield / Thermal Blanket Mounting and Assembly Hardware Analysis / Design**	3/15	2/7
405	4.1.6.5.2.3	Micrometeoroid Shield / Thermal Blanket Mounting Hardware & Assembly Proc/Fab/Assy/Test for Full Scale EM (Qual) Unit	6/14	9/9
406	4.1.6.5.2.4	Micrometeoroid Shield / Thermal Blanket Mounting Hardware & Assembly Proc/Fab/Assy/Test for DAQ I/F and Calibration Units	7/15	10/7
407	4.1.6.5.2.5	**Micrometeoroid Shield / Thermal Blanket Mounting Hardware & Assembly Proc/Fab/Assy/Test for Flight Unit**	8/12	6/9
411	4.1.6.5.4	Micrometeoroid Shield / Thermal Blanket Full Scale EM (Qual) Unit Integration & Test	1/22	1/28
412	4.1.6.5.5	Micrometeoroid Shield / Thermal Blanket Calibration Unit Integration & Test	4/24	4/30
413	4.1.6.5.6	Micrometeoroid Shield / Thermal Blanket Flight Unit Integration & Test	7/28	8/1
414	4.1.6.6	**Flight Software Development**	12/11	1/11
415	4.1.6.6.1	**ACD Flight Software Design**	7/2	2/4
447	4.1.6.6.2	**ACD TEM Operating System**	12/11	12/30
453	4.1.6.6.3	**ACD Application Software Code & Unit Test**	10/9	4/15
455	4.1.6.6.4	**ACD Support Software**	12/11	12/30
456	4.1.6.6.4.1	**Bench Test Equipment Software Development**	12/11	12/30
473	4.1.6.6.4.2	**Configuration Management S/W**	12/11	12/30
476	4.1.6.6.6	**DAQ I/F Test Unit Software Integration & Test**	10/15	4/30

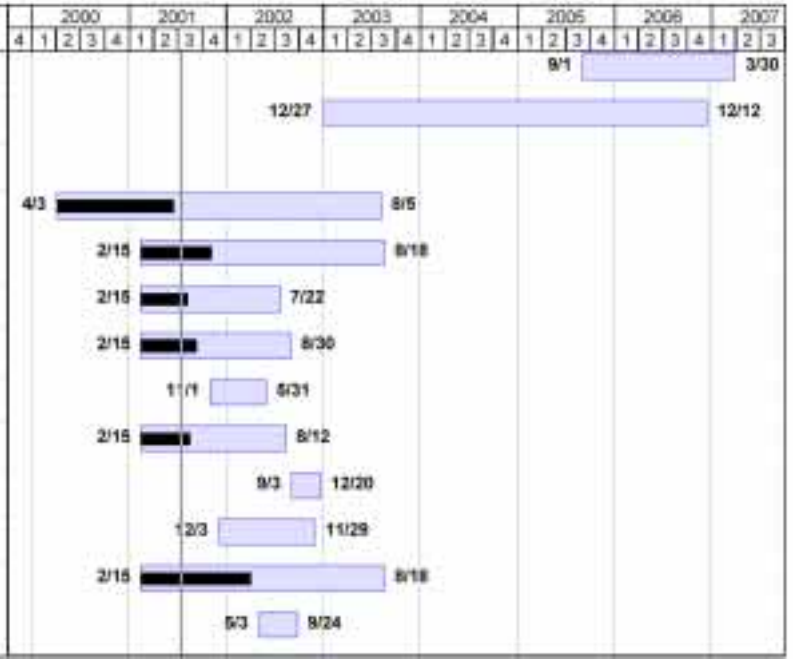


Anti-Coincidence Detector Subsystem Schedule (Preliminary)

ID	WBS	Task Name	Start	Finish
481	4.1.6.6.7	Full Scale EM & Calibration Unit Software Integration & Test	7/16	11/4
487	4.1.6.6.8	Flight Unit Software Integration & Test	3/29	1/11
497	4.1.6.6.9	Flight Software Independent Verification & Validation (IV&V) Support	12/31	1/11
498	4.1.6.7	Hardware / Software Integration & Test		
499	4.1.6.7.1	Miscellaneous LAT Interface / Assembly Hardware	4/2	6/13
500	4.1.6.7.1.1	Miscellaneous LAT Interface / Assembly Hardware Analysis / Design	4/2	1/6
504	4.1.6.7.1.3	Miscellaneous LAT Interface / Assembly Hardware Proc/Fab/Assy/Test for Full Scale EM (Qual) Unit	5/25	12/4
507	4.1.6.7.1.4	Miscellaneous LAT Interface / Assembly Hardware Proc/Fab/Assy/Test for DAQ I/F Test and Calibration Units	7/30	1/7
509	4.1.6.7.1.5	Miscellaneous LAT Interface / Assembly Hardware Proc/Fab/Assy/Test for Flight Unit	1/8	6/13
511	4.1.6.7.3	Full Scale EM (Qual) Unit Hardware / Software Integration & Test	1/3	10/2
515	4.1.6.7.4	DAQ I/F Test and Calibration Unit Hardware / Software Integration & Test	10/15	6/10
529	4.1.6.7.5	Flight Unit Hardware / Software Integration & Test	4/29	1/14
532	4.1.6.8	LAT Instrument Integration & Test Support		
533	4.1.6.8.1	BFEM ACD Integration & Test Support (Balloon Flight)	5/15	8/3
536	4.1.6.8.3	DAQ I/F Test, Full Scale EM, and Calibration Unit ACD Integration & Test Support @ SLAC	2/28	5/25
539	4.1.6.8.4	Flight Unit Integration & Test Support (Flight LAT I&T)	4/27	2/28
541	4.1.6.9	Mission Integration & Test Support	3/31	5/1
542	4.1.6.9.1	Provide ACD Subsystem Support during Flight LAT I&T w/Spacecraft	3/31	1/2
545	4.1.6.9.2	Provide ACD Subsystem Support during Launch Site / Launch Operations	1/3	5/1
547	4.1.6.A	Mission Operations & Data Analysis (MO&DA)	4/3	3/30
548	4.1.6.A.1	MO&DA Science Support Hardware	8/5	5/2
549	4.1.6.A.2	MO&DA Science Support Software	4/3	12/30
550	4.1.6.A.3	MO&DA System Integration & Test	9/5	7/4

Anti-Coincidence Detector Subsystem Schedule (Preliminary)

ID	WBS	Task Name	Start	Finish
551	4.1.6.A.4	MO&DA Support Personnel	9/1	3/30
555	4.1.6.A.5	MO&DA Facilities	12/27	12/12
558	4.1.6.B	Ground Support Facilities and Equipment		
559	4.1.6.B.1	Ground Support Facilities / Facility Modifications	4/3	8/5
560	4.1.6.B.2	Mechanical Ground Support Equipment	2/15	8/18
561	4.1.6.B.2.1	ACD Turnover / Assembly Dolly	2/15	7/22
567	4.1.6.B.2.2	Shell Handling Assembly	2/15	8/30
573	4.1.6.B.2.3	TDA Handling Cases	1/1	5/31
577	4.1.6.B.2.4	Base Frame Handling Assembly	2/15	8/12
584	4.1.6.B.2.5	Grid Interface Template	9/3	12/20
587	4.1.6.B.2.6	ACD Shipping Container w/Nitrogen Purge	12/3	11/29
595	4.1.6.B.2.7	ACD Lifting Slings	2/15	8/18
603	4.1.6.B.3	Electrical Ground Support Equipment	5/3	8/24



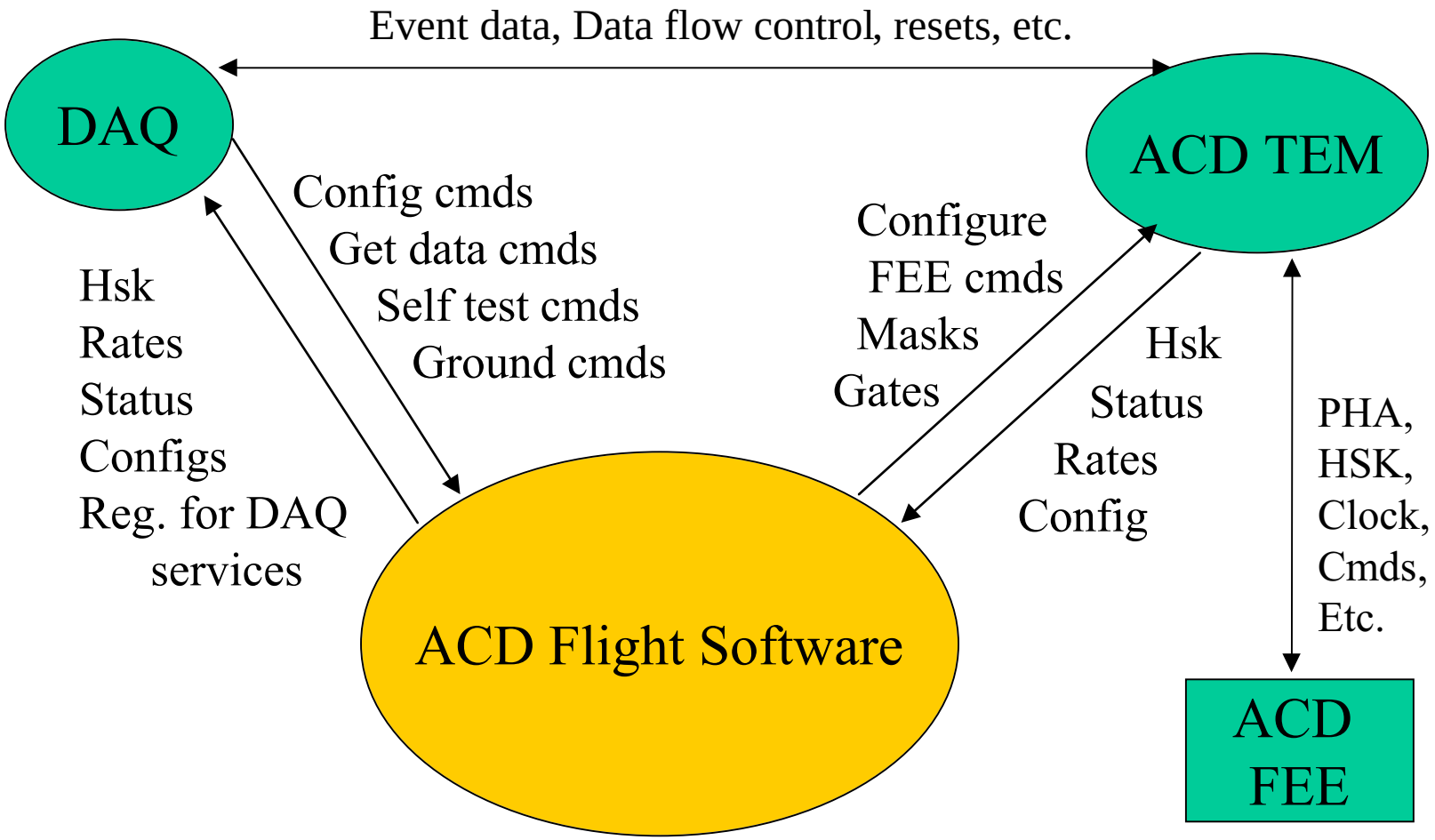
LAT/ACD Software Support (Backup)

LAT/ACD Software Support prepared by Robert Schaefer

LAT/ACD Flight Software Basic Functionality (Backup)

- Configure and Control ACD Instrument.
- Receive and Execute ACD Ground Commands
- Collect ACD Rates and Housekeeping Data
- Run ACD Self-Tests.

LAT/ACD FSW data message flow (Backup)



LAT/ACD Basic Flight Software Modules (Backup)

- ACD_init.c - set defaults, register for DAQ services.
- ACD_DAQ.c - handle communication routing to and from DAQ
- ACD_configure.c - contains functions to configure TEM masks, set thresholds, HV, etc.
- ACD_TEM_cmd.c - handles all cmds sent to ACD electronics
- ACD_rates.c - collects ACD rate data
- ACD_hsk.c - collects housekeeping data

Relevant Design Documents (Backup)

- Flight Software Management Plan (LAT-MD-00104-0)
- ACD Subsystem Specification - Level III (LAT-SS-00016-D7)
- Spacecraft Interface Requirements (GSFC-433-IRD-0001)
- Software Safety Standard NASA-STD-8719.13A
- Recommended Approach to Software Development NASA SEL-81-305 (as a guideline)
- Product Assurance Implementation Plan (LAT-MD-00039)
- CMX manual (Tony Waite)
- IRD for ACD FSW - ACD TEM Interface (TBD)
- IRD for ACD FSW - DAQ FSW Interface (TBD).

FSW Development Specifications (Backup)

- Processor: PowerPC 604e
- Operating System: vxWorks
- Programming Language: C
- Development environment: Wind River Tornado Tools
- Configuration Management Tool: CMX (CMT eXtension)
- Code generated self documentation generated by Doxygen in html and latex. -- for example see balloon code at http://www.slac.stanford.edu/exp/glast/flight/doxygen

LAT/ACD FSW Development (Backup)

- Code developed on Sun workstations
- CMX system can cross-compile and track executables for several target processors.
- All code will be supplied with special comments for use with Doxygen to generate on-line code documentation for immediate use by other FSW team members.
- ACD FSW will deliver a shareable library of functions which interface to DAQ boot and normal operation processes.
- Code package descriptive documentation will be generated for each package and will evolve with code

FSW Testing (Backup)

- Test plans and test code (if necessary) will be supplied with each module.
- Test suites will be built up for testing multiple modules simultaneously
- Test documents will be archived at (TBD).
- Where possible, code should be able to be run on development (Sun) target processors for testing without hardware.
- An electronic bug tracking and delivery notification system (TBD) will be used for software changes and new deliveries.
- Code checks:

  Peer Reviews at key software milestones.

  GSFC LAT Code reviews.

  QA checks by GSFC SATC team (e.g. using C code metrics and requirement specifications checking).

LAT/ACD FSW Team - Additional Tasks (Backup)

- Create ACD Electronics Simulator – allows testing of code without hardware present – Is necessary component for spacecraft telemetry simulator.

- Support ACD/TEM/FEE/Detector development – The ACD FSW is an important tool for diagnosing and testing of the hardware.